M150

Wearable Application Processor

Data Sheet

Release Date: Nov. 12, 2015

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Disclaimer

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1 Overview

M150 is an highly integrated mobile application processor with 128MB LPDDR on-chip, targeting in universal mobile device. Its also fit the requirement of many other embedded applications with its high performance and low power consumption.

1.1 Block Diagram

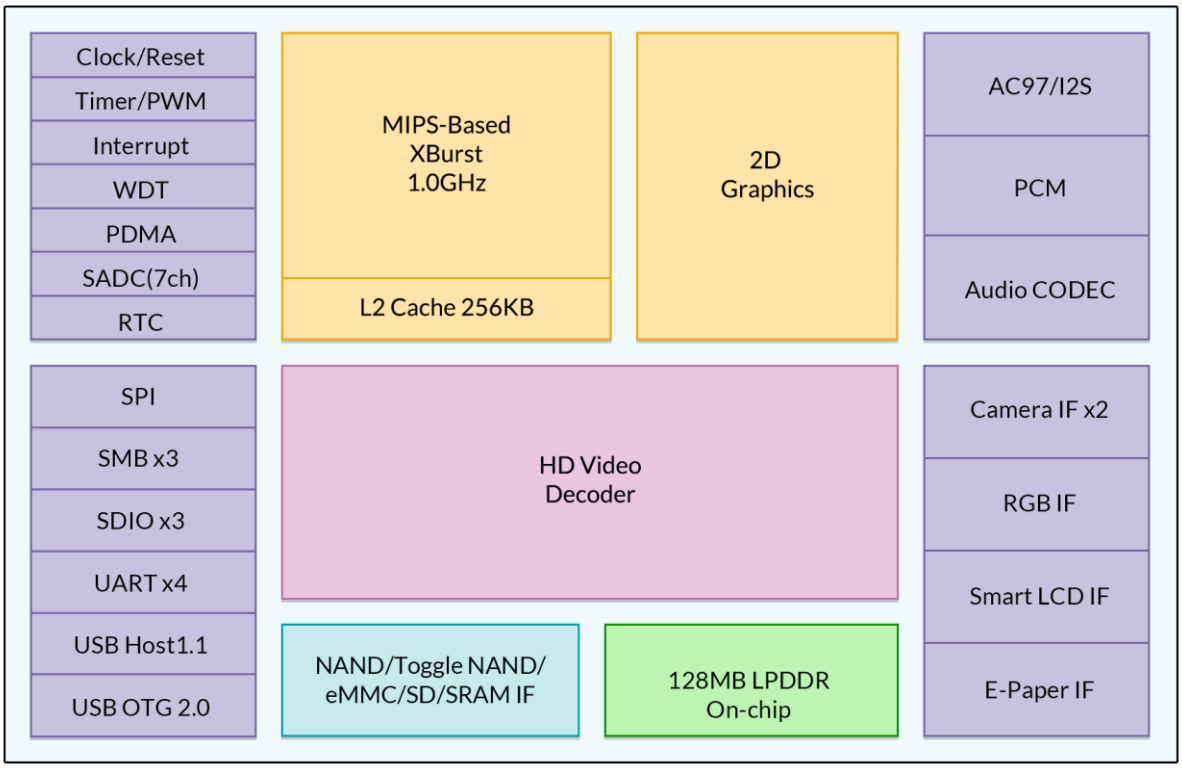


Figure 1-1 M150 Diagram

1.2 Features

1.2.1 CPU

- MIPS-Based XBurst® CPU
  - XBurst® RISC instruction set
  - XBurst® SIMD instruction set
  - XBurst® FPU instruction set supporting both single and double floating point format which are IEEE754 compatible
  - XBurst® 9-stage pipeline micro-architecture, the maximum frequency is 1G
- MMU
  - 32-entry joint-TLB
  - 4 entry Instruction TLB

  - 4 entry data TLB
- L1 Cache
  - 16kB instruction cache
  - 16kB data cache
- Hardware debug support
- 16kB tight coupled memory
- L2 Cache
  - 256kB unify cache

1.2.2 VPU

- MPEG-1/2 decoding up to 720P 30fps
- VC-1 decoding up to 720P 30fps
- H.264 decoding up to 720P 30fps
- VP8 decoding up to 720P 30fps
- MPEG-4 decoding up to 720P 30fps
- RV9 decoding up to 720P 30fps

1.2.3 GPU

- X2D
  - Input format
    - Separate frame: YUV /YCbCr (4:2:0)
    - Packaged data: RGB888, RGB565, RGB555, NV12, NV21,TileYUV
  - Output data format
    - ARGB888，XRGB888, RGB555, RGB565
  - Color convention coefficient: configurable (CSC enable)
  - Minimum input image size (pixel): 4x4
  - Maximum input image size (pixel): 12288x12288 (12k x 12k)
  - Maximum output image size (pixel)
    - Width : up to 12288
    - Height: up to 12288
  - Image resizing
    - bi-cube zooming mode
  - Image Clockwise 90, 180, 270 rotation
  - Image horizontal and vertical mirror , same time with rotation
  - 5 layers OSD

1.2.4 Display/Camera/Audio

- LCD controller(compress must with IPU direct display)
  - Basic Features
    - Support panel(TFT, SLCD)

  - Display size up to 1280*720@60Hz(BPP24)
- Colors Supports
  - Encoded pixel data of 16, 18 or 24 BPP in TFT mode
  - Support up to 16,777,216 (16M) colors in TFT mode
  - Support 24 BPP packed data
- Panel Supports
  - Support 16-bit parallel TFT panel
  - Support 18-bit parallel TFT panel
  - Support 24-bit serial TFT panel with 8 data output pins
  - Support 24-bit parallel TFT panel
  - Support Delta RGB panel
  - Support SLCD panel
- OSD Supports
  - Supports one single color background
  - Supports two foregrounds, and every size can be set for each foreground
  - Supports one transparency for the whole graphic
  - Supports one transparency for each pixel in one graphic
  - Supports color key and mask color key
  - Supports porter-duff blending

- EPD Controller
  - Supports multiple types of compatible EPD panels
  - Supports different size up to 4096x4096@20Hz
  - Supports 2/3/4 bits grayscale and color display
  - Pixel base updating
  - Supports hand-writing mode
  - Supports SW LUT algorithm
  - Supports AUTO-DU, AUTO-GC4 mode
- EPD Color Engine
  - Input data format is RGB565
  - Maximum image direction is 4096x4096
  - Includes CSC between RGB888 and YUV444
  - CSC supports 601 or 709, Wide or Narrow mode
  - Includes 3x3 Color Filter modules for RGB.R, RGB.B, RGB.B and YUV.Y.
  - Includes Color Linearization(VEE) for YUV.Y using 256-grade LUT
  - Supports Color Correction(HUE) for YUV.UV, and the coefficients are configurable
  - Supports Color Saturation for YUV.UV, and the coefficients are configurable
  - Supports Dither for RGB.R, RGB.B, RGB.B and YUV.Y. The output format is 2/3/4-bit configurable.
  - Supports Color Remapping for RGB.R, RGB.B, RGB.B and YUV.Y. If for RGB, there are two methods can be selected between individual CFA component and pixel array. And, the output order is configurable.
  - The EPDCE has a AXI master interface and a AHB slave interface.
  - Input image size up to 2048x2048 pixels

- Integrated DMA
- Supported data format: YCbCr 4:4:4, YCbCr 4:2:2 and other formats
- Supports ITU656 (YCbCr 4:2:2) input
- Configurable VSYNC and HSYNC signals: active high/low
- Configurable PCLK: active edge rising/falling
- 128x66 image data receive FIFO (RXFIFO)
- PCLK max. 30MHz
- Configurable output order

- AC97/I2S/SPDIF controller
  - AC-link (AC97) features
    - Up to 20 bit audio sample data sizes supported
    - DMA transfer mode supported
    - Stop serial clock supported
    - Programmable Interrupt function supported
    - Support mono PCM data to stereo PCM data expansion on audio play back
    - Support endian switch on 16-bits normal audio samples play back
    - Support variable sample rate in AC-link format
    - Multiple channel output and double rated supported for AC-link format
    - Power Down Mode and two Wake-Up modes Supported for AC-link format
  - I2S features
    - 8, 16, 18, 20 and 24 bit audio sample data sizes supported, 16 bits packed sample data is supported
    - DMA transfer mode supported
    - Stop serial clock supported
    - Programmable Interrupt function supported
    - Support mono PCM data to stereo PCM data expansion on audio play back
    - Support endian switch on 16-bits normal audio samples play back
    - Internal programmable or external serial clock and optional system clock supported for I2S or MSB-Justified format
    - Internal I2S CODEC supported
    - Two FIFOs for transmit and receive respectively
- SPDIF features
    - 8, 16, 18, 20 and 24 bit audio sample data sizes supported
    - DMA transfer mode supported
    - Stop serial clock supported
    - Programmable Interrupt function supported
    - Support IEC60958 two-channel PCM audio
    - Support IEC61937 multi-channel compressed audio
    - Support consumer mode and only support transmitter mode
    - Profession mode is not supported
    - The User data bit is ‘0’as it is not supported in the chip
    - Support sampling frequency from 32kHz to 192kHz
- PCM interface

- Data starts with the frame PCMSYN or one PCMCLK later
- Support three modes of operation for PCM
  - Short frame sync mode
  - Long frame sync mode
  - Multi-slot mode
- Data is transferred and received with the MSB first
- Support master mode and slave mode
- The PCM serial output data, PCMDOUT, is clocked out using the rising edge of the PCMSCLK
- The PCM serial input data, PCMDIN, is clocked in on the falling edge of the PCMSCLK
- 8/16 bit sample data sizes supported
- DMA transfer mode supported
- Two FIFOs for transmit and receive respectively with 16 samples capacity in every direction

- Internal CODEC Interface
  - 24 bits ADC and DAC
  - Headphone load up to 16 Ohm
  - Sample frequency supported: 8k, 11.025k, 12k, 16k, 22.05k, 24k, 32k, 44.1k, 48k, and 96k
  - Stereo line input
  - DAC to HP path: Power consumption: 17.6mW, SNR: 95dB, THD: -65dB @17.6mW /16Ohm
  - DAC to stereo line output path @10kOhm: SNR: 95dB A-Weighted, THD: -80dB @FS-1dB
  - Line input to ADC path: SNR: 95dB A-Weighted, THD: -80dB @FS-1dB
  - Separate power-down modes for ADC and DAC path with several shutdown modes
  - Reduction of audible glitches systems: Pop Reduction system, Soft Mute mode
  - Output short circuit protection
  - Digital MIC supported.
  - Support Capacitor-coupled and Capacitor-less mode headphone connection
  - Advance SNR of recode.
  - Update AGC system.
  - Add digital amplitude limiter use for remove the short when sound is very largely.
  - Add DAC digital amplifier the gain up to 32dB.

1.2.5 Memory Interface

- DDR Controller
  - 128MB LPDDR on-chip, up to 320Mbps.
  - Asynchornize to system bus and each port.
  - Support clock-stop mode
  - Support auto-refresh and self-refresh
  - Support power-down mode and deep-power-down mode

- Programmable DDR timing parameters
- Programmable DDR row and column address width and order

- Static memory interface
  - Support 3 external chip selection CS3~1#. Each bank can be configured separately
  - The size and base address of static memory banks are programmable
  - Direct interface to 8/16-bit bus width external memory interface devices or external static memory to each bank. Read/Write strobe setup time and hold time periods can be programmed and inserted in an access cycle to enable connection to low-speed memory
  - Wait insertion by WAIT pin
  - Automatic wait cycle insertion to prevent data bus collisions in case of consecutive memory accesses to different banks, or a read access followed by a write access to the same bank
- NAND flash interface
  - Support on CS3~CS1#, sharing with static memory bank3~bank1
  - Support both of conventional NAND flash memory and Toggle NAND flash memory
  - Support most types of NAND flashes, 8/16-bit data access, 512B/2KB/4KB/8KB/16KB page size. For 512B page size, 3 and 4 address cycles are supported. For 2KB/4KB/8KB/16KB page size, 4 and 5 address cycles are supported
  - Support read/erase/program NAND flash memory
  - Support boot from NAND flash
- BCH Controller
  - Support up to 64-bit ECC encoding and decoding for NAND
- The XBurst® processor system supports little endian only

1.2.6 System Functions

- Clock generation and power management
  - On-chip 24/26MHZ oscillator circuit
  - On-chip 32.768KHZ oscillator circuit
  - One two-chip phase-locked loops (PLL) with programmable multiplier
  - CCLK, HHCLK, H2CLK, PCLK, H0CLK, DDR_CLK, VPU_CLK frequency can be changed separately for software by setting registers
  - SSI clock supports 50M clock
  - MSC clock supports 100M clock
  - Functional-unit clock gating
  - Shut down power supply for J1, VPU, L2CC, X2D
- Timer and counter unit with PWM output and/or input edge counter
  - Provide eight channels, four channels 0~3 can generate PWM, two of them have input signal transition edge counter
  - 16-bit A counter and 16-bit B counter with auto-reload function every channel
  - Support interrupt generation when the A counter underflows
  - Three clock sources: RTCLK (real time clock), EXCLK (external clock input), PCLK (APB Bus clock) selected with 1, 4, 16, 64, 256 and 1024 clock dividing selected

- Every channel has PWM output

- OS timer
  - One channel
  - 32-bit counter and 32-bit compare register
  - Support interrupt generation when the counter matches the compare register
  - Three clock sources: RTCLK (real time clock), EXCLK (external clock input), PCLK (APB Bus clock) selected with 1, 4, 16, 64, 256 and 1024 clock dividing selected
- Interrupt controller
  - Total 64 interrupt sources
  - Each interrupt source can be independently enabled
  - Priority mechanism to indicate highest priority interrupt
  - All the registers are accessed by CPU
  - Unmasked interrupts can wake up the chip in sleep mode
  - Another set of source, mask and pending registers to serve for PDMA
- Watchdog timer
  - Generates WDT reset
  - A 16-bit Data register and a 16-bit counter
  - Counter clock uses the input clock selected by software
    - PCLK, EXTAL and RTCCLK can be used as the clock for counter
    - The division ratio of the clock can be set to 1, 4, 16, 64, 256 and 1024 by software
- PDMA Controller
  - Support up to 32 independent DMA channels
  - Descriptor or No-Descriptor Transfer mode compatible with previous JZ SOC
  - A simple Xburst®-1 CPU supports smart transfer mode controlled by programmable firmware
  - Transfer data units: 1-byte, 2-byte, 4-byte, 16-byte, 32-byte, 64-byte, 128-byte
  - Transfer number of data unit: $1 \sim 2^{24} - 1$
  - Independent source and destination port width: 8-bit, 16-bit, 32-bit
  - Fixed three priorities of channel groups: 0~3, highest; 4~11: mid; 12~31: lowest
  - A dedicated bus interface - BIF interconnects with on-chip BCH
  - A dedicated bus interface - NIF interconnects with on-chip NEMC or off-chip NEMC.
  - An extra INTC IRQ can be bound to one programmable DMA channel
- SAR A/D Controller
  - 7 Channels
  - Resolution: 12-bit
  - Integral nonlinearity: ±1 LSB
  - Differential nonlinearity: ±0.5 LSB
  - Resolution/speed: up to 2Msps
  - Max Frequency: 200k
  - Low power dissipation: 1.5mW(worst)
  - Support 4-wire and 5-wire touch panel measurement (Through pin XP, XN, YP, YN and AUX2)
  - Support multi-touch detect

- Support write control command by software
- Support voltage measurement (Through pin VBAT)
- Support two auxiliary input (Through pin AUX1, AUX2)
- Single-end and Differential Conversion Mode
- Auto X/Y, X/Y/Z1/Z2 and X/Y/Z1/Z2/X2/Y2 position measurement
- Support external touch screen controller

- RTC (Real Time Clock)
  - RTCLK selectable from the oscillator or from the divided clock of EXCLK, so that 32k crystal can be absent if the hibernating mode is not needed
  - 32-bits second counter
  - Programmable and adjustable counter to generate accurate 1 Hz clock
  - Alarm interrupt, 1Hz interrupt
  - Stand alone power supply, work in hibernating mode
  - Power down controller
  - Alarm wakeup
  - External pin wakeup with up to 2s glitch filter

1.2.7 Peripherals

- General-Purpose I/O ports
  - Each port can be configured as an input, an output or an alternate function port
  - Each port can be configured as an interrupt source of low/high level or rising/falling edge triggering. Every interrupt source can be masked independently
  - Each port has an internal pull-up or pull-down resistor connected. The pull-up/down resistor can be disabled
  - GPIO output 7 interrupts, 1 for every group, to INTC
- SMB Controller
  - Two-wire SMB serial interface – consists of a serial data line (SDA) and a serial clock (SCL)
  - Two speeds
    - Standard mode (100 Kb/s)
    - Fast mode (400 Kb/s)
  - Device clock is identical with pclk
  - Programmable SCL generator
  - Master or slave SMB operation
  - 7-bit addressing/10-bit addressing
  - -level transmit and receive FIFOs
  - Interrupt operation
  - The number of devices that you can connect to the same SMB-bus is limited only by the maximum bus capacitance of 400pF
  - APB interface
  - 3 independent SMB channels (SMB0, SMB1, SMB2)
- Synchronous serial interfaces (SSI0)

- 3 protocols support: National's Microwire, TI's SSP, and Motorola's SPI
- Full-duplex or transmit-only or receive-only operation
- Programmable transfer order: MSB first or LSB first
- 128 entries deep x 32 bits wide transmit and receive data FIFOs
- Configurable normal transfer mode or Interval transfer mode
- Programmable clock phase and polarity for Motorola's SSI format
- Two slave select signal (SSI_CE0_ / SSI_CE1_) supporting up to 2 slave devices
- Back-to-back character transmission/reception mode
- Loop back mode for testing

- Four UARTs (UART0, UART1, UART2, UART3)
  - Full-duplex operation
  - 5-, 6-, 7- or 8-bit characters with optional no parity or even or odd parity and with 1, 1½, or 2 stop bits
  - 64x8 bit transmit FIFO and 64x11bit receive FIFO
  - Independently controlled transmit, receive (data ready or timeout), line status interrupts
  - Internal diagnostic capability Loopback control and break, parity, overrun and framing-error is provided
  - Separate DMA requests for transmit and receive data services in FIFO mode
  - Supports modem flow control by software or hardware
  - Slow infrared asynchronous interface that conforms to IrDA specification
- Three MMC/SD/SDIO controllers (MSC0, MSC1, MSC2)
  - Fully compatible with the MMC System Specification version 4.2
  - Support SD Specification 3.0
  - Support SD I/O Specification 1.0 with 1 command channel and 4 data channels
  - Consumer Electronics Advanced Transport Architecture (CE-ATA – version 1.1)
  - Maximum data rate is 50MBps
  - Support MMC data width 1bit ,4bit and 8bit
  - Built-in programmable frequency divider for MMC/SD bus
  - Built-in Special Descriptor DMA
  - Maskable hardware interrupt for SDIO interrupt, internal status and FIFO status
  - 128 x 32 built-in data FIFO
  - Multi-SD function support including multiple I/O and combined I/O and memory
  - IRQ supported enable card to interrupt MMC/SD controller
  - Single or multi block access to the card including erase operation
  - Stream access to the MMC card
  - Supports SDIO read wait, interrupt detection during 1-bit or 4-bit access
  - Supports CE-ATA digital protocol commands
  - Support Command Completion Signal and interrupt to CPU
  - Command Completion Signal disable feature
  - The maximum block length is 4096bytes
- USB 1.1 host interface
  - Open Host Controller Interface OHCI-compatible and USB Revision 1.1-compatible
  - Full speed and low speed

- Embedded USB 1.1 PHY

- USB 2.0 OTG interface
  - Complies with the USB 2.0 standard for high-speed (480 Mbps) functions and with the On-The-Go supplement to the USB 2.0 specification
  - Operates either as the function controller of a high- /full-speed USB peripheral or as the host/peripheral in point-to-point or multi-point communications with other USB functions
  - Supports Session Request Protocol (SRP) and Host Negotiation Protocol (HNP)
  - UTMI+ Level 3 Transceiver Interface
  - Soft connect/disconnect
  - 16 Endpoints:
  - Dedicate FIFO
  - Supports control, interrupt, ISO and bulk transfer
- GMAC controller
  - 10/100/1000 Mbps operation
  - Supports MII、RMII、GMII and RGMII PHY interfaces
  - Supports VLAN and CRC
  - Station Management Agent (SMA)
  - remote wake-up frame and magic packet frame processing
- OTP Slave Interface
  - Total 256 bits. Higher 128bits are read-able and write-able, Lower 128bits are read only

1.2.8 Boot

16kB Boot ROM memory

1.3 Characteristic

Item	Characteristic
Process Technology	65nm CMOS low power
Power supply voltage	General purpose I/O: 1.6~3.6V DDR I/O for LPDDR: 1.8V± 0.15V RTC I/O: 1.8V~3.6V EFUSE programming: 2.5V± 10% Analog power supply 1: 2.5V± 10% Analog power supply 2: 3.3V± 10% Core: 1.2 -0.1/+0.2 V
Package	BGA261,11mm x 11mm x 1.4mm, 0.5mm pitch
Operating frequency	1GHz

2 Packaging and Pinout Information

2.1 Overview

M150 processor is offered in 261-pin BGA package, which is 11mm x 11mm x 1.4mm outline, 21 x 21 matrix ball grid array and 0.5mm ball pitch, show in Figure 2-1. The M150 pin to ball assignment is show in Figure 2-2.

The detailed pin description is listed in Table 2-1~Table 2-24.

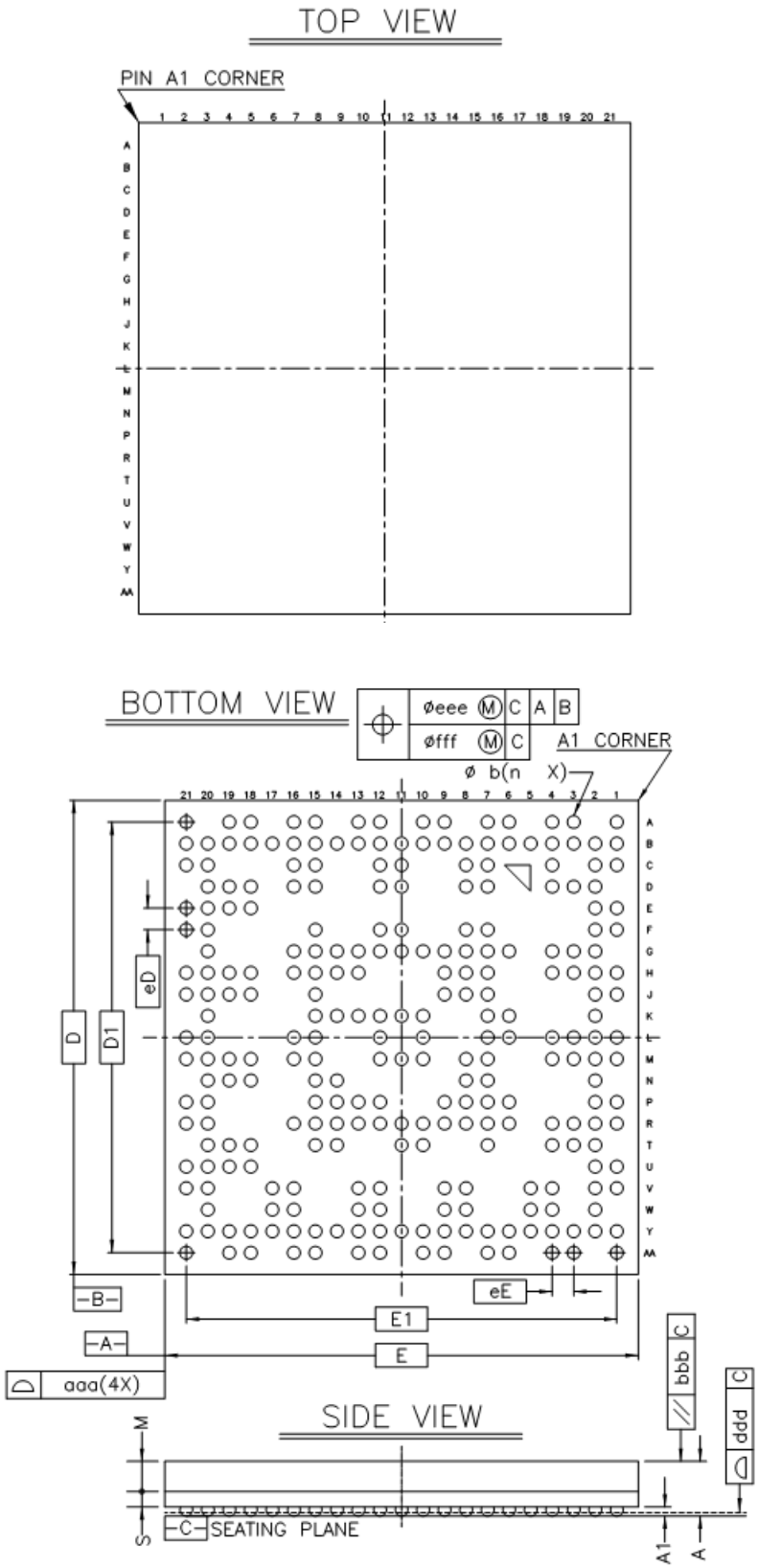
2.2 Solder Process

M150 package is lead-free. It's reflow profile follows the IPC/JEDEC lead-free reflow profile as contained in J-STD-020C.

2.3 Moisture Sensitivity Level

M150 package moisture sensitivity is level 3.

2.4 M150 Package



		Symbol	Common Dimensions
Package :			SNW LFBGA
Body Size:	X	E	11.000
	Y	D	11.000
Ball Pitch :	X	eE	0.500
	Y	eD	0.500
Total Thickness :		A	1.400 Max.
Mold Thickness :		M	0.700 Ref.
Substrate Thickness :		S	0.360 Ref.
Ball Diameter :			0.300
Stand Off :		A1	0.160 ~ 0.260
Ball Width :		b	0.270 ~ 0.370
Package Edge Tolerance :		aaa	0.150
Mold Flatness :		bbb	0.200
Coplanarity:		ddd	0.080
Ball Offset (Package) :		eee	0.150
Ball Offset (Ball) :		fff	0.080
Ball Count :		n	261
Edge Ball Center to Center :	X	E1	10.000
	Y	D1	10.000

Figure 2-1 M150 package outline drawing

M150 Ball Assignment Ver1.0
BGA261, 11mm X 11mm X 1.4mm, 0.5pitch, top view

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	
A	CIM1_D3_SD11_PG13		SA1_PB01	SD6_MSC0_D6_PA06		SD7_MSC0_D7_PA07	SD4_MSC0_D4_PA04		VSSMEM_DDR	VDDMEM_DDR		VSSMEM_DDR	VDDMEM_DDR		VSSMEM_DDR	LCD_DE_PC09		LCD_R2_PC22	LCD_R0_LCD_CLS_UART2_RXD_PC20		LCD_G2_PC12	A
B	CIM1_D4_SD12_PG14	MSC0_D0_SSI0_DR_PA20	SA2_PB02	DQSN_PA29	FRE_MSC0_CLK_SSI0_CLK_PA18	SD3_PA03	CS2_MSC0_D2_PA22	CS1_MSC0_D1_PA21	VSSMEM_DDR	VDDMEM_DDR	VDDMEM_DDR	VSSMEM_DDR	VDDMEM_DDR	VDDMEM_DDR	VSSMEM_DDR	LCD_HSYN_PC18	LCD_R4_PC24	LCD_R6_PC26	LCD_B2_PC02	LCD_G5_PC15	LCD_G1_PC11	B
C	CIM1_D6_SD14_PG16	CIM1_D1_SD9_PG11		SD2_PA02			SD5_MSC0_DS_PA05	CS3_MSC0_D3_SSI0_CE0_PA23		VDDMEM_DDR	VDDMEM_DDR	VDDMEM_DDR			LCD_PCLK_PC08	LCD_VSYN_PC19				LCD_G4_PC14	LCD_B7_PC07	C
D		CIM1_D5_SD13_PG15	SD0_PA00	FWE_MSC0_CMD_SSI0_DT_PA10			SD1_PA01	ZQ			VSSMEM_DDR	VSSMEM_DDR			VREF2	LCD_R3_PC23		LCD_R5_PC25	LCD_B1_LCD_PS_PC01	LCD_G3_PC13		D
E	SA5_PB05	CIM1_D2_SD10_PG12																LCD_R7_PC27	LCD_G6_PC16	LCD_G0_LCD_SPI_UART2_TXD_PC10	LCD_B5_PC05	E
F	SA4_GMAC_CRS_PB04	CIM1_D7_SD15_PG17					VSSQ	VSSQ			VDDQ	VDDQ			VDDQ					LCD_B6_PC06	LCD_B4_PC04	F
G		CIM1_D0_SD8_PG10	SA0_PB00	WE_PA17		VDDIO_N	VDDIO_N	VSSQ	VSSQ	VDDQ	VDDQ	VDDQ	VSSQ	VDDQ	VDDQ	VSSQ				LCD_B3_PC03		G
H	CIM1_HSYN_PG07	SA3_PB03	RD_PA16	WAIT_PA27			CIM0_D1_GMAC_TXD5_EPD_PWR1_PB11	VSS	VSSQ				VSSQ	VDDQ	VDDQ	VSSQ		LCD_R1_PC21	LCD_G7_PC17	LCD_B0_LCD_REV_PC00	AVDEFUSE	H
J	CIM0_VSYN_GMAC_TXER_PB08	CIM1_MCLK_PG09					CIM0_D2_GMAC_TXD6_EPD_SCE2_PB12	VSS	VSS						VSSQ			PWM2_PE02	PWM1_PE01	ADC_YM	ADC_AUX2	J
K		CIM0_MCLK_GMAC_GTXC_EPD_PWC_PB09				CIM0_D7_GMAC_RXD7_EPD_PWR3_PB17	CIM0_HSYN_PB07			VSS	VSS	VSS	VSS	VSS	VSS					ADC_XP		K
L	CIM0_D3_GMAC_TXD7_EPD_SCE3_PB13	CIM0_D6_GMAC_RXD6_EPD_PWR2_PB16	CIM1_PCLK_PG06	CIM1_VSYN_PG08		UART1_TXD_GMAC_TXD2_PD28	VSS			VSS		VSS			VDD	VDD				ADC_AUX1	ADC_VBAT	L
M	CIM0_PCLK_PB06	CIM0_D5_GMAC_RXD5_EPD_SCE5_PB15	CIM0_D4_GMAC_RXD4_EPD_SCE4_PB14	CIM0_D0_GMAC_TXD4_EPD_PWR0_PB10			VSS	VDDIO		VSS	VSS	VSS			VDD	VDD		AVSADC	ADC_XM	ADC_YP	AVDADC	M
N			UART1_RXD_GMAC_RXD2_PD26				UART1_RTS_GMAC_TXD3_PD27	VDDIO						VDD	VDD			MSC0_D3_MSC1_D3_MSC2_D3_PE23	MSC0_CMD_MSC1_CMD_MSC2_CMD_PE29	MSC0_D0_MSC1_D0_MSC2_D0_PE20		N
P	GMAC_MDIO_PCM0_SYN_PF14	GMAC_MDC_PCM0_CLK_PF13				GMAC_COL_PCM0_DI_PF15	UART1_CTS_GMAC_RXD3_PD29	VDDIO	VDDIO			VDD	VDD	VDD	VDD					MSC0_CLK_MSC1_CLK_MSC2_CLK_PE26	MSC0_D1_MSC1_D1_MSC2_D1_PE21	P
R	GMAC_TXEN_PCM0_DO_PF12	GMAC_RXD1_GMAC_IN_EPD_PWR7_PF11	GMAC_RXDV_EPD_PWR5_PF09	GMAC_TXD1_UART2_RXD_PF05		SMB0_SDA_PD30	BOOT_SEL1_PD18	BOOT_SEL2_PD19	PPRST_	TEST_TE	VSS	VSS	TXR_RKL	ID	VSS	VSS				PWM3_SMB2_SCK_SYSCLK_PE03	MSC0_D2_MSC1_D2_MSC2_D2_PE22	R
T		GMAC_RXD0_GMAC_CLK_EPD_PWR6_PF10	GMAC_TXD0_UART2_TXD_PF04	_jtad_TRST_			BOOT_SEL0_PD17			CLK32K_PD14	VSS			UHC_AVSS	VSS			UART0_RTS_SDATI_PF02	UART0_TXD_SDATO_PF03	PWM0_SMB2_SDA_PE00		T
U	GMAC_RXER_EPD_PWR4_PF08	GMAC_TXCLK_PF06																AVSCDC	UART0_RXD_BCLK_PF00	UART0_CTS_LPCLK_PF01	AIL	U
V	GMAC_RXCLK_PF07	TCK_UART3_RTS_PS2_MCLK		SMB1_SDA_PE30	MSC1_D2_SSI0_GPC_PD22			DRV_VBUS_PE10	VSSRTC			PLLAVSS	UHC_DM1			VBUS	AVSHP			MICN1	AIR	V
W		TDI_UART3_RXD_PS2_CCLK_		MSC1_D1_SSI0_DT_PD21	MSC1_CMD_SSI0_CE0_PD25			EXCLK_PD15	LDOOUT			PLLDVSS	UHC_DP1			AOHPM	AOHPMS			MICP1		W
Y	MS_UART2_CTS_PS2_MDATA	SMB0_SCK_PD31	SMB1_SCK_PE31	MSC1_D3_SSI0_CE1_PD23	MSC2_D0_PB20	MSC2_D1_PB21	MSC2_CLK_PB28	MSC2_CMD_PB29	PWRON	XRTCLK	VDDRTC	PLLAVDD	EXCLKO	AVDOTG25	OTG_DM	AOLON	AOLOP	AOHPL	HPSENSE	AVDCDC25	MICBIAS	Y
AA	TDO_UART3_TXD_PS2_KDATA		MSC1_D0_SSI0_DR_PD20	MSC1_CLK_SSI0_CLK_PD24		MSC2_D2_PB30	MSC2_D3_PB31		WKUP_PA30	RTCLK		PLLDVDD	EXCLK		OTG_DP	UHC_AVDD		AOHPR	AVDHP25		VCAP	AA

Figure 2-2 M150 pin to ball assignment

2.5 Pin Description [1][2]

2.5.1 DRAM

Table 2-1 Port 0 DDR Pins (2)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
VREF2	AI	D15		VREF2: input reference voltage for DDR PHY	
ZQ	AIO	D8		Just for test	

2.5.2 BOOT and storage

Implementation	BOOT pin/signal used
NAND flash 8-bit	SD0~SD7, FRE_, FWE_, FRB, CS1_~CS2_, CL(SA0), AL(SA1),
NAND flash 8/16-bit	SD0~SD15, FRE_, FWE_, FRB, CS1_~CS2_, CL(SA0), AL(SA1),
MMC/SD card	MSC0_D0~D3, MSC0_CLK, MSC0_CMD
SPI	SSI0_CLK, SSI0_DT, SSI0_DR, SSI0_CE0_

Implementation	Storage pin/signal used
EBOOK/EPEN	Static memory: SD0~SD7, SA0~SA5, CS1_~CS3_, RD_, WE_, WAIT_

Table 2-2 Static-Memory/MSC0/SPI0 Pins (24)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
SD0 PA00	IO IO	D3	8mA, pullup-pe	SD0: Static memory data bus bit 0 PA0: GPIO group A bit 0	VDDIO_N
SD1 PA01	IO IO	D7	8mA, pullup-pe	SD1: Static memory data bus bit 1 PA1: GPIO group A bit 1	VDDIO_N
SD2 PA02	IO IO	C4	8mA, pullup-pe	SD2: Static memory data bus bit 2 PA2: GPIO group A bit 2	VDDIO_N
SD3 PA03	IO IO	B6	8mA, pullup-pe	SD3: Static memory data bus bit 3 PA3: GPIO group A bit 3	VDDIO_N
SD4 **MSC0_D4** PA04	IO IO IO	A7	8mA, pullup-pe	SD4: Static memory data bus bit 4 MSC0_D4: MSC (MMC/SD) 0 data bit 4 PA4: GPIO group A bit 4	VDDIO_N
SD5 **MSC0_D5** PA05	IO IO IO	C7	8mA, pullup-pe	SD5: Static memory data bus bit 5 MSC0_D5: MSC (MMC/SD) 0 data bit 5 PA5: GPIO group A bit 5	VDDIO_N
SD6 **MSC0_D6** PA06	IO IO IO	A4	8mA, pullup-pe	SD6: Static memory data bus bit 6 MSC0_D6: MSC (MMC/SD) 0 data bit 6 PA6: GPIO group A bit 6	VDDIO_N
SD7 **MSC0_D7** PA07	IO IO IO	A6	8mA, pullup-pe	SD7: Static memory data bus bit 7 MSC0_D7: MSC (MMC/SD) 0 data bit 7 PA7: GPIO group A bit 7	VDDIO_N
SA0 (CL) PB00	O IO	G3	8mA, pulldown-pe, **rst-pe**	SA1: Static memory address bus bit 0 If NAND flash is used, this pin is used as NAND CL (command latch) pin PB0: GPIO group B bit 0	VDDIO_N

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
SA1 (AL) PB01	O IO	A3	8mA, pulldown-pe, **rst-pe**	SA1: Static memory address bus bit 1 If NAND flash is used, this pin is used as NAND AL (address latch) pin PB1: GPIO group B bit 1	VDDIO_N
SA2 PB02	O IO	B3	8mA, pullup-pe	SA2: Static memory address bus bit 2 PB2: GPIO group B bit 2	VDDIO
SA3 PB03	O IO	H2	8mA, pullup-pe	SA3: Static memory address bus bit 3 PB3: GPIO group B bit 3	VDDIO
SA4 GMAC_CRS PB04	O I IO	F1	**4mA(~SL)** pullup-pe	SA4: Static memory address bus bit 4 GMAC_ CRS: Ethernet carrier sense for GMAC PB4: GPIO group B bit 4	VDDIO
SA5 PB05	O IO	E1	8mA, pullup-pe	SA5: Static memory address bus bit 5 PB5: GPIO group B bit 5. NAND flash FRB input 1 candidate	VDDIO
RD_ PA16	O IO	H3	8mA, pullup-pe, **rst-pe**	RD_: Static memory read strobe PA16: GPIO group A bit 16	VDDIO
WE_ PA17	O IO	G4	8mA, pullup-pe, **rst-pe**	WE_: Static memory write strobe PA17: GPIO group A bit 17	VDDIO
FRE_ MSC0_CLK SSI0_CLK PA18	O O O IO	B5	8mA, pullup-pe, **rst-pe**	FRE_: NAND read enable MSC0_CLK: MSC (MMC/SD) 0 clock output SSI0_CLK: SSI 0 clock output PA18: GPIO group A bit 18	VDDIO_N
FWE_ MSC0_CMD SSI0_DT PA19	O O O IO	D4	8mA, pullup-pe, **rst-pe**	FEW_: NAND write enable MSC0_CMD: MSC (MMC/SD) 0 command SSI0_DT: SSI 0 data output PA19: GPIO group A bit 19	VDDIO_N
MSC0_D0 SSI0_DR PA20(FRB0)	IO I IO	B2	8mA, pullup-pe **rst-pe**	MSC0_D0: MSC (MMC/SD) 0 data bit 0 SSI0_DR: SSI 0 data input PA20: GPIO group A bit 20. NAND flash FRB (ready/busy) input 0	VDDIO_N
CS1_ MSC0_D1 PA21	O IO IO	B8	8mA, pullup-pe, **rst-pe**	CS1_: NAND/NOR/SRAM chip select 1 MSC0_D1: MSC (MMC/SD) 0 data bit 1 PA21: GPIO group A bit 21	VDDIO_N
CS2_ MSC0_D2 PA22	O IO IO	B7	8mA, pullup-pe, **rst-pe**	CS2_: NAND/NOR/SRAM chip select 2 MSC0_D2: MSC (MMC/SD) 0 data bit 2 PA22: GPIO group A bit 22	VDDIO_N
CS3_ MSC0_D3 **SSI0_CE0_** PA23	O IO O IO	C8	8mA, pullup-pe, **rst-pe**	CS3_: NAND/NOR/SRAM chip select 3 MSC0_D3: MSC (MMC/SD) 0 data bit 3 **SSI0_CE0_: SSI 0 chip enable 0** PA23: GPIO group A bit 23. NAND flash FRB input 1 candidate	VDDIO_N
WAIT_ PA27(FRB1)	I IO	H4	8mA, pullup-pe	WAIT_: Slow static memory/device wait signal PA27: GPIO group A bit 27. NAND flash FRB input 1 candidate	VDDIO
DQSN PA29	IO IO	B4	8mA pullup-pe	DQSN: Toggle nand DQS pin. PA29: GPIO group A bit 29.	VDDIO_N

2.5.3 LCD/EPD

Table 2-3 LCDC Pins (28; all GPIO shared: PC0~27)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
LCD_B0 LCD_REV PC00	O O IO	H20	8mA, pullup-pe	LCD_B0: LCD Blue data bit 0 LCD_REV: LCD REV output for special TFT PC0: GPIO group C bit 0	VDDIO
LCD_B1 LCD_PS PC01	O O IO	D19	8mA, pullup-pe	LCD_B1: LCD Blue data bit 1 LCD_PS: LCD PS output for special TFT PC01: GPIO group C bit 1	VDDIO

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
LCD_B2 PC02	O IO	B19	8mA, pullup-pe	LCD_B2: LCD Blue data bit 2 PC02: GPIO group C bit 2	VDDIO
LCD_B3 PC03	O IO	G20	8mA, pullup-pe	LCD_B3: LCD Blue data bit 3 PC03: GPIO group C bit 3	VDDIO
LCD_B4 PC04	O IO	F21	8mA, pullup-pe	LCD_B4: LCD Blue data bit 4 PC04: GPIO group C bit 4	VDDIO
LCD_B5 PC05	O IO	E21	8mA, pullup-pe	LCD_B5: LCD Blue data bit 5 PC05: GPIO group C bit 5	VDDIO
LCD_B6 PC06	O IO	F20	8mA, pullup-pe	LCD_B6: LCD Blue data bit 6 PC06: GPIO group C bit 6	VDDIO
LCD_B7 PC07	O IO	C21	8mA, pullup-pe	LCD_B7: LCD Blue data bit 7 PC07: GPIO group C bit 7	VDDIO
LCD_PCLK PC08	O IO	C15	8mA, pullup-pe	LCD_PCLK: LCD pixel clock PC8: GPIO group C bit 8	VDDIO
LCD_DE PC09	O IO	A16	8mA, pullup-pe	LCD_DE: STN AC bias drive/non-STN data enable PC09: GPIO group C bit 9	VDDIO
LCD_G0 LCD_SPL UART2_TxD PC10	O O O IO	E20	8mA, pullup-pe, **rst-pe**	LCD_G0: LCD Green data bit 0 LCD_SPL: LCD SPL output UART2_TxD: UART 2 transmitting data PC10: GPIO group C bit 10	VDDIO
LCD_G1 PC11	O IO	B21	8mA, pullup-pe	LCD_G1: LCD Green data bit 1 PC11: GPIO group C bit 11	VDDIO
LCD_G2 PC12	O IO	A21	8mA, pullup-pe	LCD_G2: LCD Green data bit 2 PC12: GPIO group C bit 12	VDDIO
LCD_G3 PC13	O IO	D20	8mA, pullup-pe	LCD_G3: LCD Green data bit 3 PC13: GPIO group C bit 13	VDDIO
LCD_G4 PC14	O IO	C20	8mA, pullup-pe	LCD_G4: LCD Green data bit 4 PC14: GPIO group C bit 14	VDDIO
LCD_G5 PC15	O IO	B20	8mA, pullup-pe	LCD_G5: LCD Green data bit 5 PC15: GPIO group C bit 15	VDDIO
LCD_G6 PC16	O IO	E19	8mA, pullup-pe	LCD_G6: LCD Green data bit 6 PC16: GPIO group C bit 16	VDDIO
LCD_G7 PC17	O IO	H19	8mA, pullup-pe	LCD_G7: LCD Green data bit 7 PC17: GPIO group C bit 17	VDDIO
LCD_HSYN PC18	IO IO	B16	8mA, pullup-pe	LCD_HSYN: LCD line clock/horizonal sync PC18: GPIO group C bit 18	VDDIO
LCD_VSYN PC19	IO IO	C16	8mA, pullup-pe	LCD_VSYN: LCD frame clock/vertical sync PC19: GPIO group C bit 19	VDDIO
LCD_R0 LCD_CLS UART2_RxD PC20	O O I IO	A19	8mA, pullup-pe	LCD_R0: LCD Red data bit 0 LCD_CLS: LCD CLS output UART2_RxD: UART 2 Receiving data PC20: GPIO group C bit 20	VDDIO
LCD_R1 PC21	O IO	H18	8mA, pullup-pe	LCD_R1: LCD Red data bit 1 PC21: GPIO group C bit 21	VDDIO
LCD_R2 PC22	O IO	A18	8mA, pullup-pe	LCD_R2: LCD Red data bit 2 PC22: GPIO group C bit 22	VDDIO
LCD_R3 PC23	O IO	D16	8mA, pullup-pe	LCD_R3: LCD Red data bit 3 PC23: GPIO group C bit 23	VDDIO
LCD_R4 PC24	O IO	B17	8mA, pullup-pe	LCD_R4: LCD Red data bit 4 PC24: GPIO group C bit 24	VDDIO
LCD_R5 PC25	O IO	D18	8mA, pullup-pe	LCD_R5: LCD Red data bit 5 PC25: GPIO group C bit 25	VDDIO
LCD_R6 PC26	O IO	B18	8mA, pullup-pe	LCD_R6: LCD Red data bit 6 PC26: GPIO group C bit 26	VDDIO
LCD_R7 PC27	O IO	E18	8mA, pullup-pe	LCD_R7: LCD Red data bit 7 PC27: GPIO group C bit 27	VDDIO

2.5.4 MAC/EPD/UART2

Table 2-4 MAC-GMAC/RGMAC/PCM0 Pins (12; all GPIO shared: PF4~15)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
GMAC_TXD0 UART2_TxD PF04	O O IO	T3	**4mA(~SL)**, pulldown-pe	GMAC_TXD0: Ethernet transmit data bit 0 for RMII、MII、RGMII and GMII UART2_TxD: UART 2 transmitting data PF04: GPIO group F bit 4. Pull-down not enabled at and after reset	VDDIO
GMAC_TXD1 UART2_RxD PF05	O I IO	R4	**4mA(~SL)** pulldown-pe	GMAC_TXD1: Ethernet transmit data bit 1 for RMII、MII、RGMII and GMII UART2_RxD: UART 2 Receiving data PF05: GPIO group F bit 5. Pull-down not enabled at and after reset	VDDIO
GMAC_TXCLK (RGMAC_CLK) PF06	I IO	U2	**4mA(~SL)** pulldown-pe	GMAC_TXCLK: Ethernet 25MHz transmit clock for GMAC or (RGMAC_CLK) ethernet 50MHz reference clock for RGMAC input PF06: GPIO group F bit 6. Pull-down not enabled at and after reset	VDDIO
GMAC_RXCLK PF07	I IO	V1	**4mA(~SL)** pulldown-pe	GMAC_RXCLK: Ethernet receive clock for GMAC (25MHz) PF07: GPIO group F bit 7. Pull-down not enabled at and after reset	VDDIO
GMAC_RXER EPD_PWR4 PF08	I O IO	U1	**4mA(~SL)** pulldown-pe	GMAC_RXER: Ethernet receive error EPD_PWR7: EPD power control bit4 PF08: GPIO group F bit 8. Pull-down not enabled at and after reset	VDDIO
GMAC_RXDV EPD_PWR5 PF09	I O IO	R3	**4mA(~SL)** pulldown-pe	GMAC_RXDV: Ethernet receive data valid EPD_PWR7: EPD power control bit5 PF09: GPIO group F bit 9. Pull-down not enabled at and after reset	VDDIO
GMAC_RXD0 DMIC_CLK EPD_PWR6 PF10	I O O IO	T2	**4mA(~SL)** pulldown-pe	GMAC_RXD0: Ethernet receive data bit 0 for RMII、MII、RGMII and GMII DMIC_CLK: Digital MIC clock output EPD_PWR7: EPD power control bit6 PF10: GPIO group F bit 10. Pull-down not enabled at and after reset	VDDIO
GMAC_RXD1 DMIC_IN EPD_PWR7 PF11	I O I IO	R2	**4mA(~SL)** pulldown-pe	GMAC_RXD1: Ethernet receive data bit 1 for RMII、MII、RGMII and GMII DMIC_IN: Digital MIC input EPD_PWR7: EPD power control bit7 PF11: GPIO group F bit 11. Pull-down not enabled at and after reset	VDDIO
GMAC_TXEN PCM0_DO PF12	O O IO	R1	**4mA(~SL)** pullup-pe	GMAC_TXEN: Ethernet transmit enable PCM0_DO: PCM 0 data out PF12: GPIO group F bit 12	VDDIO
GMAC_MDC PCM0_CLK PF13	O IO IO	P2	**4mA(~SL)** pullup-pe	GMAC_MDC: Ethernet management clock for GMAC and RGMAC PCM0_CLK: PCM 0 clock PF13: GPIO group F bit 13	VDDIO
GMAC_MDIO PCM0_SYN PF14	IO IO IO	P1	**4mA(~SL)** pullup-pe	GMAC_MDIO: Ethernet management data for GMAC and RGMAC PCM0_SYN: PCM 0 sync PF14: GPIO group F bit 14	VDDIO
GMAC_COL, PCM0_DI PF15	I IIO	P6	**4mA(~SL)** pullup-pe	GMAC_COL: Ethernet collision for GMAC PCM0_DI: PCM 0 data in PF15: GPIO group F bit 15	VDDIO

2.5.5 CIM0/EPD/GMAC

Table 2-5 CIM/EPD/GMAC Pins (12; all GPIO shared: PB6~17)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
CIM0_PCLK PB06	I IO	M1	8mA, pullup-pe	CIM_PCLK: CIM pixel clock input PB06: GPIO group B bit 6	VDDIO
CIM0_HSYN PB07	I O	K7	8mA, pullup-pe	CIM_HSYN: CIM horizonal sync input PB07: GPIO group B bit 7	VDDIO
CIM0_VSYN	I	J1	**4mA(~SL)**	CIM_VSYN: CIM vertical sync input	VDDIO

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
GMAC_TXER PB08	O IO		pullup-pe, **rst-pe**	GMAC_TXER: PHY Transmit Error PB08: GPIO group B bit 8	
CIM0_MCLK**(** **GMAC_GTXC)** EPD_PWC PB09	O O IO	K2	**8mA(~SL)** pullup-pe	CIM_MCLK: CIM master clock output **()** EPD_PWC: EPD power control common PB09: GPIO group B bit 9	VDDIO
CIM0_D0 GMAC_TXD4 EPD_PWR0 PB10	I O O IO	M4	**4mA(~SL)** pulldown-pe	CIM_D0: CIM data input bit 0. When use 8-bit data, use CIM_D0~D7 GMAC_TXD4: PHY Transmit Data bit 4 for GMII EPD_PWR0: EPD power control bit 0 PB10: GPIO group B bit 10	VDDIO
CIM0_D1 GMAC_TXD5 EPD_PWR1 PB11	I O O IO	H7	**4mA(~SL)** pulldown-pe	CIM_D1: CIM data input bit 1 GMAC_TXD5: PHY Transmit Data bit 5 for GMII EPD_PWR1: EPD power control bit 1 PB11: GPIO group B bit 11	VDDIO
CIM0_D2 GMAC_TXD6 EPD_SCE2_ PB12	I O O IO	J7	**4mA(~SL)** pullup-pe	CIM_D2: CIM data input bit 2 GMAC_TXD6: PHY Transmit Data bit 6 for GMII EPD_SCE2_: EPD source driver chip select 2 PB12: GPIO group B bit 12	VDDIO
CIM0_D3 GMAC_TXD7 EPD_SCE3_ PB13	I O O IO	L1	**4mA(~SL)** pullup-pe	CIM_D3: CIM data input bit 3 GMAC_TXD7: PHY Transmit Data bit 7 for GMII EPD_SCE3_: EPD source driver chip select 3 PB13: GPIO group B bit 13	VDDIO
CIM0_D4 GMAC_RXD4 EPD_SCE4_ PB14	I O I IO	M3	**4mA(~SL)** pullup-pe	CIM_D4: CIM data input bit 4 GMAC_RXD4: PHY Receive Data bit 4 for GMII EPD_SCE4_: EPD source driver chip select 4 PB14: GPIO group B bit 14	VDDIO
CIM0_D5 GMAC_RXD5 EPD_SCE5_ PB15	I O I IO	M2	**4mA(~SL)** pullup-pe	CIM_D5: CIM data input bit 5 GMAC_RXD5: PHY Receive Data bit 5 for GMII EPD_SCE5_: EPD source driver chip select 5 PB15: GPIO group B bit 15	VDDIO
CIM0_D6 GMAC_RXD6 EPD_PWR2 PB16	I O I IO	L2	**4mA(~SL)** pulldown-pe	CIM_D6: CIM data input bit 6 GMAC_RXD6: PHY Receive Data bit 6 for GMII EPD_PWR2: EPD power control bit 2 PB16: GPIO group B bit 16	VDDIO
CIM0_D7 GMAC_RXD7 EPD_PWR3 PB17	I O I IO	K6	**4mA(~SL)** pulldown-pe	CIM_D7: CIM data input bit 7 GMAC_RXD7: PHY Receive Data bit 7 for GMII EPD_PWR3: EPD power control bit 3 PB17: GPIO group B bit 17	VDDIO

2.5.6 CIM1/Storage

Table 2-6 CIM1/ Static-Memory Pins (12; all GPIO shared: PG6~17)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
CIM1_PCLK PG06	I IO	L3	8mA, pullup-pe	CIM_PCLK: CIM pixel clock input PG06: GPIO group G bit 6	VDDIO
CIM1_HSYN PG07	I IO	H1	8mA, pullup-pe	CIM_HSYN: CIM horizonal sync input PG07: GPIO group G bit 7	VDDIO
CIM1_VSYN PG08	I IO	L4	8mA, pullup-pe, rst-pe	CIM_VSYN: CIM vertical sync input PG08: GPIO group G bit 8	VDDIO
CIM1_MCLK PG09	O IO	J2	8mA, pullup-pe	CIM_MCLK: CIM master clock output PG09: GPIO group G bit 9	VDDIO
CIM1_D0 SD8 PG10	I IO IO	G2	8mA, pulldown-pe	CIM_D0: CIM data input bit 0. When use 8-bit data, use CIM_D0~D7 SD8: Static memory data bus bit 8 PG10: GPIO group G bit 10	VDDIO_ N
CIM1_D1	I	C2	8mA,	CIM_D1: CIM data input bit 1	VDDIO_

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
SD9 PG11	IO IO		pulldown-pe	SD9: Static memory data bus bit 9 PG11: GPIO group G bit 11	N
CIM1_D2 SD10 PG12	I IO IO	E2	8mA, pullup-pe	CIM_D2: CIM data input bit 2 SD10: Static memory data bus bit 10 PG12: GPIO group G bit 12	VDDIO_N
CIM1_D3 SD11 PG13	I IO IO	A1	8mA, pullup-pe	CIM_D3: CIM data input bit 3 SD11: Static memory data bus bit 11 PG13: GPIO group G bit 13	VDDIO_N
CIM1_D4 SD12 PG14	I IO IO	B1	8mA, pullup-pe	CIM_D4: CIM data input bit 4 SD12: Static memory data bus bit 12 PG14: GPIO group G bit 14	VDDIO_N
CIM1_D5 SD13 PG15	I IO IO	D2	8mA, pullup-pe	CIM_D5: CIM data input bit 5 SD13: Static memory data bus bit 13 PB15: GPIO group B bit 15	VDDIO_N
CIM1_D6 SD14 PG16	I IO IO	C1	8mA, pulldown-pe	CIM_D6: CIM data input bit 6 SD14: Static memory data bus bit 14 PG16: GPIO group G bit 16	VDDIO_N
CIM1_D7 SD15 PG17	I IO IO	F2	8mA, pulldown-pe	CIM_D7: CIM data input bit 7 SD15: Static memory data bus bit 15 PG17: GPIO group G bit 17	VDDIO_N

2.5.7 UART0

Implementation	Pin/signal used
UART	UART0_TxD, UART0_RxD, UART0_CTS_, UART0_RTS_

Table 2-7 UART0/I2S Pins (4; all GPIO shared: PF0~3)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
UART0_RxD BCLK PF00	I IO IO	U19	8mA, pullup-pe	UART0_RxD: UART 0 Receiving data I2S unified or DAC bit clock PF00: GPIO group F bit 0	VDDIO
UART0_CTS_ LRCLK PF01	I IO IO	U20	4mA, pullup-pe,	UART0_CTS_: UART 0 CTS_ input LRCLK: I2S unified or DAC Left/Right clock PF01: GPIO group F bit 1	VDDIO
UART0_RTS_ SDATI PF02	O I IO	T18	4mA, pullup-pe,	UART0_RTS_: UART 0 RTS_ output SDATI: I2S serial data input PF02: GPIO group F bit 2	VDDIO
UART0_TxD SDATO PF03	O O IO	T19	4mA, pullup-pe,	UART0_TxD: UART 0 transmitting data SDATO: I2S serial data output PF03: GPIO group F bit 3	VDDIO

2.5.8 UART1(DEBUG)

Table 2-8 UART1/GMAC Pins (4; all GPIO shared: PD26~29)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
UART1_RxD GMAC_RXD2 PD26	I I IO	N2	**4mA(~SL)** pullup-pe	UART1_RxD: UART 1 Receiving data GMAC_RXD2: Ethernet receive data bit 2 for MII、RGMII and GMII PD26: GPIO group D bit 26	VDDIO
UART1_CTS_	I	P7	**4mA(~SL)**	UART1_CTS_: UART 1 CTS_ input	VDDIO

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
GMAC_RXD3 PD27	I IO		pullup-pe	GMAC_RXD3: Ethernet receive data bit 3 for MII、RGMII and GMII PD27: GPIO group D bit 27	
UART1_TxD GMAC_TXD2 PD28	O O IO	L6	**4mA(~SL)** pullup-pe, rst-pe	UART1_TxD: UART 1 transmitting data GMAC_TXD2: Ethernet transmit data bit 2 for MII、RGMII and GMII PD28: GPIO group D bit 28	VDDIO
UART1_RTS_ GMAC_TXD3 PD29	O O IO	N7	**4mA(~SL)** pullup-pe, **rst-pe**	UART1_RTS_: UART 1 RTS_ output GMAC_TXD3: Ethernet transmit data bit 3 for MII、RGMII and GMII PD29: GPIO group D bit 29	VDDIO

2.5.9 System/JTAG/UART3(DEBUG Used)

Table 2-9 JTAG/UART3/PS2 Pins (5, GPIO PA30~31 are used to control)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
i_pad TRST_	I	T4	Schmitt, pull-down **rst-pe**	TRST_: JTAG reset	VDDIO
TCK UART3_RTS_ PS2_MCLK	I O	V2	8mA, Schmitt, pulldown-pe, **rst-pe**	TCK: JTAG clock UART3_RTS_: UART 3 RTS_ output	VDDIO
TMS UART3_CTS_ PS2_MDATA	I I	Y1	8mA, Schmitt, pullup-pe, **rst-pe**	TMS: JTAG mode select UART3_CTS_: UART 3 CTS_ input	VDDIO
TDI UART3_RxD PS2_KCLK	I I	W2	8mA, Schmitt, pullup-pe, **rst-pe**	TDI: JTAG serial data input UART3_RxD: UART 3 Receiving data	VDDIO
TDO UART3_TxD PS2_KDATA	O O	AA1	8mA, Schmitt, pullup-pe, **rst-pe**	TDO: JTAG serial data output UART3_TxD: UART 3 transmitting data	VDDIO

2.5.10 SMB0/1

Table 2-10 SMB0/SMB1 Pins (4; all GPIO shared: PD30~31, PE30~31)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
SMB0_SDA PD30	IO IO	R6	8mA, pullup-pe	SMB0_SDA: SMB 0 serial data PD30: GPIO group D bit 30	VDDIO
SMB0_SCK PD31	IO IO	Y2	8mA, pullup-pe	SMB0_SCK: SMB 0 serial clock PD31: GPIO group D bit 31	VDDIO
SMB1_SDA PE30	IO IO	V4	8mA, pullup-pe	SMB1_SDA: SMB 1 serial data PE30: GPIO group E bit 30	VDDIO
SMB1_SCK PE31	IO IO	Y3	8mA, pullup-pe	SMB1_SCK: SMB 1 serial clock PE31: GPIO group E bit 31	VDDIO

2.5.11 MSC1

Implementation	Pin/signal used
SDIO	MSC1_D0~MSC1_D3, MSC1_CLK, MSC1_CMD
SPI	SSI_CLK, SSI_DT, SSI_DR, SSI_CE0_, SSI_CE1_

Table 2-11 MSC1/SSI0, Pins (6; all GPIO shared: PD20~25)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
MSC1_D0 SSI0_DR PD20	IO I IO	AA3	8mA, pullup-pe	MSC1_D0: MSC (MMC/SD) 1 data bit 0 SSI0_DR: SSI 0 data input PD20: GPIO group D bit 20	VDDIO
MSC1_D1 SSI0_DT PD21	IO O IO	W4	8mA, pullup-pe	MSC1_D1: MSC (MMC/SD) 1 data bit 1 SSI0_DT: SSI 0 data output PD21: GPIO group D bit 21	VDDIO
MSC1_D2 SSI0_GPC PD22	IO O IO	V5	8mA, pullup-pe	MSC1_D2: MSC (MMC/SD) 1 data bit 2 SSI0_GPC: SSI 0 general-purpose control signal PD22: GPIO group D bit 22	VDDIO
MSC1_D3 SSI0_CE1_ PD23	IO O IO	Y4	8mA, pullup-pe, **rst-pe**	MSC1_D3: MSC (MMC/SD) 1 data bit 3 SSI0_CE1_: SSI 0 chip enable 1 PD23: GPIO group D bit 23	VDDIO
MSC1_CLK SSI0_CLK PD24	O O IO	AA4	8mA, pullup-pe	MSC1_CLK: MSC (MMC/SD) 1 clock output SSI0_CLK: SSI 0 clock output PD24: GPIO group D bit 24	VDDIO
MSC1_CMD SSI0_CE0_ PD25	IO O IO	W5	8mA, pullup-pe, **rst-pe**	MSC1_CMD: MSC (MMC/SD) 1 command SSI0_CE0_: SSI 0 chip enable 0 PD25: GPIO group D bit 25	VDDIO

2.5.12 MSC2

Implementation	Pin/signal used
SDIO	MSC2_D0~MSC2_D4, MSC2_CLK, MSC2_CMD

Table 2-12 MSC2 Pins (6; all GPIO shared: PB20~21,PB28~31)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
MSC2_D0 PB20	IO IO	Y5	8mA, pullup-pe	MSC2_D0: MSC (MMC/SD) 2 data bit 0 PB20: GPIO group B bit 20	VDDIO
MSC2_D1 PB21	IO IO	Y6	8mA, pullup-pe	MSC2_D1: MSC (MMC/SD) 2 data bit 1 PB21: GPIO group B bit 21	VDDIO
MSC2_CLK PB28	O IO	Y7	8mA, pullup-pe	MSC2_CLK: MSC (MMC/SD) 2 clock output PB28: GPIO group B bit 28	VDDIO
MSC2_CMD PB29	O IO	Y8	8mA, pullup-pe, **rst-pe**	MSC2_CMD: MSC (MMC/SD) 2 command PB29: GPIO group B bit 29	VDDIO
MSC2_D2 PB30	IO IO	AA6	8mA, pullup-pe	MSC2_D2: MSC (MMC/SD) 2 data bit 2 PB30: GPIO group B bit 30	VDDIO
MSC2_D3 PB31	IO IO	AA7	8mA, pullup-pe, **rst-pe**	MSC2_D3: MSC (MMC/SD) 2 data bit 3 PB31: GPIO group B bit 31	VDDIO

2.5.13 MSCx

Table 2-13 MSCx (6; all GPIO shared: PE20~23, PE28~29)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
MSC0_CLK MSC1_CLK MSC2_CLK PE28	O O O IO	P20	8mA, pullup-pe	MSC0_CLK: MSC (MMC/SD) 0 clock output MSC1_CLK: MSC (MMC/SD) 1 clock output MSC2_CLK: MSC (MMC/SD) 2 clock output PE28: GPIO group E bit 28	VDDIO
MSC0_CMD MSC1_CMD MSC2_CMD PE29	O O O IO	N19	8mA, pullup-pe	MSC0_CMD: MSC (MMC/SD) 0 command MSC1_CMD: MSC (MMC/SD) 1 command MSC2_CMD: MSC (MMC/SD) 2 command PE29: GPIO group E bit 29	VDDIO
MSC0_D0 MSC1_D0 MSC2_D0 PE20	IO IO IO IO	N20	8mA, pullup-pe	MSC0_D0: MSC (MMC/SD) 0 data bit 0 MSC1_D0: MSC (MMC/SD) 1 data bit 0 MSC2_D0: MSC (MMC/SD) 2 data bit 0 PE20: GPIO group E bit 20	VDDIO
MSC0_D1 MSC1_D1 MSC2_D1 PE21	IO IO IO IO	P21	8mA, pullup-pe	MSC0_D1: MSC (MMC/SD) 0 data bit 1 MSC1_D1: MSC (MMC/SD) 1 data bit 1 MSC2_D1: MSC (MMC/SD) 2 data bit 1 PE21: GPIO group E bit 21	VDDIO
MSC0_D2 MSC1_D2 MSC2_D2 PE22	IO IO IO IO	R21	8mA, pullup-pe	MSC0_D2: MSC (MMC/SD) 0 data bit 2 MSC1_D2: MSC (MMC/SD) 1 data bit 2 MSC2_D2: MSC (MMC/SD) 2 data bit 2 PE22: GPIO group E bit 22	VDDIO
MSC0_D3 MSC1_D3 MSC2_D3 PE23	IO IO IO IO	N18	8mA, pullup-pe	MSC0_D3: MSC (MMC/SD) 0 data bit 3 MSC1_D3: MSC (MMC/SD) 1 data bit 3 MSC2_D3: MSC (MMC/SD) 2 data bit 3 PE23: GPIO group E bit 23	VDDIO

2.5.14 PWM/SMB2

Table 2-14 PWM/AIC/UART3 Pins (4; all GPIO shared: PE0~3)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
PWM0 SMB2_SDA PE00	IO IO	T20	8mA, **pullup-pe**	PWM0: PWM output or pulse input 0 SMB2_SDA: SMB 2 serial data PE00: GPIO group E bit 0. Pull-down not enabled at and after reset	VDDIO
PWM1 PE01	O IO	J19	8mA, pulldown-pe	PWM1: PWM 1 output. This PWM can run in sleep mode in RTCLK clock PE01: GPIO group E bit 1. Pull-down not enabled at and after reset	VDDIO
PWM2 PE02	O IO	J18	8mA, pullup-pe	PWM2: PWM 2 output. This PWM can run in sleep mode in RTCLK clock PE02: GPIO group E bit 2. Pull-up not enabled at and after reset	VDDIO
PWM3 SMB2_SCK SYSCLK PE03	IO O O IO	R20	8mA, pullup-pe, **rst-pe**	PWM3: PWM output or pulse input 3 SMB2_CLK: SMB 2 serial clock SYSCLK: I2S system clock output PE03: GPIO group E bit 5	VDDIO

Table 2-15 System Pins (3, all GPIO shared: PD17~19)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
PD17 (BOOT_SEL0)	IO I	T7	8mA, pullup-pe	PD17: GPIO group D bit 17 It is taken as BOOT select bit 0 by Boot ROM code	VDDIO
PD18 (BOOT_SEL1)	IO I	R7	8mA, pullup-pe	PD18: GPIO group D bit 18 It is taken as BOOT select bit 1 by Boot ROM code	VDDIO
PD19	IO	R8	8mA,	PD19: GPIO group D bit 19	VDDIO

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
(BOOT_SEL2)	I		pullup-pe	It is taken as BOOT select bit 2 by Boot ROM code	

Table 2-16 USB OTG Digital Pins (1, all GPIO shared: PE10)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
DRV_VBUS PE10	O IO	V8	8mA, pulldown-pe, **rst-pe**	DRVVBUS: USB OTG VBUS driver control signal PE10: GPIO group E bit 10	VDDIO

Table 2-17 EXCLK output Pins (1, all GPIO shared: PD15)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
EXCLKO_ PD15	O IO	W8	8mA, pulldown-pe, **rst-pe**	EXCLKO_: output external clock PD15: GPIO group D bit 15	VDDIO

2.5.15 Digital power/ground

Table 2-18 IO/Core power supplies for BGAs (74)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
VDDQ	P	F11 F12 F15 G10 G11 G12 G14 G15 H14 H15		VDDQ: IO digital power for DDR PHY, 1.8V	-
VSSQ	P	F7 F8 G8 G9 G13 G16 H9 H13 H16 J15		VSSQ: IO digital ground for DDR PHY, 0V	-
VDDMEM_DDR	P	A10 A13 B10 B11 B13 B14 C11 C12		VDDMEM_DDR: Power for LPDDR chip, 1.8V	
VSSMEM_DDR		A9 A12 A15 B9 B12 B15 D11 D12		VSSMEM_DDR: Ground for LPDDR chip, 1.8V	
VDDIO_N	P	G6 G7		VDDIO_N: IO digital power for NAND power domain, 1.8V~3.3V	-
VDDIO	P	M8 N8 P8 P9		VDDIO: IO digital power for none DRAM/NAND, 3.3V	-
VSS	P	H8 J8 J9 K10 K11 K12 K13 K14 K15 L7 L10 L12 M7 M10 M11 M12 R11 R12 R15 R16 T11 T15		VSS: IO digital gound for none DRAM and CORE digital ground, 0V	-

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
VDD	P	L15 L16 M15 M16 N14 N15 P12 P13 P14 P15		VDD: CORE digital power, 1.2V	-

2.5.16 Analog

Table 2-19 Audio CODEC Pins (17)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
MICP1	AI	W20		Microphone mono differential analog input 1 (MIC1), positive pin.	AVDCDC25
MICN1	AI	V20		Microphone mono differential analog input 1 (MIC1), negative pin.	AVDCDC25
MICBIAS	AO	Y21		Microphone bias.	AVDCDC25
AIL	AI	U21		Left line single-ended analog input.	AVDCDC25
AIR	AI	V21		Right line single-ended analog input.	AVDCDC25
AOLOP	AO	Y17		Differential line output, positive pin.	AVDCDC25
AOLON	AO	Y16		Differential line output, negative pin.	AVDCDC25
AOHPL	AO	Y18		Left headphone single-ended analog output.	AVDHP
AOHPR	AO	AA18		Right headphone single-ended analog output.	AVDHP
AOHPM	AO	W16		Headphone common mode output.	AVDHP
AOHPMS	AI	W17		Headphone common mode sense input.	AVDHP
VCAP	AO	AA21		Voltage Reference Output. An 10μF ceramic or tantalum capacitor in parallel with a 0.1μF ceramic capacitor attached from this pin to AVSCDC eliminates the effects of high frequency noise.	AVDCDC25
AVDHP25	P	AA19		Headphone amplifier power, 2.5V.	-
AVSHP	P	V17		Headphone amplifier ground.	-
AVDCDC25	P	Y20		CODEC analog power, 2.5V, inter signal VREFP.	-
AVSCDC	P	U18		CODEC analog ground, inter signal VREFN.	-
HPSENSE	AI	Y19		Headphone jack sense.	AVDHP

Table 2-20 USB 2.0 OTG, USB 1.1 host (10)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
OTG_DP	AIO	AA15		OTG_DP: USB OTG data plus	UHC_AVDD
OTG_DM	AIO	Y15		OTG_DM: USB OTG data minus	UHC_AVDD
VBUS	AIO	V16		VBUS: USB 5-V power supply pin for USB OTG. An external charge pump must provide power to this pin	5V
ID	AI	R14		ID: USB mini-receptacle identifier. It differentiates a mini-A from a mini-B plug. If this signal is not used, internal resistance pulls the signal's voltage level to AVDOTG25.	AVDOTG25

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
TXR_RKL	AIO	R13		TXR_RKL: Transmitter resister tune. It connects to an external resistor of 43.2Ω with 1% tolerance to analog ground, that adjusts the USB 2.0 high-speed source impedance	AVDOTG25
UHC_DP1	AIO	W13		UHC_DP1: USB 1.1 host data plus	UHC_AVDD
UHC_DM1	AIO	V13		UHC_DM1: USB 1.1 host data minus	UHC_AVDD
UHC_AVDD	P	AA16		UHC_AVDD: USB analog power.3.3V	-
UHC_AVSS	P	T14		UHC_AVSS: USB analog ground.	
AVDOTG25	P	Y14		AVDOTG25: USB OTG analog power, 2.5V	-

Table 2-21 SAR ADC Pins (9)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
ADC_XP	AIO	K20		ADC_XP: Touch screen input, X+ for 4-wire, bottom-right for 5-wire	AVDADC
ADC_XM	AIO	M19		ADC_XM: Touch screen input, X- for 4-wire, top-left for 5-wire	AVDADC
ADC_YP	AIO	M20		ADC_YP: Touch screen input Y+ for 4-wire, top-right for 5-wire	AVDADC
ADC_YM	AIO	J20		ADC_YM: Touch screen input Y- for 4-wire, bottom-left for 5-wire	AVDADC
ADC_AUX1	AI	L20		ADC_AUX1: ADC general purpose input	AVDADC
ADC_AUX2	AI	J21		ADC_AUX2: Top sheet connection for 5-wire touch screen or ADC general purpose input	AVDADC
ADC_VBAT	AI	L21		ADC_VBAT: Battery voltage input with external resistance divider or ADC general purpose input	AVDADC
AVDADC	P	M21		AVDADC: ADC analog power, 3.3 V	-
AVSADC	P	M18		AVSADC: ADC analog ground	-

Table 2-22 EFUSE Pins for Two EFUSE (1)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
AVDEFUSE	P	H21		AVDEFUSE: EFUSE programming power, 0V/2.5V	AVDADC

Table 2-23 CPM Pins (6)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
EXCLK	AI	AA13	2~30 MHz Oscillator, OSC on/off	EXCLK: OSC input.	VDDIO
EXCLKO	AO	Y13		EXCLKO: OSC output.	VDDIO
PLLDVDD	P	AA12		PLLDVDD:PLL digital power, 1.2V	-
PLLDVSS	P	W12		PLLDVSS:PLL digital ground	-
PLLAVDD	P	Y12		PLLAVDD: PLL analog power, 1.2V	-
PLLAVSS	P	V12		PLLAVSS: PLL analog ground	-

Table 2-24 RTC Pins (10, 2 with GPIO input: PA30, PD14)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
RTCLK	AI	AA10	32768Hz Oscillator	RTCLK: OSC input	VDD_{RTC}
XRTCLK	AO	Y10		XRTCLK: OSC output or 32768Hz clock input	VDD_{RTC}
PWRON	O	Y9	8mA	PWRON: Power on/off control of main power	VDD_{RTC}
CLK32K PD14	O IO	T10	8mA, pullup-pe	CLK32K: 32768Hz clock output PD14: GPIO group D bit 14. When main power down, this pin is controlled by RTC register: CLK32K or PD14, pull-up enable/disable, input/output if it is PD14, 0/1 if it is PD14 output	VDD_{RTC}
WKUP PA30	I I	AA9	Schmitt	WKUP: Wakeup signal after main power down PA30: GPIO group A bit 30, input/interrupt only	VDD_{RTC}
PPRST_	I	R9	Schmitt	PPRST_: RTC power on reset and RESET-KEY reset input	VDD_{RTC}
TEST_TE	I	R10	Schmitt, pull-down	TEST_TE: Manufacture test enable, program readable	VDD_{RTC}
VDDRTC	P	Y11		VDDRTC: power for RTC and hibernating mode controlling that never power down	-
VSSRTC	P	V9		VSSRTC:	
LDOOUT	AIO	W9		LDOOUT: capacitor pin for RTC LDO need a 1nF decoupling capacitor to ground	

2.5.17 Summary

BGA261 11mm x 11mm x 1.4mm, 0.5 pitch, 21 x 21 matrix

Blocks	Notes		
	BGA8	mA	
DDR	2	-	
Boot & storage: Static/NAND /MSC0/SPI0	24	8	
LCDC/EPD/UART2	28	8	PCLK 8mA
MAC/SPI/UART/EPD	12	8	GMAC-TXD0~1 4mA
CIM0/EPD	12	8	
CIM1/SRAM8~15	12	8	
MSC1/SPI0,1	6	8	
MSC2/SPI0,1	6	8	
MSC0/MSC1/MSC2	6	8	
SMB0/SMB1	4	8	
UART0	4	8	
UART1	4	8	
UART3/JTAG	5		
PWM/SMB2	4	8	
BOOT_SEL	3	8	
OTG DRVVBUS	1	8	
EXCLK_O	1	8	EXCLK output pin

CODEC	17		
USB OTG + USB 2.0 host	10		
SARADC	9		
EFUSE	1		
RTC	10		PA30 is only input/int
Core power(VDD)	10		
Ground for core/IO	22		
IO power/ground for LPDDR chip	16		
IO power/ground for DDR PHY	20		
IO power for NAND	2		
IO P/G for PLL0/1(digital)	2		
IO P/G for PLL0/1(analog)	2		
IO power for other none DRAM	4		IO 3.3 (mainly LCD and others)
EXCLK	1		
EXCLKO	1		
NC	0		
SUM	**261**		

NOTES:

1 The meaning of phases in IO cell characteristics are:
   a Bi-dir, Single-end: bi-direction and single-ended DDR IO are used.
   b Output, Single-end: output and single-ended DDR IO are used.
   c Output, Differential: output and differential signal DDR IO are used.
   d Bi-dir, Differential: bi-direction and differential signal DDR IO are used.
   e 4mA,8mA out: The IO cell's output driving strength is about 4mA,8mA.
   f Pull-up: The IO cell contains a pull-up resistor.
   g Pull-down: The IO cell contains a pull-down resistor.
   h Pullup-pe: The IO cell contains a pull-up resistor and the pull-up resistor can be enabled or disabled by setting corresponding register.
   i Pulldown-pe: The IO cell contains a pull-down resistor and the pull-down resistor can be enabled or disabled by setting corresponding register.
   j rst-pe: these pins are initialed (during reset and after reset) to IO internal pull (up or down) enabled. Otherwise, the pins are initialed to pull disabled
   k Schmitt: The IO cell is Schmitt trig input.
   l ~SL: The IO cell do not limited slew rate.
2 All GPIO shared pins are reset to GPIO input

3 Electrical Specifications

3.1 Absolute Maximum Ratings

The absolute maximum ratings for the processors are listed in Table 3-1. Do not exceed these parameters or the part may be damaged permanently. Operation at absolute maximum ratings is not guaranteed.

Table 3-1 Absolute Maximum Ratings

Parameter	Min	Max	Unit
Storage Temperature	-65	150	°C
Operation Temperature	-40	125	°C
VDDQ power supplies voltage	-0.5	1.98	V
VDDIO power supplies voltage	-0.5	3.6	V
VDDIO_N power supplies voltage	-0.5	3.6	V
VDDcore power supplies voltage	-0.2	1.32	V
AVDPLL power supplies voltage	-0.2	1.32	V
AVDEFUSE power supplies voltage	-0.5	2.75	V
VDDRTC power supplies voltage	-0.5	3.63	V
AVDOTG25 power supplies voltage	-0.5	2.75	V
UHC_AVDD power supplies voltage	-0.5	3.63	V
AVDADC power supplies voltage	-0.5	3.63	V
AVDCDC25 power supplies voltage	-0.5	2.75	V
Input voltage to VDDQ supplied non-supply pins	-0.3	1.98	V
Input voltage to VDDIO supplied non-supply pins with 5V tolerance	-0.5	6.0	V
Input voltage to VDDIO supplied non-supply pins without 5V tolerance	-0.5	3.6	V
Input voltage to VDDIO_N supplied non-supply pins	-0.5	3.6	V
Input voltage to VDDRTC supplied non-supply pins	-0.5	3.6	V
Input voltage to AVDCDC25 supplied non-supply pins	-0.5	2.75	V
Input voltage to AVDOTG25 supplied non-supply pins	-0.5	2.75	V
Input voltage to UHC_AVDD supplied non-supply pins	-0.5	3.63	V
Input voltage to AVDADC supplied non-supply pins	-0.5	3.63	V
Output voltage from VDDQ supplied non-supply pins	-0.5	1.98	V
Output voltage from VDDIO supplied non-supply pins	-0.5	3.6	V
Output voltage from VDDIO_N supplied non-supply pins	-0.5	3.6	V
Output voltage from VDDRTC supplied non-supply pins	-0.5	3.6	V
Output voltage from AVDOTG25 supplied non-supply pins	-0.5	2.75	V
Output voltage from UHC_AVDD supplied non-supply pins	-0.5	3.6	V
Output voltage from AVDADC supplied non-supply pins	-0.5	2.75	V
Output voltage from AVDCDC25 supplied non-supply pins	-0.5	2.75	V

Maximum ESD stress voltage, Human Body Model; Any pin to any supply pin, either polarity, or Any pin to all non-supply pins together, either polarity. Three stresses maximum.		2000	V

3.2 Recommended operating conditions

Table 3-2 Recommended operating conditions for power supplies

Symbol	Description	Min	Typical	Max	Unit
VMEM	VDDQ voltage for LPDDR	1.65	1.8	1.95	V
	VDDMEM_DDR voltage for LPDDR	1.65	1.8	1.95	V
VIO	VDDIO voltage	1.62	-	3.6	V
VION	VDDIO_N voltage	1.62	-	3.6	V
VCORE	VDDcore voltage	1.08	1.2	1.32	V
VPLL	AVDPLL analog voltage	1.08	1.2	1.32	V
VEFUSE	AVDEFUSE voltage	2.25	2.5	2.75	V
VRTC	VDDRTC voltage	1.8	1.8	3.63	V
VUSB25	AVDOTG25 voltage	2.25	2.5	2.75	V
VUSB33	UHC_AVDD voltage	3.0	3.3	3.6	V
VADC	AVDADC voltage	3.0	3.3	3.6	V
VCDC	AVDCDC25 voltage	2.25	2.5	2.75	V

Table 3-3 Recommended operating conditions for VDDQ/VDDMEM_DDR supplied pins

Symbol	Parameter	Min	Typical	Max	Unit
VI18	Input voltage for LPDDR applications	0		1.9	V
VO18	Output voltage for LPDDR applications	0		1.9	V

Table 3-4 Recommended operating conditions for VDDIO/VDDIO_N/VDDRTC supplied pins

Symbol	Parameter	Min	Typical	Max	Unit
V_{IH18}	Input high voltage for 1.8V I/O application	1.17		3.6	V
V_{IL18}	Input low voltage for 1.8V I/O application	–0.3		0.63	V
V_{IH25}	Input high voltage for 2.5V I/O application	1.7		3.6	V
V_{IL25}	Input low voltage for 2.5V I/O application	–0.3		0.7	V
V_{IH33}	Input high voltage for 3.3V I/O application	2		3.6	V
V_{IL33}	Input low voltage for 3.3V I/O application	–0.3		0.8	V

Table 3-5 Recommended operating conditions for others

Symbol	Description	Min	Typical	Max	Unit
T_A	Ambient temperature	–20		85	°C

Table 3-6 Recommended operating conditions for ADC pins

Symbol	Description	Min	Typical	Max	Unit
Vbat	VBAT input voltage range	0		1.15	V
V_{IADC}	ADC_XP/ADC_XM/ADC_YP/ADC_YM/ADC_AUX1/ADC_AUX2 input voltage range	0		AVDADC	V

3.3 DC Specifications

The DC characteristics for each pin include input-sense levels and output-drive levels and currents. These parameters can be used to determine maximum DC loading, and also to determine maximum transition times for a given load. All DC specification values are valid for the entire temperature range of the device.

Table 3-7 DC characteristics for V_{REFMEM} and V_{TT}

Symbol	Parameter	Min	Typical	Max	Unit
VREFM	Reference voltage supply	0.49	0.5	0.51	VMEM
VTT	Terminal Voltage	VREFM – 0.4	VREFM	VREFM + 0.4	V

Table 3-8 DC characteristics for VDDQ/VDDMEM_DDR supplied pins in LPDDR application

Symbol	Parameter	Min	Typical	Max	Unit
$V_{IH(DC)}$	Input logic threshold High	0.7* VMEM		VMEM+0.3	V
$V_{IL(DC)}$	Input logic threshold Low	VMEM-0.3		0.3* VMEM	V
VIH(AC)	AC Input logic High	0.8* VMEM		VMEM+0.3	V
VIL(AC)	AC Input logic Low	VMEM-0.3		0.2* VMEM	V
VOH	DC output logic High (IOH=-0.1mA)	0.9*VMEM			V
VOL	DC output logic Low (IOL=0.1mA)			0.1 *VMEM	V
ILL	Input leakage current		0.01	6.45	uA
IMEM	VMEM quiescent current		0.02	15.03	uA

Table 3-9 DC characteristics for VDDIO/VDDIO_N/VDDRTC supplied pins for 1.8V application

Symbol	Parameter	Min	Typical	Max	Unit
V_T	Threshold point	0.79	0.86	0.94	V
V_{T+}	Schmitt trig low to high threshold point	0.95	1.06	1.16	V
V_{T-}	Schmitt trig high to low threshold point	0.58	0.69	0.79	V
V_{TPU}	Threshold point with pull-up resistor enabled	0.79	0.86	0.94	V
V_{TPD}	Threshold point with pull-down resistor enabled	0.79	0.86	0.94	V

V_{TPU+}	Schmitt trig low to high threshold point with pull-up resistor enabled		0.95	1.06	1.16	V
V_{TPU-}	Schmitt trig high to low threshold point with pull-down resistor enabled		0.58	0.68	0.78	V
V_{TPD+}	Schmitt trig low to high threshold point with pull-down resistor enabled		0.96	1.07	1.17	V
V_{TPD-}	Schmitt trig high to low threshold point with pull-up resistor enabled		0.59	0.69	0.79	V
I_L	Input Leakage Current @ V_I=1.8V or 0V				±10	μA
I_{OZ}	Tri-State output leakage current @ V_I=1.8V or 0V				±10	μA
R_{PU}	Pull-up Resistor		66	114	211	kΩ
R_{PD}	Pull-down Resistor		58	103	204	kΩ
V_{OL}	Output low voltage				0.45	V
V_{OH}	Output high voltage		1.35			V
I_{OL}	Low level output current @ V_{OL}(max)	8mA	5.3	9.8	15.8	mA
		16mA	10.8	19.7	31.8	mA
I_{OH}	High level output current @ V_{OH}(min)	8mA	3.3	8.3	16.6	mA
		16mA	6.6	16.5	33.2	mA

Table 3-10 DC characteristics for VDDIO/VDDIO_N/VDDRTC supplied pins for 2.5V application

Symbol	Parameter	Min	Typical	Max	Unit
V_T	Threshold point	1.06	1.17	1.27	V
V_{T+}	Schmitt trig low to high threshold point	1.27	1.40	1.50	V
V_{T-}	Schmitt trig high to low threshold point	0.86	0.98	1.09	V
V_{TPU}	Threshold point with pull-up resistor enabled	1.05	1.16	1.25	V
V_{TPD}	Threshold point with pull-down resistor enabled	1.06	1.17	1.27	V
V_{TPU+}	Schmitt trig low to high threshold point with pull-up resistor enabled	1.27	1.39	1.48	V
V_{TPU-}	Schmitt trig high to low threshold point with pull-down resistor enabled	0.85	0.97	1.08	V
V_{TPD+}	Schmitt trig low to high threshold point with pull-down resistor enabled	1.27	1.41	1.50	V
V_{TPD-}	Schmitt trig high to low threshold point with pull-up resistor enabled	0.88	0.99	1.10	V
I_L	Input Leakage Current @ V_I=1.8V or 0V			±10	μA
I_{OZ}	Tri-State output leakage current @ V_I=1.8V or 0V			±10	μA
R_{PU}	Pull-up Resistor	43	69	120	kΩ
R_{PD}	Pull-down Resistor	41	66	124	kΩ
V_{OL}	Output low voltage			0.7	V
V_{OH}	Output high voltage	1.7			V

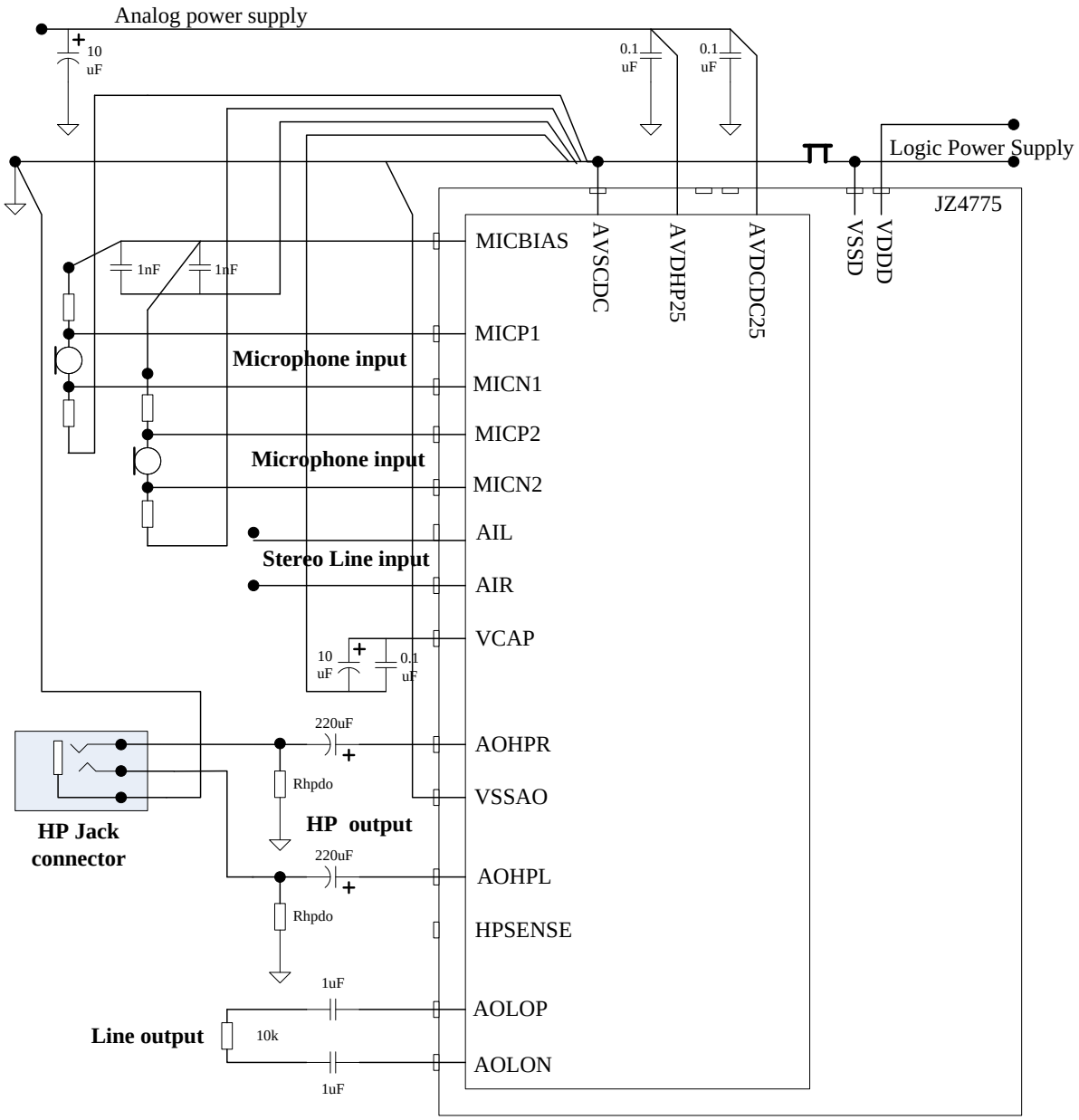
I_{OL}	Low level output current @ V_{OL}(max)	8mA	11.6	19.4	28.4	mA
		16mA	23.3	39.1	57.2	mA
I_{OH}	High level output current @ V_{OH}(min)	8mA	9.3	19.4	34.6	mA
		16mA	18.6	38.7	69.2	mA

Table 3-11 DC characteristics for VDDIO/VDDIO_N/VDDRTC supplied pins for 3.3V application

Symbol	Parameter		Min	Typical	Max	Unit
V_T	Threshold point		1.39	1.50	1.65	V
V_{T+}	Schmitt trig low to high threshold point		1.62	1.75	1.90	V
V_{T-}	Schmitt trig high to low threshold point		1.18	1.29	1.44	V
V_{TPU}	Threshold point with pull-up resistor enabled		1.36	1.48	1.64	V
V_{TPD}	Threshold point with pull-down resistor enabled		1.40	1.52	1.66	V
V_{TPU+}	Schmitt trig low to high threshold point with pull-up resistor enabled		1.62	1.75	1.89	V
V_{TPU-}	Schmitt trig high to low threshold point with pull-down resistor enabled		1.16	1.28	1.43	V
V_{TPD+}	Schmitt trig low to high threshold point with pull-down resistor enabled		1.64	1.77	1.91	V
V_{TPD-}	Schmitt trig high to low threshold point with pull-up resistor enabled		1.19	1.31	1.45	V
I_L	Input Leakage Current @ V_I=1.8V or 0V				±10	μA
I_{OZ}	Tri-State output leakage current @ V_I=1.8V or 0V				±10	μA
R_{PU}	Pull-up Resistor		34	51	81	kΩ
R_{PD}	Pull-down Resistor		35	51	88	kΩ
V_{OL}	Output low voltage				0.4	V
V_{OH}	Output high voltage		2.4			V
I_{OL}	Low level output current @ V_{OL}(max)	4mA	4.9	4.5	10	mA
		8mA	10.0	15.2	20.2	mA
I_{OH}	High level output current @ V_{OH}(min)	4mA	7	14	24.2	mA
		8mA	13.9	28.0	48.2	mA

3.4 Audio codec

3.4.1 Application schematic



Note: 1. The Rhpdo value is 470 Ohm, it use to prevent pop-up noise.

2. AVDCDC25 / AVDHP25 / VCAP each of them requires connecting decoupling capacitors (0.1uF) between the pads AVDCDC25 / AVDHP25 / VCAP and AVSCDC. This ceramic capacitor has to be kept as close as possible to IC package (closer than 0.2 inch)

3.4.2 Line input to audio ADC path

Measurement conditions: T = 25°C, AVDCDC25 = AVDHP = VREFP = 2.5V, input sine wave with a frequency of 1kHz, Fmclk = 12MHz, Fs = 8 to 96kHz, measurement bandwidth 20Hz – 20kHz, unless otherwise specified.					
Parameter	Test conditions	Min.	Typ	Max.	Unit
Input level	Full Scale, Gain GIDL, GIDR = 0dB (note 1)	1.89	2.12	2.39	Vpp
Input resistance		8.5			kOhm
Input capacitance	Includes 10pF for ESD, bonding and package pins capacitances			25	pF
Input bypass capacitor	Cbyline		1		uF

NOTE: The Full Scale input voltage scales with AVDCDC25, equals to 0.85*VREF (typ).

3.4.3 Microphone input to audio ADC path

Measurement conditions: T = 25°C, AVDCDC25 = AVDHP = VREFP = 2.5V, input sine wave with a frequency of 1kHz, Fmclk = 12MHz, Fs = 8 to 96kHz, measurement bandwidth 20Hz – 20kHz, unless otherwise specified.					
Parameter	Test conditions	Min.	Typ	Max.	Unit
Input level	Full Scale, Gain GIDL, GIDR = 0dB, boost gain GIM1,GIM2 = 20dB (note 1)	0.189	0.212	0.239	Vpp
Input resistance (Differential mic configuration)	Boost gain GIM1,GIM2 = 0 dB	66	80	100	kOhm
	Boost gain GIM1,GIM2 = 20 dB	10	13	15	
Input resistance (single-ended mic configuration)	Boost gain GIM1,GIM2 = 0 dB	92	115	138	kOhm
	Boost gain GIM1,GIM2 = 20 dB	19	24	29	
Input capacitance	Includes 10pF for ESD, bonding and package pins capacitances			25	pF
Input bypass capacitor	Cbyline		1		uF

NOTE: The Full Scale input voltage scales with AVDCDC25, equals to 0.085*VREF (typ).

3.4.4 Audio DAC to headphone output path

Measurement conditions: T = 25°C, AVDCDC25 = AVDHP = VREFP = 2.5V, input sine wave with a frequency of 1kHz, Fmclk = 12MHz, Fs = 8 to 96 kHz, measurement bandwidth 20Hz – 20kHz, unless otherwise specified.					
Parameter	Test conditions	Min.	Typ	Max.	Unit
DAC playback on 16 Ohm HeadPhone					
Output level	Full Scale, Gain GOL, GOR = -3 dB, GODL, GODR=0dB, 16 Ohm load	1.33	1.5	1.69	Vpp
Maximum output power	Rl = 16 Ohm		17.6		mW
Output resistance	R1	16			Ohm
Output bypass capacitor	Cl (Rl = 16 Ohm)			220	uF
DAC playback to 10k Ohms lineout single					
Output level	Full Scale, Gain GOL, GOR = 0 dB, GODL, GODR=0dB (note 1)	1.89	2.12	2.39	Vpp
Output resistance	R1	10k			Ohm
Output bypass capacitor	Cl (Rl = 10 kOhm)			1	uF
Common characteristics					
Output capacitance (note 2)	Cp			200	pF

NOTES:

1 The Full Scale output voltage scales with AVDCDC25, equals to 0.85*VREF. The minimum and maximum output levels are given with gain accuracy.

2 Output may oscillate above specified load capacitances. The capacitance is equivalent to a 2-meter cable.

3.4.5 Audio DAC to mono line output path

Measurement conditions: T = 25°C, AVDCDC25 = AVDHP = VREFP = 2.5V, input sine wave with a frequency of 1kHz, Fmclk = 12MHz, Fs = 8 to 96kHz, measurement bandwidth 20Hz – 20kHz, unless otherwise specified.					
Parameter	Test conditions	Min.	Typ	Max.	Unit
Output level	Full Scale, Gain GODL, GODR = 0dB (note 1)	3.78	4.25	4.78	Vpp
Output resistance		10			kOhm
Output capacitance	Cp			100	pF
Output bypass capacitor	Cl (Rl = 10 kOhm)			1	uF

NOTE: The Full Scale output voltage scales with AVDCDC25, equals to 1.7*VREF (typ).

3.4.6 Line input to headphone output path (analog bypass)

Measurement conditions: T = 25°C, AVDCDC25 = AVDHP = VREFP = 2.5V, input sine wave with a frequency of 1kHz, Fmclk = 12MHz, Fs = 8 to 96 kHz, measurement bandwidth 20Hz – 20kHz, unless otherwise specified.					
Parameter	Test conditions	Min.	Typ	Max.	Unit
Input level	Full Scale	1.89	2.12	2.39	Vpp
Input resistance		8.5			kOhm
bypass on 16 Ohm HeadPhone					
Output level	Full Scale, Gain GOL, GOR = -3 dB, GIL, GIR=0dB, 16 Ohm load	1.33	1.5	1.69	Vpp
Output resistance	R1	16			Ohm
bypass to 10k Ohms lineout single					
Output level	Full Scale, Gain GOL, GOR = 0 dB, GIL, GIR=0 dB (note 1)	1.89	2.12	2.39	Vpp
Common characteristics					
Input capacitance	Includes 10pF for ESD, bonding and package pins capacitances			25	pF
Input bypass capacitor	Cbyline		1		uF

NOTE: The Full Scale output voltage scales with AVDCDC25, equals to 1.7*VREF (typ).

3.4.7 Microphone input to headphone output path (analog sidetone)

Measurement conditions: T = 25°C, AVDCDC25 = AVDHP = VREFP = 2.5V, input sine wave with a frequency of 1kHz, Fmclk = 12MHz, Fs = 8 to 96kHz, measurement bandwidth 20Hz – 20kHz, unless otherwise specified.					
Parameter	Test conditions	Min.	Typ	Max.	Unit
Input level	Full Scale, Gain GOL, GOR = 0dB, boost gain GIM1,GIM2 = 20dB (note 1)	0.189	0.212	0.239	Vpp
Output level	Full Scale, Gain GOL,GOR= 0dB, boost gain GIM1,GIM2 = 0 to 20dB, 10kOhm load (note 2)	1.89	2.12	2.39	Vpp
	Full Scale, Gain GOL,GOR= -3 dB, boost gain GIM1,GIM2 = 0 to 20dB, 16Ohm load (note 2)	1.33	1.5	1.69	Vpp

NOTES:

1 The Full Scale input voltage scales with AVDCDC25, equals to 0.085*VREF (typ).

2 The Full Scale output voltage scales with AVDCDC25, equals to 0.85*VREF (typ).

3.4.8 Micbias and reference

Measurement conditions: T = 25°C, AVDCDC25 = AVDHP = VREFP = 2.5V, input sine wave with a frequency of 1kHz, Fmclk = 12MHz, Fs = 8 to 96kHz, measurement bandwidth 20Hz – 20kHz, unless otherwise specified.					
Parameter	Test conditions	Min.	Typ	Max.	Unit
Micbias output level	(note 1)		2.08 1.66		V
Micbias output current				4	mA
Micbias decoupling capacitor	Cmic	0.75	1	1.25	nF
VCAP voltage	(note 2)		2		V

NOTES:

1 Micbias output voltage scales with AVDCDC25, equals to 5/6*VREF or 4/6*VREF (typ).

2 VCAP output voltage scales with AVDCDC25, equals to 0.8*VREF (typ).

3.5 Power On, Reset and BOOT

3.5.1 Power-On Timing

The external voltage regulator and other power-on devices must provide the M150 processor with a specific sequence of power and resets to ensure proper operation. Figure 3-1 shows this sequence and Table 3-9 gives the timing parameters. Following are the name of the power.

- VDDRTC
- AVDAUD: AVDCDC25, AVDHP
- VDD11: all 1.2V power supplies, include VDDCORE, AVDPLL
- VDD: all other digital IO, include DDR power supplies: VDDQ, VDDMEM_DDR, VDDIO, VDDIO_N
- AVD: all other analog power supplies: AVDADC, AVDOTG25, UHC_AVDD
- AVDEFUSE

Table 3-9 Power-On Timing Parameters

Symbol	Parameter	Min	Max	Unit
t_{R_VDDRTC}	VDDRTC rise time[1]	0	5	ms
t_{R_VDD}	VDD rise time[1]	0	5	ms
t_{D_VDD}	Delay between VDDRTC arriving 50% (or 90%) to VDD33 arriving 50% (or 90%)	0	–	ms
t_{R_VDD11}	VDD11 rise time[1]	0	5	ms

t_{D_VDD11}	Delay between VDD arriving 50% (or 90%) to VDD11 arriving 50% (or 90%)	–1	1	ms
t_{R_AVDAUD}	AVDAUD rise time[1]	0	5	ms
t_{D_AVDAUD}	Delay between VDD11 arriving 50% (or 90%) to AVDAUD arriving 50% (or 90%)	0.01	1	ms
t_{R_AVD}	AVD rise time[1]	0	5	ms
t_{D_AVDA}	Delay between VDD arriving 50% to AVD arriving 50%	-1	1	ms
$t_{D\_PPRST\_}$	Delay between VDDAUD stable and PPRST_ deasserted	TBD[3]	–	ms[2]
$t_{D\_VPEFUSE}$	Delay between PPRST_ finished and E-fuse programming power apply	0	–	ms

NOTES:

1 The power rise time is defined as 10% to 90%.

2 The PPRST_ must be kept at least 100us. After PPRST_ is deasserted, the corresponding chip reset will be extended at least 40ms.

3 It must make sure the EXCLK is stable and all power(except AVDEFUSE) is stable.

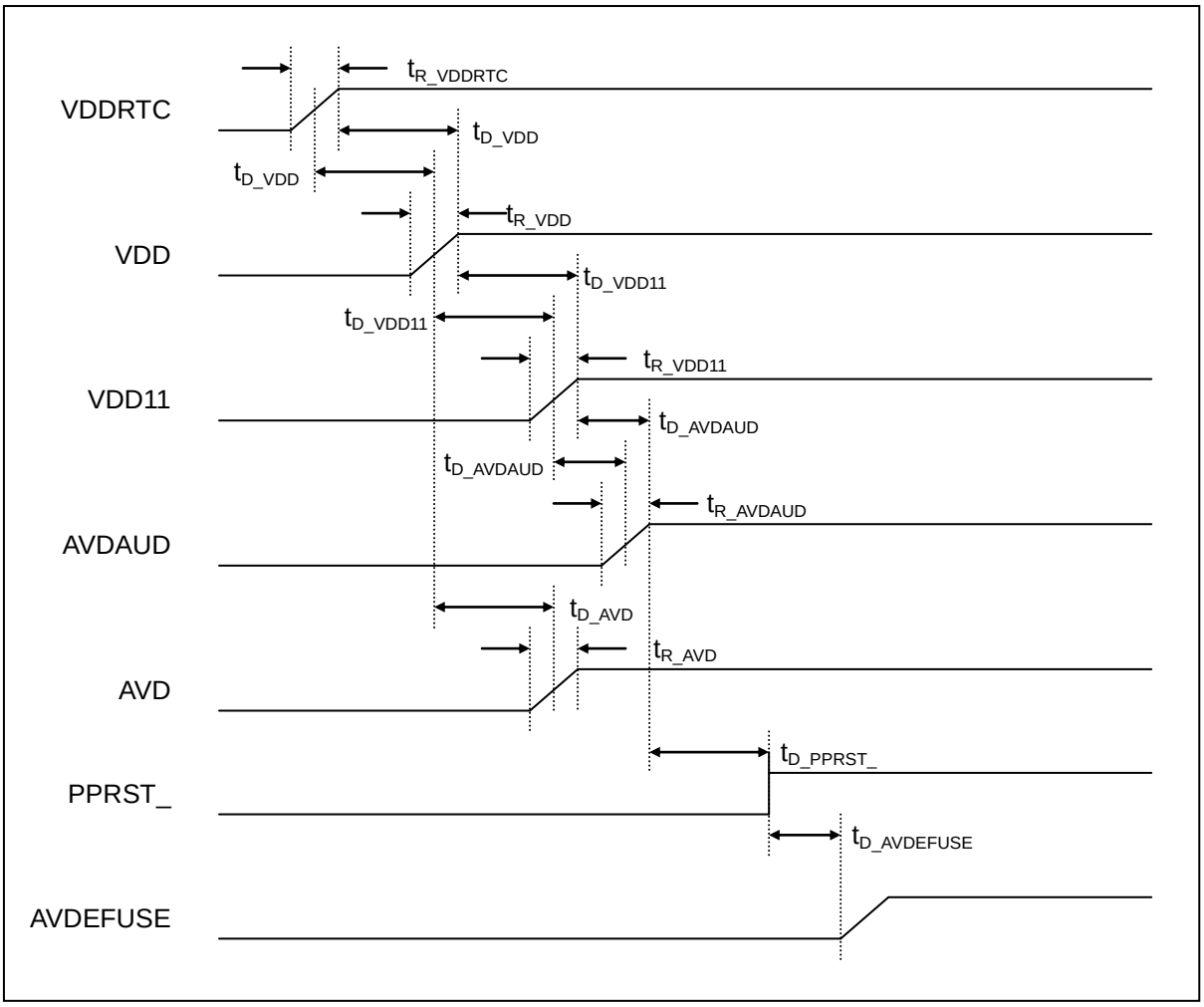


Figure 3-1 Power-On Timing Diagram

3.5.2 Reset procedure

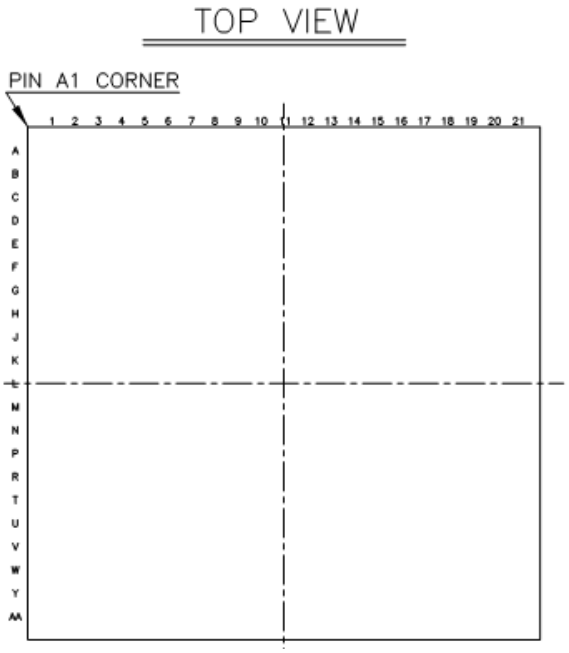
There 3 reset sources: 1 PPRST_ pin reset; 2 WDT timeout reset; and 3 hibernating reset when exiting hibernating mode. After reset, program start from boot.

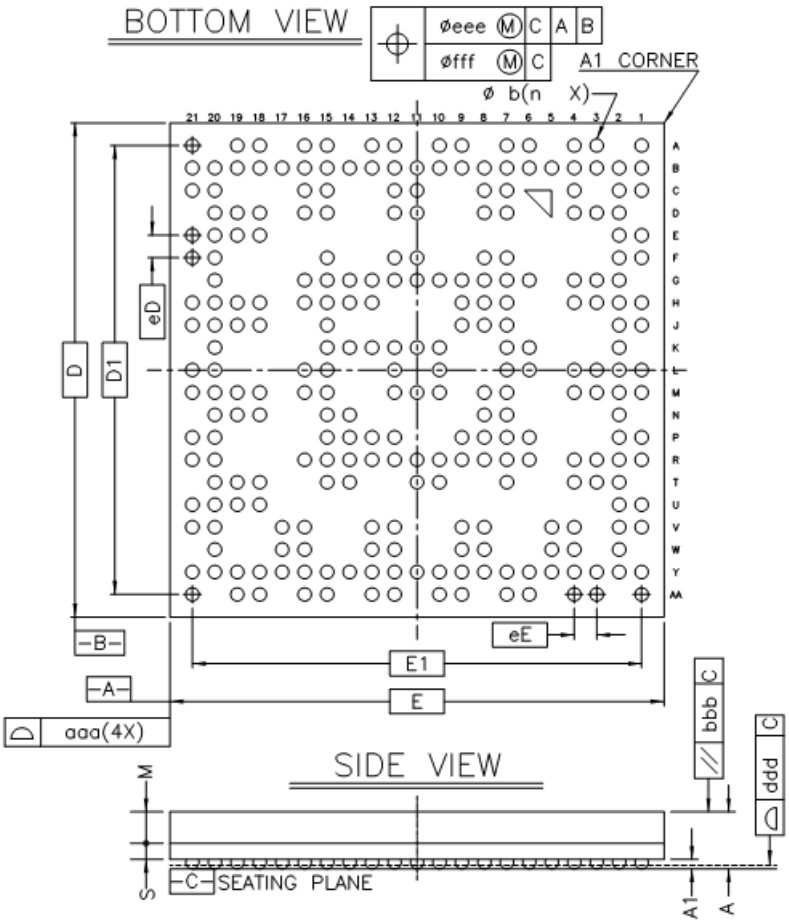
1 PPRST_ pin reset.
This reset is trigged when PPRST_ pin is put to logic 0. It happens in power on RTC power and RESET-KEY pressed to reset the chip from unknown dead state. The reset end time is about 1M EXCLK cycles after rising edge of PPRST_.

2 WDT reset.
This reset happens in case of WDT timeout. The reset keeps for about a few RTCLK cycles.

3 Hibernating reset.
This reset happens in case of wakeup the main power from power down. The reset keeps for about 1ms ~ 125ms programable, plus 1M EXCLK cycles, start after WKUP_ signal is recognized.

After reset, all GPIO shared pins are put to GPIO input function and most of their internal pull-up/down resistor are set to on, see “0





		Symbol	Common Dimensions
Package :			SNW LFBGA
Body Size:	X	E	11.000
	Y	D	11.000
Ball Pitch :	X	eE	0.500
	Y	eD	0.500
Total Thickness :		A	1.400 Max.
Mold Thickness :		M	0.700 Ref.
Substrate Thickness :		S	0.360 Ref.
Ball Diameter :			0.300
Stand Off :		A1	0.160 ~ 0.260
Ball Width :		b	0.270 ~ 0.370
Package Edge Tolerance :		aaa	0.150
Mold Flatness :		bbb	0.200
Coplanarity:		ddd	0.080
Ball Offset (Package) :		eee	0.150
Ball Offset (Ball) :		fff	0.080
Ball Count :		n	261
Edge Ball Center to Center :	X	E1	10.000
	Y	D1	10.000

Figure 2-1 M150 package outline drawing

M150 Ball Assignment Ver1.0
BGA261, 11mm X 11mm X 1.4mm, 0.5pitch, top view

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	
A		CIM1_D3_SD11_PG13		SA1_PB01		SD6_MSC0_D6_PA06		SD7_MSC0_D7_PA07	SD4_MSC0_D4_PA04		VSSMEM_DDR	VDDMEM_DDR		VSSMEM_DDR	VDDMEM_DDR		VSSMEM_DDR	LCD_DE_PC09		LCD_R2_PC22	LCD_R0_LCD_CLS_UART2_RXD_PC20		LCD_G2_PC12	A
B		CIM1_D4_SD12_PG14	MSC0_D0_SSI0_DR_PA20	SA2_PB02	DQSN_PA29	FRE_MSC0_CLK_SSI0_CLK_PA18	SD3_PA03	CS2_MSC0_D2_PA22	CS1_MSC0_D1_PA21	VSSMEM_DDR	VDDMEM_DDR	VDDMEM_DDR	VSSMEM_DDR	VDDMEM_DDR	VDDMEM_DDR	VSSMEM_DDR	LCD_HSYN_PC18	LCD_R4_PC24	LCD_R6_PC26	LCD_B2_PC02	LCD_G5_PC15	LCD_G1_PC11	B
C		CIM1_D6_SD14_PG16	CIM1_D1_SD9_PG11		SD2_PA02			SD5_MSC0_D5_PA05	CS3_MSC0_D3_SSI0_CE0_PA23			VDDMEM_DDR	VDDMEM_DDR			LCD_PCLK_PC08	LCD_VSYN_PC19				LCD_G4_PC14	LCD_B7_PC07	C
D			CIM1_D5_SD13_PG15	SD0_PA00	FWE_MSC0_CMD_SSI0_DT_PA15			SD1_PA01	ZQ			VSSMEM_DDR	VSSMEM_DDR			VREF2	LCD_R3_PC23		LCD_R5_PC25	LCD_B1_LCD_PCLK_PC01	LCD_G3_PC13		D
E		SA5_PB05	CIM1_D2_SD10_PG12																LCD_R7_PC27	LCD_G6_PC16	LCD_G0_LCD_SPL_UART2_TXD_PC10	LCD_B5_PC05	E
F		SA4_GMAC_CRS_PB04	CIM1_D7_SD15_PG17					VSSQ	VSSQ			VDDQ	VDDQ			VDDQ					LCD_B6_PC06	LCD_B4_PC04	F
G			CIM1_D0_SD8_PG10	SA0_PB00	WE_PA17		VDDIO_N	VDDIO_N	VSSQ	VSSQ	VDDQ	VDDQ	VDDQ	VSSQ	VDDQ	VDDQ	VSSQ				LCD_B3_PC03		G
H		CIM1_HSYN_PG07	SA3_PB03	RD_PA16	WAIT_PA27			CIM0_D1_GMAC_TXD5_EPD_PWR1_PB11	VSS	VSSQ				VSSQ	VDDQ	VDDQ	VSSQ		LCD_R1_PC21	LCD_G7_PC17	LCD_B0_LCD_REV_PC00	AVDEFUSE	H
J		CIM0_VSYN_GMAC_TXER_PB08	CIM1_MCLK_PG09					CIM0_D2_GMAC_TXD6_EPD_SCE2_PB12	VSS	VSS						VSSQ			PWM2_PE02	PWM1_PE01	ADC_YM	ADC_AUX2	J
K			CIM0_MCLK_GMAC_GTXC_EPD_PWC_PB09				CIM0_D7_GMAC_RXD7_EPD_PWR3_PB17	CIM0_HSYN_PB07			VSS	VSS	VSS	VSS	VSS	VSS					ADC_XP		K
L		CIM0_D3_GMAC_TXD7_EPD_SCE3_PB13	CIM0_D6_GMAC_RXD6_EPD_PWR2_PB10	CIM1_PCLK_PG06	CIM1_VSYN_PG08		UART1_TXD_GMAC_TXD2_PD28	VSS			VSS		VSS			VDD	VDD				ADC_AUX1	ADC_VBAT	L
M		CIM0_PCLK_PB06	CIM0_D5_GMAC_RXD5_EPD_SCE5_PB15	CIM0_D4_GMAC_RXD4_EPD_SCE4_PB14	CIM0_D0_GMAC_TXD4_EPD_PWR0_PB10			VSS	VDDIO		VSS	VSS	VSS			VDD	VDD		AVSADC	ADC_XM	ADC_YP	AVDADC	M
N			UART1_RXD_GMAC_RXD2_PD26					UART1_RTS_GMAC_TXD3_PD27	VDDIO						VDD	VDD			MSC0_D3_MSC1_D3_MSC2_D3_PE30	MSC0_CMD_MSC1_CMD_MSC2_CMD_PE29	MSC0_D0_MSC1_D0_MSC2_D0_PE28		N
P		GMAC_MDIO_PCM0_SYN_PF14	GMAC_MDC_PCM0_CLK_PF13				GMAC_COL_PCM0_DI_PF15	UART1_CTS_GMAC_RXD3_PD29	VDDIO	VDDIO			VDD	VDD	VDD	VDD					MSC0_CLK_MSC1_CLK_MSC2_CLK_PE26	MSC0_D1_MSC1_D1_MSC2_D1_PE21	P
R		GMAC_TXEN_PCM0_DO_PF12	GMAC_RXD1_DMIC_IN_EPD_PWR7_PF11	GMAC_RXDV_EPD_PWR5_PF09	GMAC_TXD1_UART2_RXD_PF05		SMB0_SDA_PD30	BOOT_SEL1_PD18	BOOT_SEL2_PD19	PPRST_	TEST_TE	VSS	VSS	TXR_RKL	ID	VSS	VSS				PWM3_SMB2_SCK_SYSCLK_PE32	MSC0_D2_MSC1_D2_MSC2_D2_PE22	R
T			GMAC_RXD0_DMIC_CLK_EPD_PWR6_PF10	GMAC_TXD0_UART2_TXD_PF04	L_pad_TRST_			BOOT_SEL0_PD17			CLK32K_PD14	VSS			UHC_AVSS	VSS			UART0_RTS_SDATI_PF02	UART0_TXD_SDATO_PF03	PWM0_SMB2_SDA_PE00		T
U		GMAC_RXER_GPO_PWR4_PF08	GMAC_TXCLK_PF06																AVSCDC	UART0_RXD_BCLK_PF00	UART0_CTS_LRCLK_PF01	AIL	U
V		GMAC_RXCLK_PF07	TCK_UART3_RTS__PS2_MCLK		SMB1_SDA_PE30	MSC1_D2_SSI0_GPC_PD22			DRV_VBUS_PE10	VSSRTC			PLLAVSS	UHC_DM1			VBUS	AVSHP			MICN1	AIR	V
W			TDI_UART3_RXD_PS2_SCLK		MSC1_D1_SSI0_DT_PD23	MSC1_CMD_SSI0_CE0_PD25			EXCLK_PD15	LDOOUT			PLLDVSS	UHC_DP1			AOHPM	AOHPMS			MICP1		W
Y		SMS_UART3_CTS__PS2_SDATA	SMB0_SCK_PD31	SMB1_SCK_PE31	MSC1_D3_SSI0_CE1_PD24	MSC2_D0_PB20	MSC2_D1_PB21	MSC2_CLK_PB28	MSC2_CMD_PB29	PWRON	XRTCLK	VDDRTC	PLLAVDD	EXCLKO	AVDDTG25	OTG_DM	AOLON	AOLOP	AOHPL	HPSENSE	AVDCDC25	MICBIAS	Y
AA		TDO_UART3_TXD_PS2_KDATA		MSC1_D0_SSI0_DR_PD20	MSC1_CLK_SSI0_CLK_PD21		MSC2_D2_PB30	MSC2_D3_PB31		WKUP_PA30	RTCLK		PLLDVDD	EXCLK		OTG_DP	UHC_AVDD		AOHPR	AVDHP25		VCAP	AA
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	

Figure 2-2 M150 pin to ball assignment

Pin Description [1][2]" for details. The PWRON is output 1. The oscillators are on. The USB 2.0 OTG PHY and USB 1.1 PHY, the audio CODEC DAC/ADC, the SAR-ADCs is put in suspend mode.

3.5.3 BOOT

M150 supports 7 different boot sources depending on BOOT_SEL0, BOOT_SEL1 and BOOT_SEL2 pins values. Table 3-10 lists them.

Table 3-10 Boot from 3 boot sources

boot_sel[2:0]	Boot method
110	NAND boot @ CS1
101	SD boot @ MSC0 (MMC/SD use GPIO Port A)
011	eMMC boot @ MSC0 (use GPIO Port A)
000	SPI boot @ SPI0/CE0
010	NOR boot @ CS4 (just for FPGA testing)
111	USB boot @ USB 2.0 device, EXTCLK=24MHz
100	SD boot @ MSC1 (MMC/SD use GPIO Port E)
001	USB boot @ USB 2.0 device, EXTCLK=26MHz

The boot procedure is showed in the following flow chart:

After reset, the boot program on the internal boot ROM executes as follows:

1 Disable all interrupts and read boot_sel[2:0] to determine the boot method.
2 If it is boot from NAND flash, 4 flags at the beginnig of NAND are read to know the NAND information including nand type, page cycle(2 or 3 cycles) and its page size(512B, 2KB, 4KB 8KB or 16KB). Then 14KB code are read out from NAND to tcsm, if the 14KB reading failed, the next 14KB backup in NAND will be read. Then branch to tcsm at 192 bytes offset.
3 There 14KB backup reading failed, the 14KB backup at 128th, 256th , …, and finally 1024th page will be tried in consecutive order.
4 If it is boot from MMC/SD card at MSC0, its function pins MSC0_D0, MSC0_CLK, MSC0_CMD are initialized, the boot program loads the 14KB code from MMC/SD card to tcsm and jump to it. Only one data bus which is MSC0_D0 is used. The clock EXTCLK/128 is used initially. When reading data, the clock EXTCLK/4 is used.
5 If it is boot from eMMC boot partition1 at MSC0, its function pins MSC0_D0, MSC0_CLK, MSC0_CMD are initialized, the boot program loads the 14KB code from eMMC boot partition1 to tcsm and jump to it. Only one data bus which is MSC0_D0 is used. The clock EXTCLK/4 is used.
6 If it is boot from USB, a block of code will be received through USB cable connected with host PC and be stored in tcsm. Then branch to this area in tcsm.
7 If it is boot from MMC/SD card at MSC1, its function pins MSC1_D0,D1,D2,D3, MSC1_CLK, MSC1_CMD are initialized, the boot program loads the 14KB code from MMC/SD card to tcsm and jump to it.

NOTE: The M150's tcsm is 16KB, its address is from 0xf4000000 to 0xf4004000.