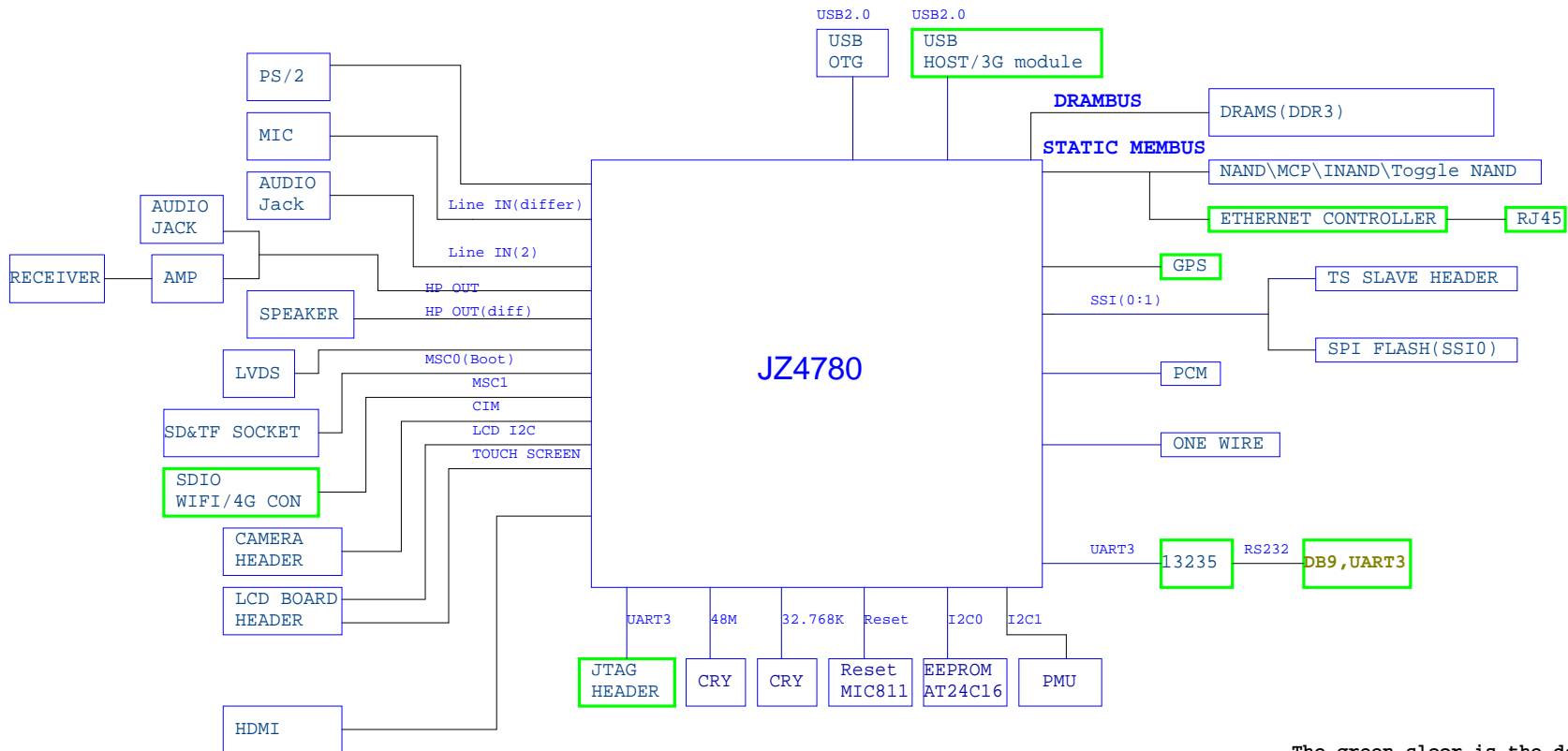




# RD4780\_GRUS\_BOARD

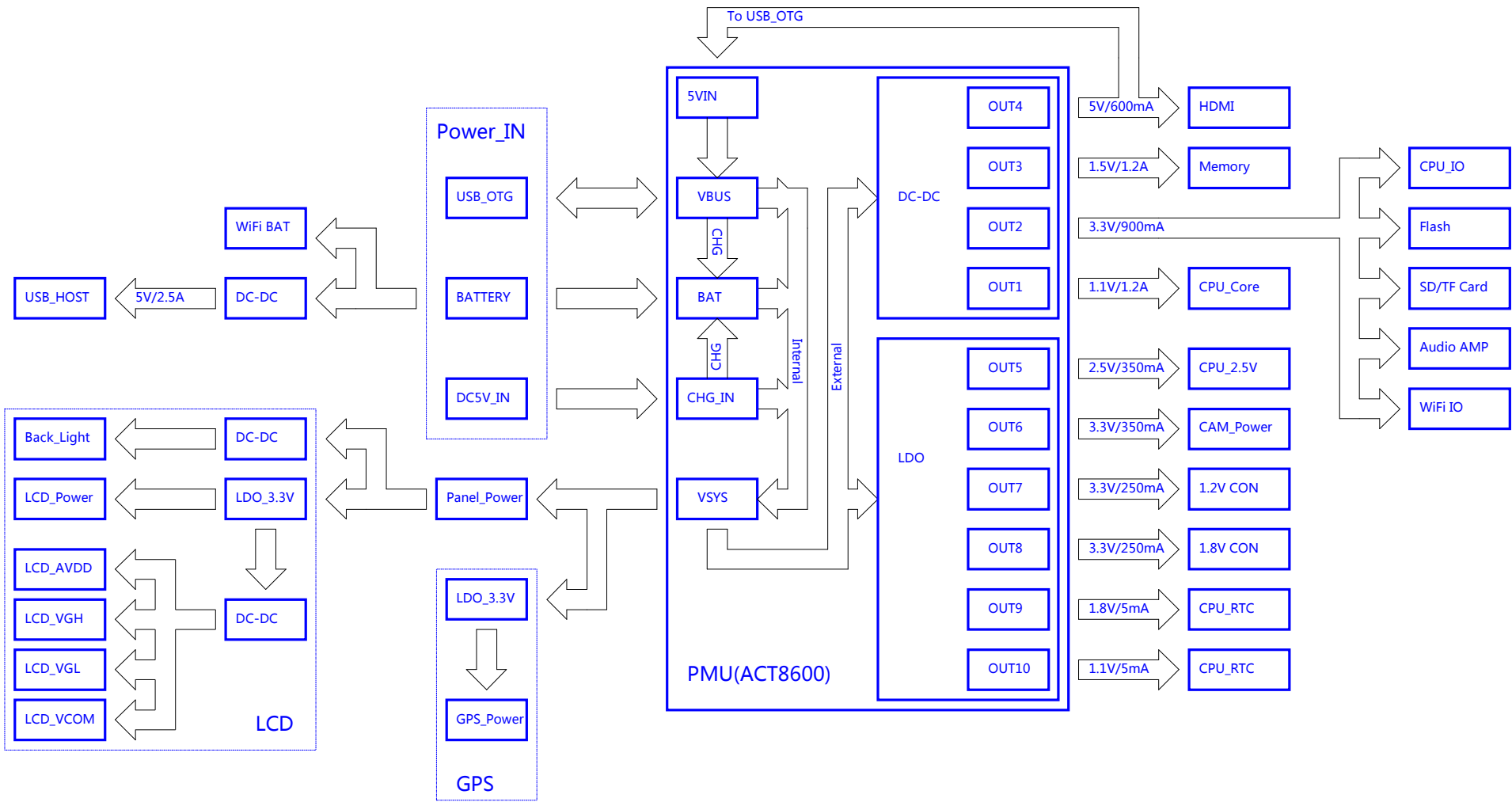
## Schematic Revision 1.1.5

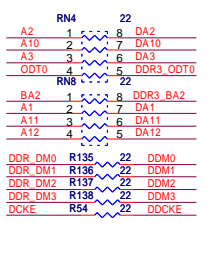
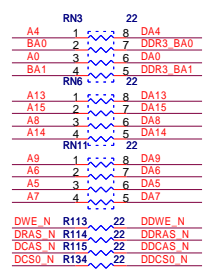
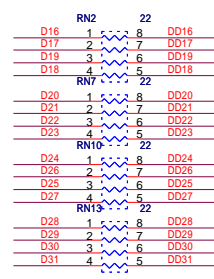
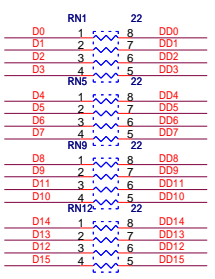
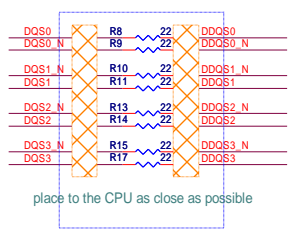
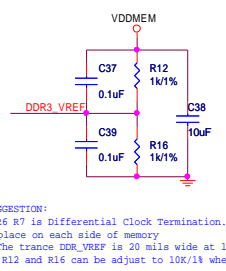
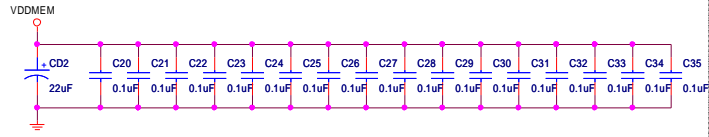
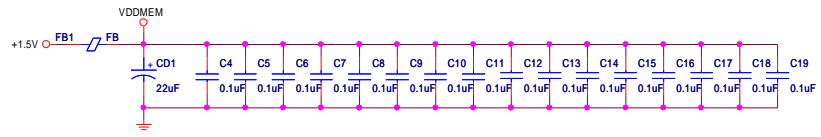
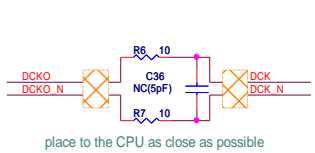
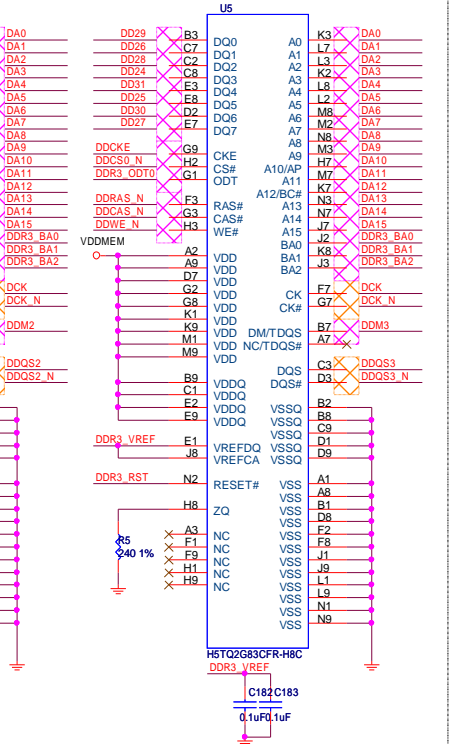
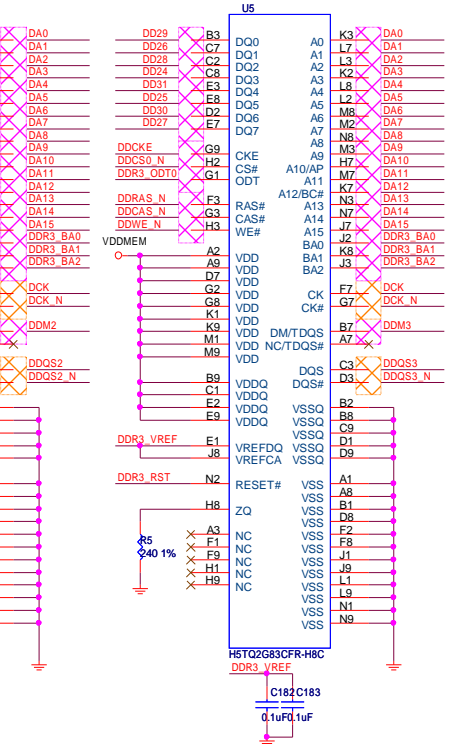
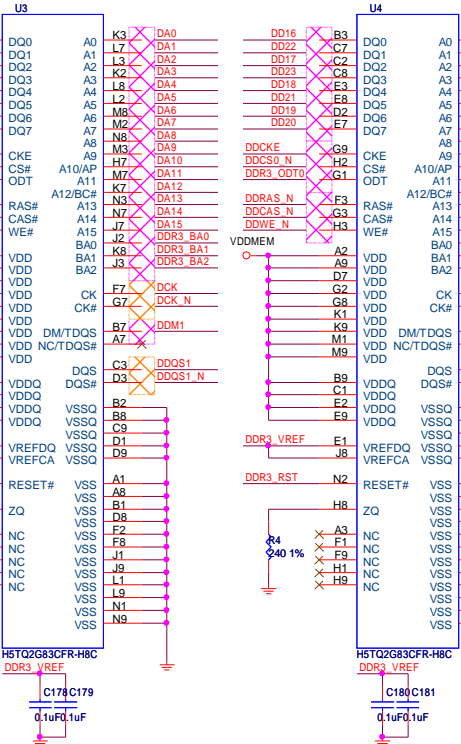
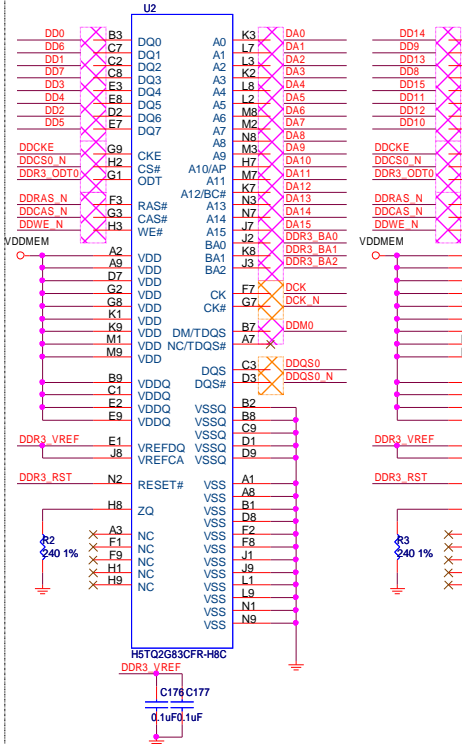
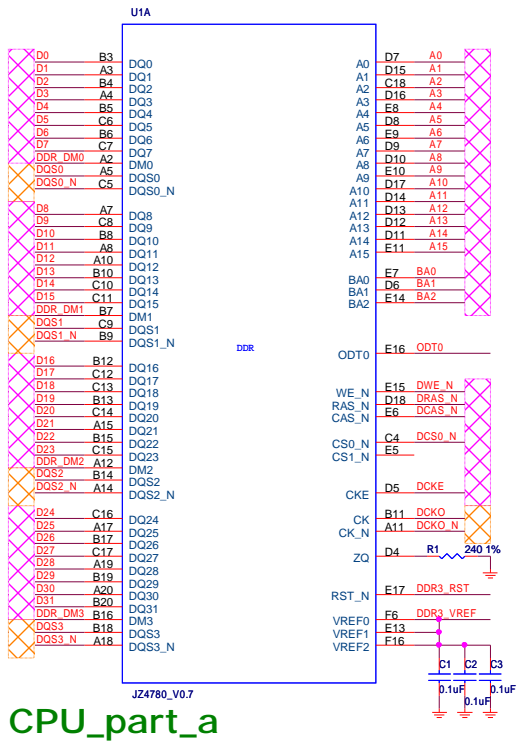
Title	Page
COVER SHEET	1
SYSTEM ARCHITECTURE	2
POWER ARCHITECTURE	3
DDR3	4
Nand/Camera	5
BOOT/AUDIO/HDMI	6
POWER/PMU	7
MMC/LCD/LVDS	8
CPU POWER/RESET/SYS CLK/KEY	9
TS/ETH/UART/GPS/JTAG/USB_CON	10
USB OTG/PS2/DITIGAL MIC	11
REVISION HISTORY	12



The green color is the debug board

<b>INGENIC SEMICONDUCTOR CO.,LTD</b>			
Title		RD4780_GRUS	
Size	Document Number	Rev	
A3	SYSTEM ARCHITECTURE	1.1.5	
Date:	Friday, February 21, 2014	Sheet	2 of 12

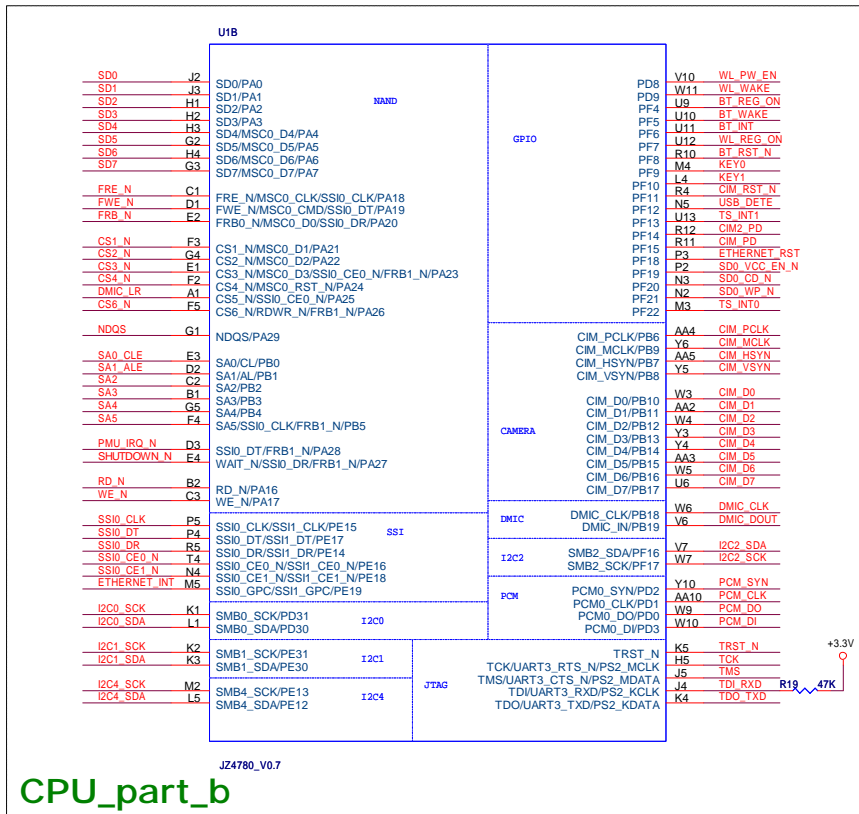




Differential pairs Z0= 100 ohm Equiling BUS Z0= 50 ohm

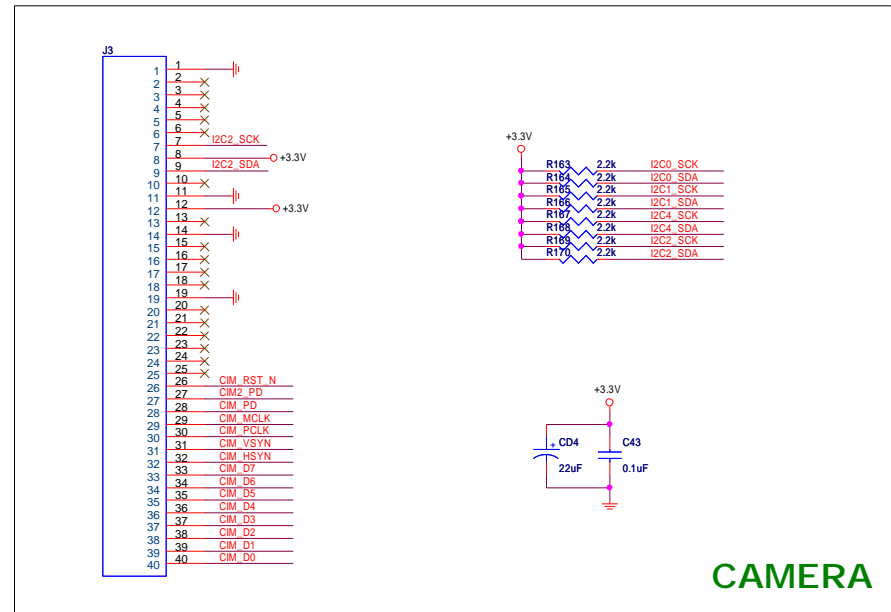
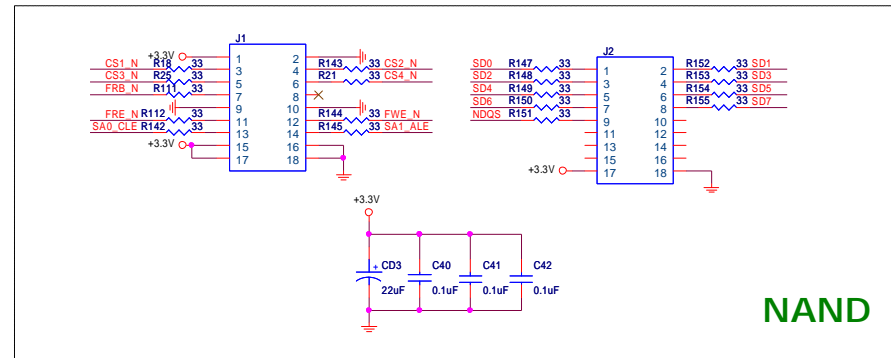
**DDR3**

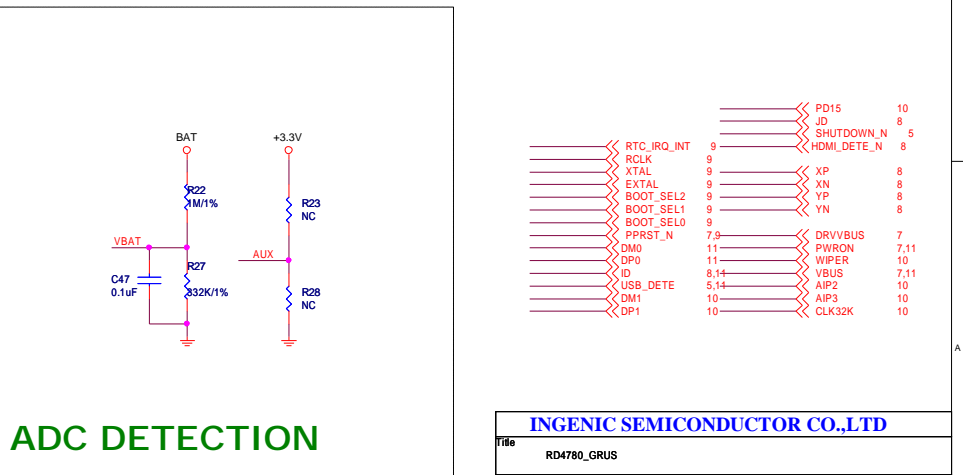
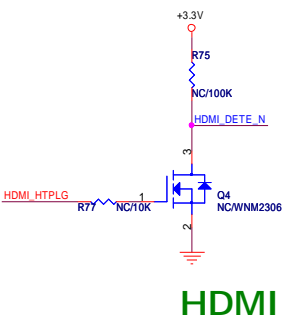
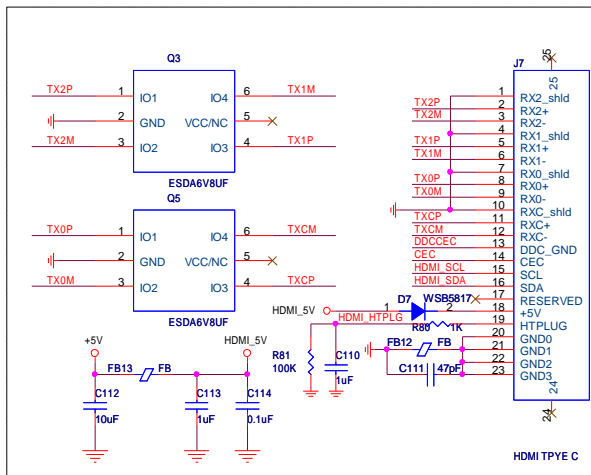
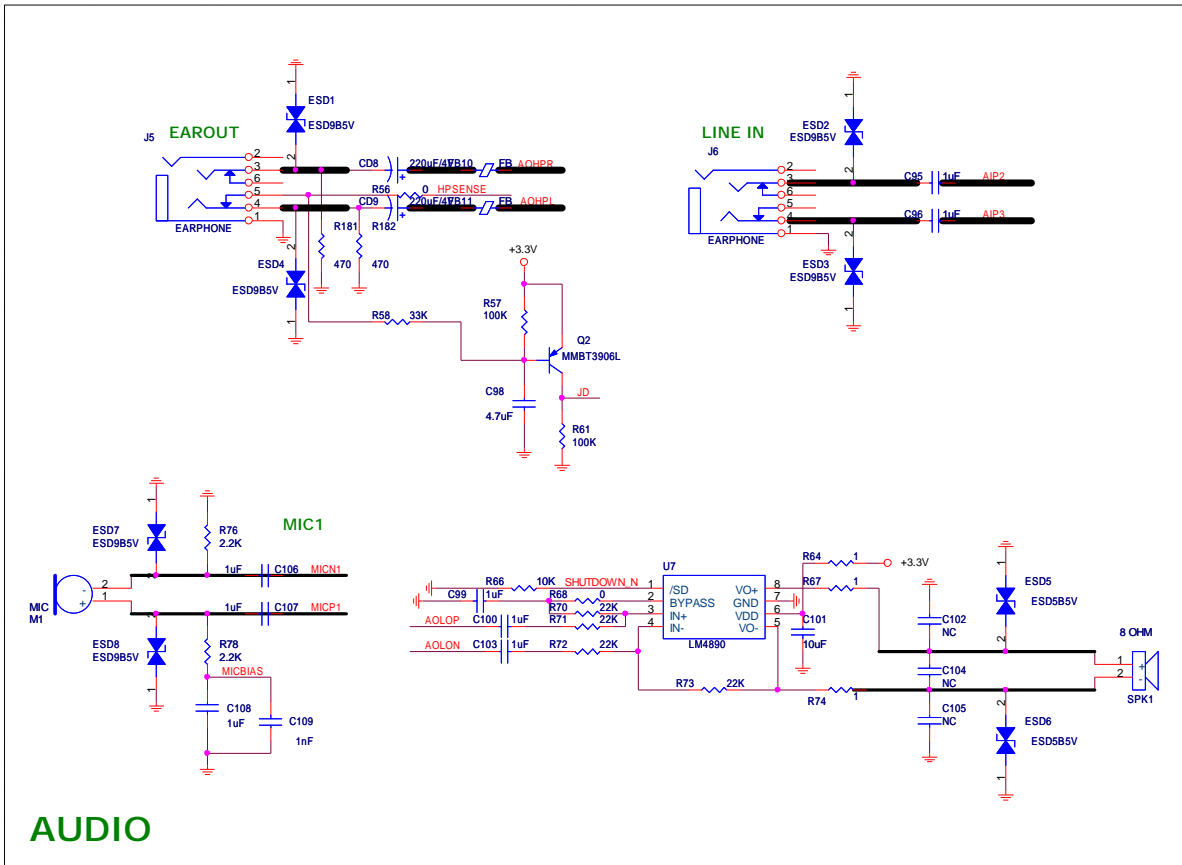
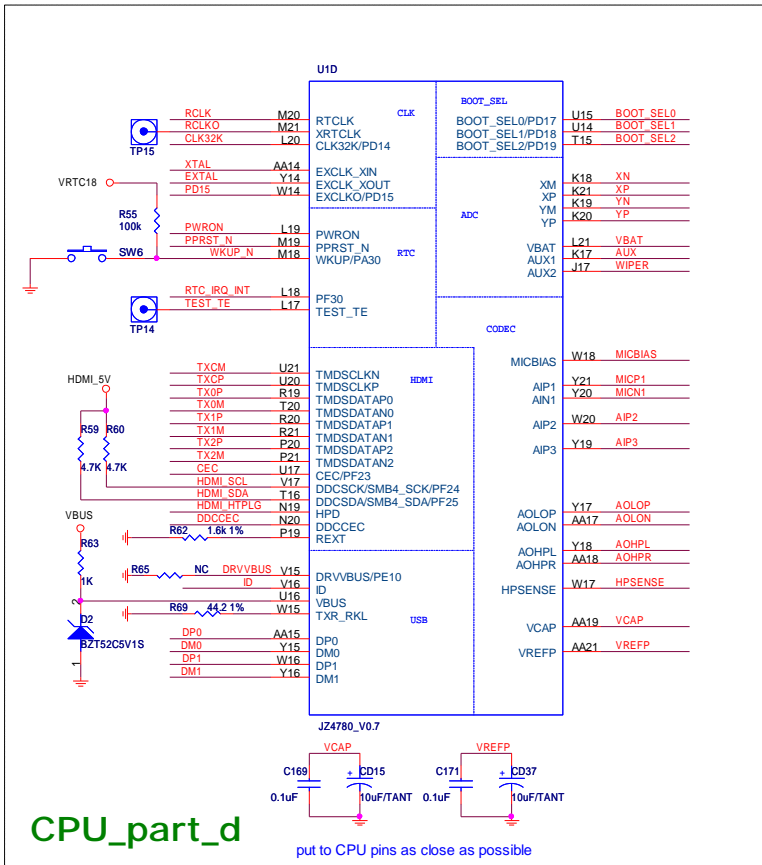
<b>INGENIC SEMICONDUCTOR CO.,LTD</b>		
Title	RD4780_GRUS	
Size	Document Number	Rev
A3	DDR3	1.1.5
Date:	Friday, February 21, 2014	Sheet 4 of 12



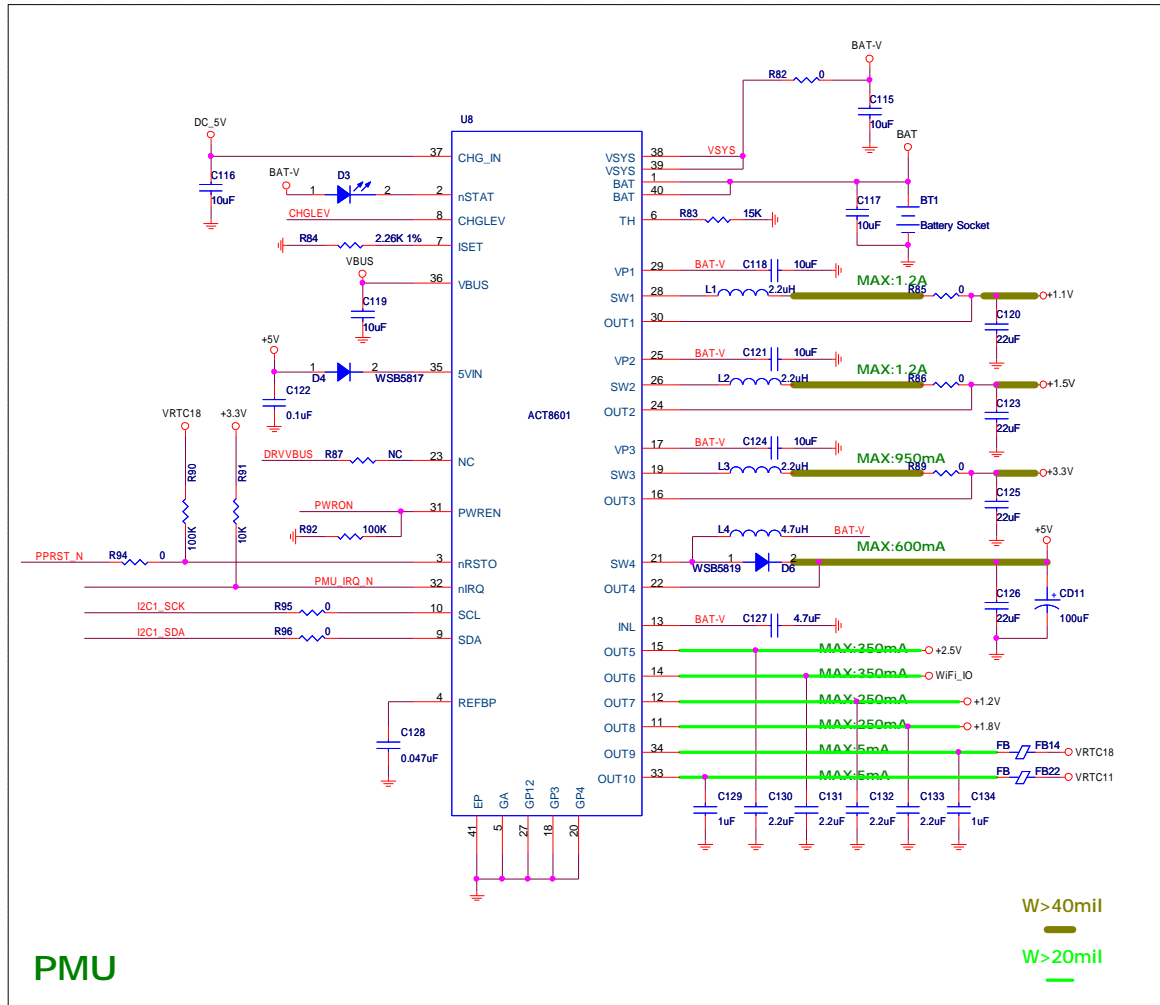
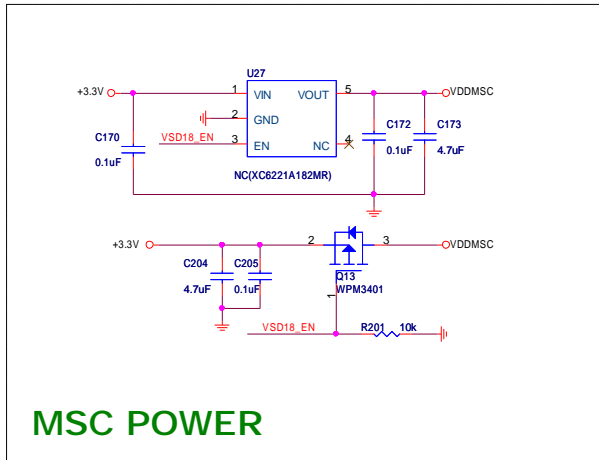
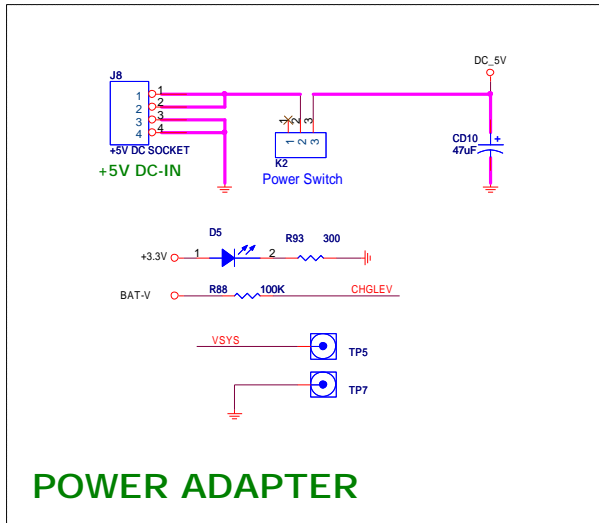
CPU\_part\_b

BT_RST_N	10	USB_DET	11	SA0_CLE	10
WL_REG_ON	10	PMU_IRQ_N	7	SA1_ALE	10
BT_INT	10	KEY0	9	SA2	10
WL_PW_EN	10	KEY1	9	SA3	10
WL_WAKE	10	TS_INT0	10	SA4	10
BT_REG_ON	10	TS_INT1	10	SA5	10
BT_WAKE	10			ETHERNET_INT	10
PCM_CLK	10	I2C0_SCK	8	ETHERNET_RST	10
PCM_SYN	10	I2C0_SDA	8	RD_N	10
PCM_DI	10	I2C1_SCK	7	WE_N	10
PCM_DO	10	I2C1_SDA	7	CS6_N	10
TDO_TXD	10	I2C2_SCK	10	SD0[7]	10
TRST_N	10	I2C2_SDA	10	SD0_CD_N	8
TCK	10	I2C4_SCK	9,10	SD0_WP_N	8
TMS	10	I2C4_SDA	9,10	SD0_VCC_EN_N	8
TDI_RXD	10	SSIO_CE1_N	10		
		SSIO_CLK	10	DMIC_CLK	11
		SSIO_DT	10	DMIC_DOUT	11
		SSIO_DR	10	DMIC_LR	11
		SSIO_CE0_N	10	SHUTDOWN_N	6





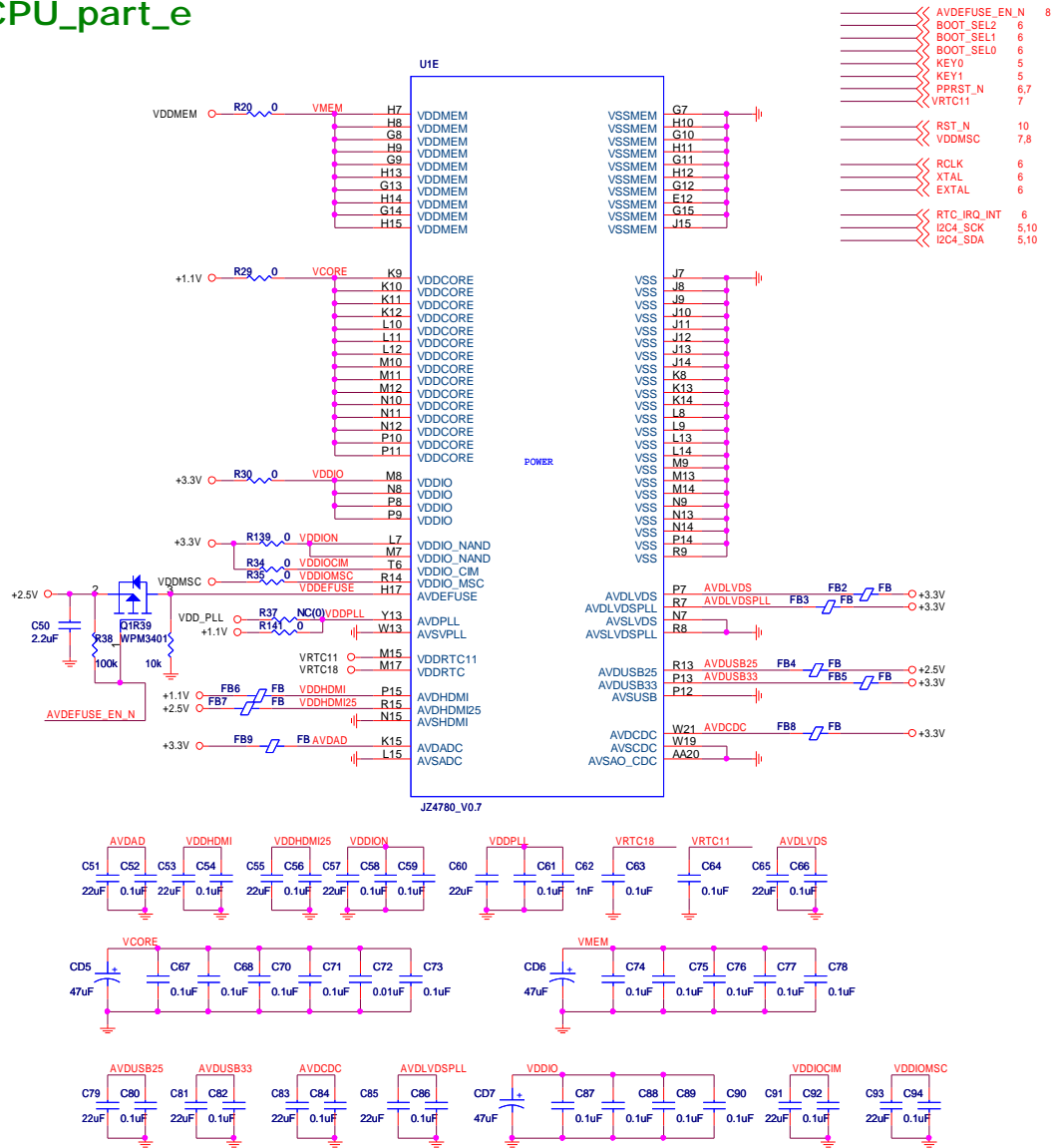
INGENIC SEMICONDUCTOR CO.,LTD		
Title	RD4780_GRUS	
Size	Document Number	Rev
A3	BOOT/AUDIO/HDMI	1.1.5
Date:	Friday, February 21, 2014	Sheet 6 of 12



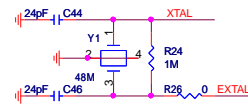




# CPU\_part\_e



## MAIN CLOCK

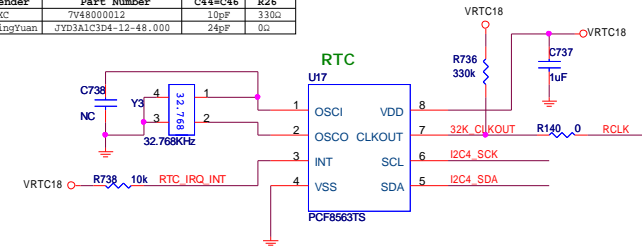


### Y1 selection list

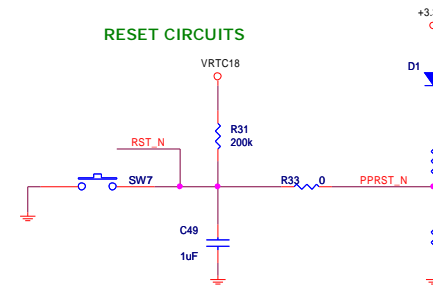
Vendor	Part Number	C44=C46	R26
TXC	7V48000012	10pF	330Ω
JingYuan	JYD3ALC3D4-12-48.000	24pF	0Ω

## Boot Mode Select

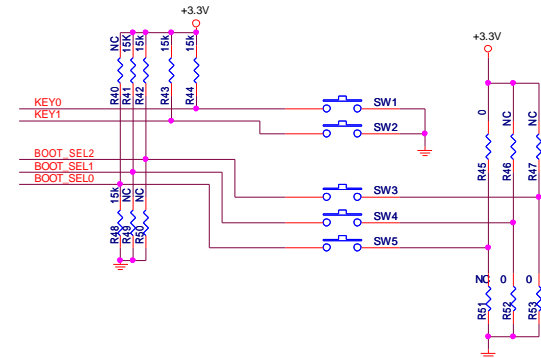
BOOT_SEL[2:1:0]	
111	USB Boot
110	NAND Boot
101	MSC0 Boot
000	SPI Boot
100	MSC1 Boot
011	eMMC Boot
010	NOR Boot(CS2)



## RESET CIRCUITS



## FUNCTION KEY

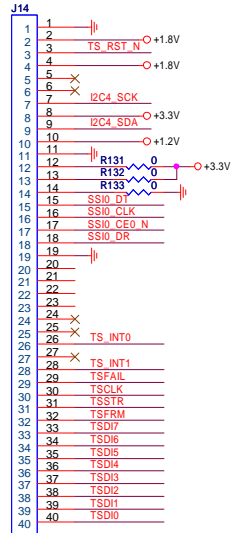


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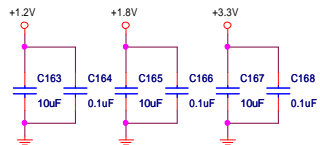
Title	RD4780_GRUS	
Size	Document Number	Rev
A3	CPU POWER/RESET/SYS CLKKEY	1.1.5
Date:	Friday, February 21, 2014	Sheet 9 of 12

WL_REG_ON	5
BT_INT	5
WL_PW_EN	5
WL_WAKE	5
BT_REG_ON	5
BT_WAKE	5
TDO_TXD	5
TRST_N	5
TCK	5
TMS	5
TDI_RXD	5
RD_N	5
WE_N	5
CS6_N	5
SDIO[7]	5
ETHERNET_INT	5
ETHERNET_RST	5
CS6_N	5
DM1	6
DP1	6
PCM_CLK	5
PCM_SYN	5
PCM_DI	5
PCM_DO	5
AIP2	6
AIP3	6
BT_RST_N	5
RST_N	9
GPS_PWR_EN	8
GPS_OSC_EN	8
GPS_RX_EN	8
GPS_CLK	8
GPS_MAG	8
GPS_SIG	8
MSC1_D[0:3]	8
MSC1_CLK	8
MSC1_CMD	8
PMU_IRQ_N	5,7
CSE_N	5
UART1_TXD	8
UART1_RXD	8
UART1_CTS_N	8
UART1_RTS_N	8
SSIO_CE0_N	5
SSIO_CE1_N	5
SSIO_CLK	5
SSIO_DT	5
SSIO_DR	5
TS_RST_N	8
PD15	6
TS_INT0	5
TS_INT1	8
TSFAIL	8
TSFRM	8
TSCLK	8
TSSTR	8
TSD[0:7]	8
WIPER	6
I2C4_SCK	5,9
I2C4_SDA	5,9
I2C2_SCK	5
I2C2_SDA	5
I2C1_SCK	5,7
I2C1_SDA	5,7
SA0_CLE	5
SA1_ALE	5
SA2	5
SA3	5
SA4	5
SA5	5
CLK32K	6

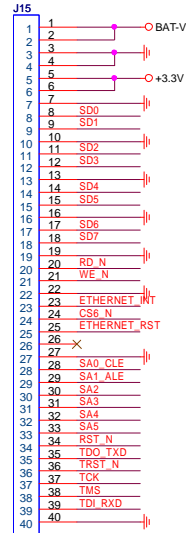
### TS Interface Connector



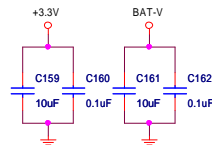
### TS INTERFACE



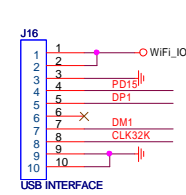
### Ethernet & JTAG Interface



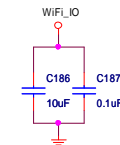
### Ethernet & JTAG



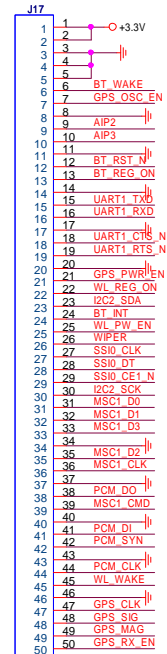
### USB Interface



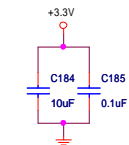
### USB INTERFACE



### WiFi & GPS Interface



### WiFi&GPS



## INGENIC SEMICONDUCTOR CO.,LTD

Title	RD4780_GRUS	
Size	Document Number	Rev
A3	TS/ETH/UART/GPS/JTAG/USB_CON	1.1.5
Date:	Friday, February 21, 2014	Sheet 10 of 12



**Data      Revision      Change**

Aug 28 2012	Rev1.0	1. First Revision
Dec 29 2012	Rev1.0.2	<ol style="list-style-type: none"> <li>1. PAGE05: Delete R18 and connect SHUTDOWN_N to CPU PIN E4.</li> <li>2. PAGE06: Change the footprint of Audio connector J5 &amp; J6</li> <li>3. PAGE06: Change the footprint of D2.</li> <li>4. PAGE07: Change OUT2 to 1.5V and OUT3 to 3.3V. Change the OUT1,OUT2,OUT3 net to the back of resistors.</li> <li>5. PAGE07: Change MSC power chip U27 to XC6221A182MR and NC</li> <li>6. PAGE08: Change the schematic and PCB package of J11.</li> <li>7. PAGE09: Change R736 from 10K to 330K to reduce hibernate current.</li> <li>8. PAGE09: Change R31 from 10K to 200K, R36 from 100K to 1M, C49 from 0805 4.7uF to 0603 1uF, in order to reduce hibernate current.</li> </ol>
Jan 22 2013	Rev1.0.3	1. PAGE06, PAGE07, PAGE09: Change the net VRTC33 to VRTC18 .
Feb 18 2013	Rev1.1	<ol style="list-style-type: none"> <li>1. PAGE08: Change MMC power switch for boot.</li> <li>2. Change the JZ4780 schematic package to V0.6.</li> <li>3. PAGE11: Add LDO power supply for PLL 1.3V and delete VDDIO external power.</li> <li>4. PAGE5: Add 33ohm resistance on nand bus.</li> <li>5. PAGE8: Adjust pullup resistance on VDDMSC0.</li> </ol>
Nov 04 2013	Rev1.1.5	<ol style="list-style-type: none"> <li>1. PAGE06: Delete R79 and add D7.</li> <li>2. PAGE06: Change the connection of DDCCEC from J7's PIN17 to PIN13.</li> <li>3. PAGE06: Change Q4 to WNM2306 and NC.</li> <li>4. PAGE09: Add Y1 selection list.</li> <li>5. PAGE11: Change the power supply of U9 from 1.8V to 3.3V.</li> <li>6. PAGE08 &amp; PAGE10: Delete the net Ethernet_CMD.</li> <li>7. PAGE07: Change the name of U8 from ACT8600 to ACT8601.</li> <li>8. Change the JZ4780 schematic package to V0.7, change some pins' names.</li> </ol>