INNOVATIVE SEMICONDUCTORS, INC.

PRELIMINARY PRODUCT INFORMATION

ISI-200
USB 2.0 PHY Macro-cell

Overview

The ISI-200 is a Mixed-signal Core that includes both the Digital and Analog blocks of the USB Transceiver Macro-cell (UTMI) Specifications. This Core is a mature product that was originally certified in Q1 2002 and the same technology has been used in our Host and On The Go (OTG) Transceivers.

Status

The design has been mapped into numerous process technologies including TSMC .25u , .18u, .15u and .13u. It has also been mapped to Freescale, LSI, NSC and other processes. We can provide design services to port the design into other processes. The design has been implemented as an ASIC library Component as well as an SOC block. The design has been verified in silicon, certified for compliance and in volume production (More than 10 million chips). It is capable of transmitting and receiving at high, full and low speeds.

Functional Blocks

The ISI-200 complies with UTMI+ specifications and consists of the following blocks: The Analog Front End (AFE), the Clock and Data Recovery (CDR), the Bit Stuffer, the Bit un-stuffer, the NRZ encoder and the NRZ Decoder. The AFE consists of the High Speed Transceiver, Full Speed Transceiver, Squelch, Oscillator, PLL, On chip resistors, VBUS sense and Short Circuit protection. A US patent was issued for our novel implementation of the termination resistor.

Ports

USB, System, Control, Data Transmit Interface and Data Receive Interface.

Innovative Partners Program

Innovative has established a network of premier design Service Partners to quickly port our reference design to new process technology. We also work with companies that offer USB Controllers to verify interoperability with our Transceiver.

Deliverables

- GDSII Layout data base.
- LEF of pin sizes and locations
- Encrypted Verilog code
- Synthesis Timing Model
- Documentation including Design Manual and Testability.

Testability

- The Design Support all the UTMI test modes.
- Four additional test modes:
  - ✓ No Test
  - ✓ No Frequency Check
  - ✓ Test at lower frequency
  - ✓ Scan Mode
- Receive Snoop test
- Special Analog Test Modes
- Loop Back Test Supported

USB Product Line

- ISI-75: USB full-speed Transceiver
- ISI-88: USB OTG full-speed Transceiver
- ISI-200: Device USB 2.0 high-speed Transceiver Macro-cell (UTMI)
- ISI-205: Host USB 2.0 high-speed Transceiver Macro-cell
- ISI-210: OTG USB 2.0 high-speed Transceiver Macro-cell (UTMI+)

Key Features

- *Digital CMOS Process Technology.*
- *On Chip Oscillator, Termination Resistors And DP/DM Short Circuit Protection.*
- *Low Pin Count*
- *Minimum number of External Components.*
- *Low Power and Small Area*
- *Supports Bus powered devices.*
- *In addition to USB 2.0 Test modes, supports special test modes.*
- *Supports High Speed 480 Mb/s, 12Mb/s full speed and 1.5Mb/s low speed operation.*
- *UTMI Compliant*
- *Design was mapped into different process technologies.*
- *Design was certified for Compliance.*

HI-SPEED CERTIFIED USB

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