INNOVATIVE SEMICONDUCTORS, INC.

PRELIMINARY PRODUCT INFORMATION

ISI-220
BIST USB PHY Core

BIST for Mixed-signal USB PHY

The USB PHY is a Mixed-signal Core that includes both the Digital and Analog blocks of the USB Transceiver Macro-cell (UTMI/ UTMI+) Specifications.

Testing of the digital section of the PHY is usually accomplished using well known techniques suitable for the intended test purpose. Scan insertion, for example, is used during manufacturing test to detect defects. The IDDQ test is also used for that purpose. Testing of the analog portion is more difficult if it were to achieve comparable circuit coverage.

Built-In-Self-Test (BIST) is usually used to make faster, less-expensive manufacturing tests. Logic BIST is extensively used. Although it was once reserved for complex digital chips, it can now be used for mixed-signal IPs.

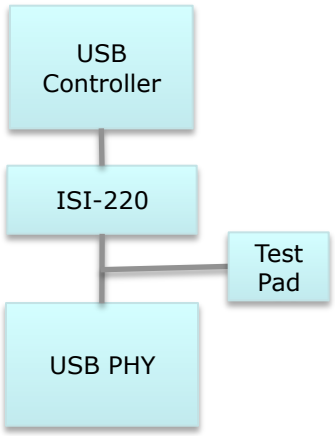
The ISI-220 is a BIST IP used in testing the USB PHY which is a mixed-signal block. It supports low/full/high speed. This is especially helpful in detecting defects in the analog section of the PHY. It is required that the PHY-under-test supports loop-back.

Advantages of the BIST approach

• Faster less expensive manufacturing test
• Low number of pins required
• Small area overhead
• Less intrusive to the design flow

ISI-220 Functional Blocks

The ISI-220 uses a pattern generator implemented with 16-bit linear feedback shift registers (LFSR).



This type of pattern generator can produce pseudorandom patterns of width n, with 2^{n-1} unique combinations before repeating (every possible combination except all zeros).

The pattern is completely deterministic when the initial conditions are known. The ISI-220 configures the USB PHY in the loopback mode. It then transmits the data generated by the pseudo random pattern generator and checks to verify that the received data is the same as the transmit data. This test can be used during debug, characterization or manufacturing.

Deliverables

•RTL Verilog of the ISI-220
•Verilog Test Bench
•Design Manual

Key Features

- *Synthesizable RTL core in Verilog*
- *Bolts into the UTMI/ UTMI+ interface*
- *Less intrusive to the design flow*
- *Minimal impact on timing*
- *Small area*
- *Low number of additional pins required*
- *Supports low/full/high speeds*

Related Products

• ISI-200 USB Device PHY
• ISI-205 USB Host PHY
• ISI-210 USB OTG PHY

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