3GBit/s APIX2 Receiver for Camera Applications

INAP378RAQ

The INAP378RAQ together with the INAP378TAQ transmitter offers a high speed digital serial link for camera applications. It provides a DC-balanced, AC coupled low latency, point-to-point link over shielded twisted pair (STP) copper cables. Its scalable physical layer provides bandwidth of up to 3 GBit/s at lowest EMI. The INAP378RAQ offers a flexible video interface for parallel video or LVDS. Software adjustable driver characteristics, selectable interfaces and configurable operating modes allow maximum transmission distances of up to 25m at 1.5GBit/s. In addition to the video transmission the INAP378RAQ provides completely independent Full Duplex Communication channels. Using the internal AShell protocol, data transfers such as camera control information are protected by error detection and retransmission mechanisms.

The INAP378RAQ offers various interfaces to drive an image sensor. Besides the capability of sending I²C jobs over the internal AShell, the link is optimized to carry low latency GPIO signals for reset or synchronization purposes. With the support of remote configuration through APIX, the status and configuration of the INAP378TAQ as well as the image sensor are under full control of the receiver unit.

Various data integrity features like CRC on video data, monitoring of contol signals or spike suppression mechanisms support the implementation of applications with functional safety requirements (ASIL).

Highly optimized for size and performance, the device is offered in a small aQFN package, tested according to the AEC-Q100 automotive qualification standards.

Applications:

- Round View Camera Systems
- Rear View Camera Systems
- Sensor Fusion Systems Automotive Driver Assistance
- Surveillance Systems
- Inspection Systems

Features:

- 500 MBit/s, 1GBit/s, 1.5GBit/s and 3GBit/s downstream link bandwidth for video data rates up to 2591 MBit/s
- 187.5 Mbit/s and 62.5 Mbit/s upstream link bandwidth
- Configurable Video Interface
  - Parallel Video (10,12,18 bit)
  - openLDI compliant LVDS interface
    - Single Channel (18, 24 bit)
- AShell protected, full duplex data communication
- SPI data interface
- I²C Master interface
- GPIOs for direct signalling and camera synchronization support
- I²S Audio Interface
  - supports 16/24/32 Bit word length
  - supports 44.1 kHz / 48 / 96 kHz sampling
  - TDM support for up to 8 channels
  - highly precise clock generator
- Diagnostic Features:
- Up to 25m distance at 1.5GBit/s

Package:

- 104 pin aQFN package

Temperature/Quality:

- -40°C to +85°C
- AEC-Q100

1.0 Block Diagram

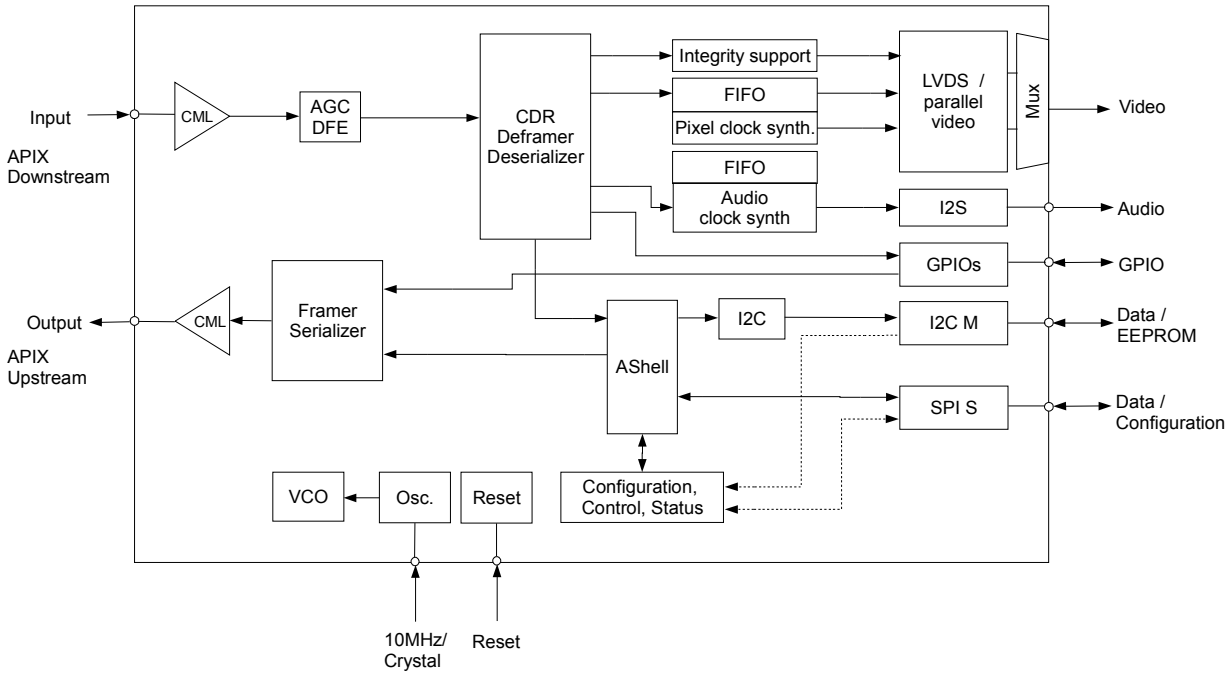


Figure 1-1: Block Diagram

2.0 Electrical Characteristics

All values in this section shall be seen as design target or estimations. Final values will be available after product characterization.

2.1 Absolute Maximum Ratings

The absolute maximum ratings define values beyond which damage to the device may occur. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The functional operation of the device at these or any other conditions beyond the recommended operating ratings is not guaranteed.

Parameter	Description	Min.	Max.	Units	Note
V_{DVDD}, V_{DVDD_XTAL}	DC Supply Voltage	-0.5	5.0	V	
V_{VDD}, V_{AVDD}, V_{AVDD_LVDS}, V_{VDD_XTAL}	Input Voltage	-0.5	3.0	V	
I_D	I/O Current (DC or transient any pin)	-20	+20	mA	
T_{stg}	Storage Temperature	-55	+150	° C	
T_{SLD} / T_{SLD}	Max Soldering Temperature		260	° C	40 seconds maximum
-	ESD Protection HBM JEDEC JESD22/A114	-3	+3	kV	R_D=1.5kΩ, C_S=100pF
-	ESD Protection CDM EIA/JEDEC JESD22/C101	-1	+1	kV	
-	ESD Protection MM EIA/JEDEC JESD22-A115A	-200	+200	V	

Table 2-1: Absolute maximum ratings

2.2 Recommended Operating Conditions

Parameter	Description	Min.	Typ.	Max.	Units	Note
V_{VDD}, V_{VDD_XTAL}	Digital Core supply, Oscillator supply	1.71	1.8	1.89	V	
V_{DVDD}, V_{DVDD_XTAL}	Digital IO Supply, Digital Oscillator supply	3.0	3.3	3.6	V	
V_{AVDD}, V_{AVDD_VCO}	CML PHY supply voltage, VCO supply	1.71	1.8	1.89	V	
$V_{AVDD\_LVDS\_PLL}$, V_{AVDD_LVDS}	LVDS PLL & Core supply	1.71	1.8	1.89	V	
T_a	Ambient Temperature	-40	-	+105	° C	

Table 2-2: Recommended operating conditions

2.3 Electrical Characteristics

2.3.1 Serial Interface

2.3.1.1 Downstream interfaces

The downstream input interface expects serial data coming from an APIX transmitter device.

Parameter	Description	Min.	Typ.	Max.	Unit
V_{diff_in}	Differential input voltage range	tbd.	-	+/-500	mV
V_{cmm_SDIN}	Serial input common mode range	V_{AVDD} - 0.5V + (V_{diff_in}/2)	-	V_{AVDD} + 0.5V - (V_{diff_in}/2)	V
$J_{acceptance}$	Random Jitter acceptance	-	-	tbd.	mUI

Table 2-3: Downstream input interface characteristics (SD_DWN_IN_P, SD_DWN_IN_N)

2.3.1.2 Upstream interfaces

The upstream output interface transmits serial data to a connected APIX transmitter device.

Parameter	Description	Min.	Typ.	Max.	Unit
$I_{out\_nom\_up}$	Drive Current	1	-	4	mA

Table 2-4: Upstream output interface characteristics (SD_UP_OUT_P, SD_UP_OUT_N)

2.3.2 Supply Current

Parameter	Description	Comments	Typ.	Max.	Unit
I_{VDD} + I_{VDD_XTAL}	Digital Core & Oscillator Supply Current		75	120	mA
I_{DVDD} + I_{DVDD_XTAL}	Digital IO & Oscillator Supply Current		60	120	mA
I_{AVDD_LVDS} + $I_{AVDD\_LVDS\_PLL}$	LVDS Core & PLL Supply Current		-	30	mA
I_{AVDD}	CML PHY Supply Current		130	210	mA
I_{AVDD_VCO}	VCO Supply Current		5	15	mA

Table 2-5: Supply current

2.3.3 Pixel Interface

The INAP378RAQ's pixel interface can be configured to RGB or/and LVDS outputs. For further informations please refer to the INAP378RAQ user manual.

2.3.3.1 RGB Interface

Parameter	Description	Test Condition	Min.	Max.	Units
V_{OH}	Output High Voltage	IOH= -4mA	2.4	-	V
V_{OL}	Output Low Voltage	IOL= 4mA	-	0.4	V

Table 2-6: RGB characteristics

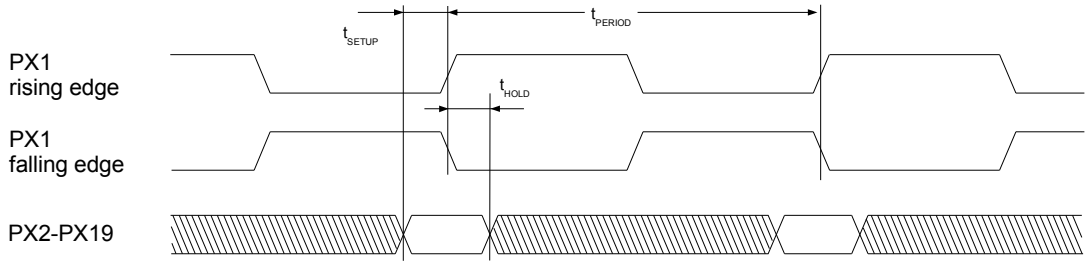


Figure 2-1: RGB Interface Timing

The active edge of pixel clock can be set to rising or falling. For further information please refer to the INAP378RAQ user manual. $f_{PIXEL\_CLOCK} = 1/t_{PERIOD}$. All values specified for T_A=25°C.

Parameter	Description	Test Condition	Min.	Max.	Units
f_{PIXEL_CLOCK}	Pixel Clock Output Frequency		5	120	MHz
t_{SKEW}	Skew Pixel Clock Active Edge To Pixel Data		-2	1	ns

Table 2-7: RGB Interface timing

2.3.3.2 LVDS Interface

LVDS interface according to TIA/EIA644 specification. Exceptions are listed at table 1-10.

Parameter	Description	Min.	Max.	Units
V_{OD}	Differential Output Voltage	247	454	mV
V_{OS}	Offset Voltage	1.125	1.375	V
V_{COD}	|Change to V_{OD}|	-	50	mV
V_{COS}	|Change to V_{Os}|	-	50	mV
I_{SA}	Short Circuit Current	-	24	mA
I_{IN}	Input Current	-	20	µA
V_{TH}	Receiver Threshold Voltage	-	+100	mV
V_{IN}	Input Voltage Range	0	1.8	V
f_{LVDS_CLK}	LVDS Clock Frequency	5	80	MHz

Table 2-8: LVDS interface exceptions to TIA/EIA644 specification

2.3.4 Data Interface

2.3.4.1 General Characteristics

The following characteristics are valid for SPI, GPIO, I²S and I²C functionality. The pins I2C_SCL and I2C_SD are open drain outputs and require external pull up circuitry. All values specified for T_A=25°C.

Parameter	Description	Test Condition	Min.	Max.	Units
V_{IH}	Input High Voltage		2.0	V_{DVDD}	V
V_{IL}	Input Low Voltage		0	0.8	V
I_{IH_PD}	Pull Down Current [a]	Vin = V_{DVDD}	30	120	µA
I_{IH}	Input High Current	Vin = V_{DVDD}	-10	10	µA
I_{IL}	Input Low Current	Vin = 0 V	-10	10	µA
V_{OH}	Output High Voltage [b]	IOH= -3mA, Figure 2-9	2.4	-	V
V_{OL}	Output Low Voltage	IOL= 3mA, Figure 2-9	-	0.4	V
t_{RO}	Output Rise Time [b]	C_L=5pF	-	2.6	ns
t_{FO}	Output Fall Time [b]	C_L=5pF	-	2.1	ns

Table 2-9: General IO Characteristics

a. pins with internal pull down to GND
b. not relevant for open drain outputs

2.3.4.2 SPI Slave Interface timing

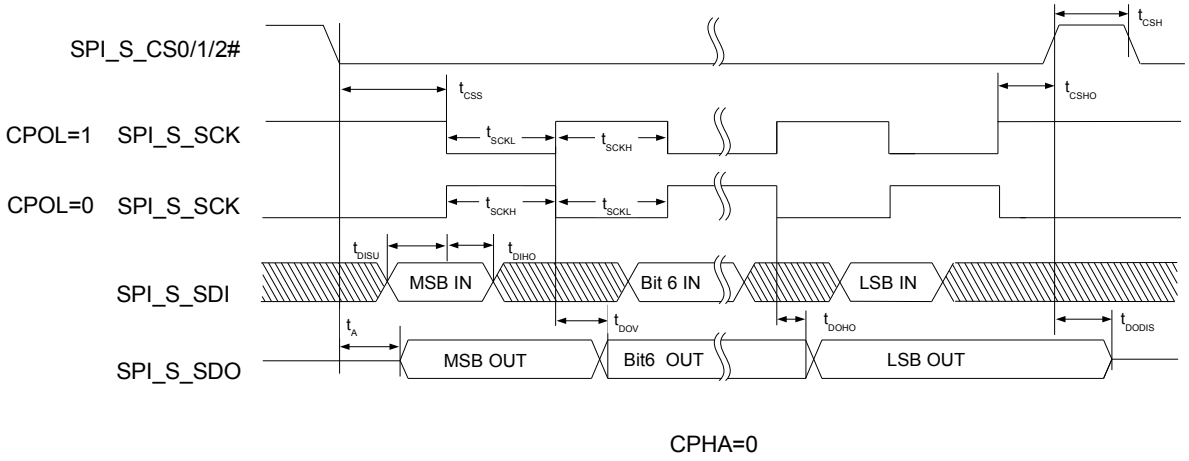


Figure 2-2: SPI Slave Timing Diagram (CPHA=0)

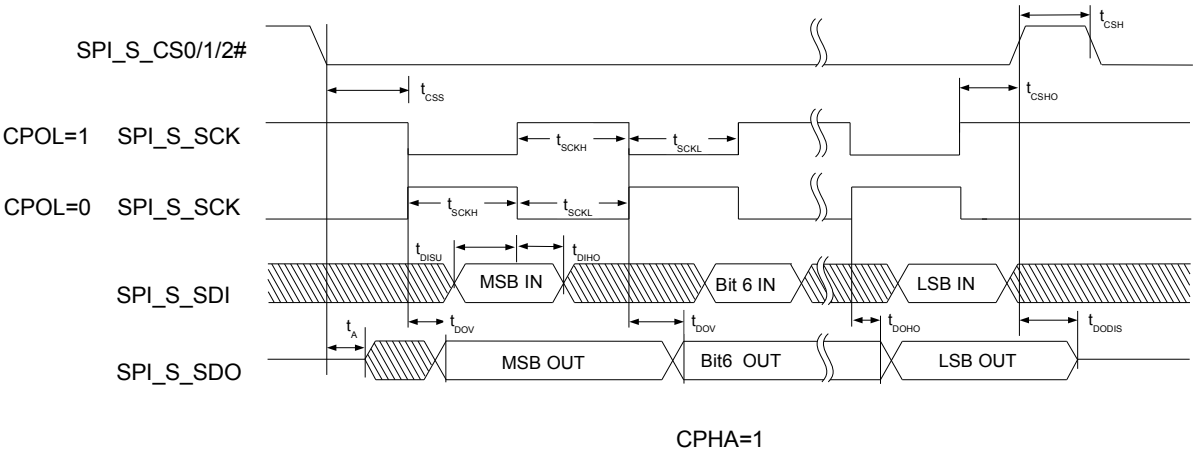


Figure 2-3: SPI Slave Timing Diagram (CPHA=1)

The SPI Slave interface can be flexible configured with the parameters cfg_spi_s_cpol, cfg_spi_s_cpha. For further informations please refer to the INAP378RAQ user manual.

Core clock frequency is 187.5MHz. All values specified for T_A=25°C. $t_{SCK} = 1/f_{SCK}$.

Parameter	Description	Min	Max	Units
f_{SCK}	SCK Clock Frequency	-	15	MHz
t_{SCKH}	SCK High Time	33	-	ns
t_{SCKL}	SCK Low Time	33	-	ns
t_{CSH}	CS# High Time	15	-	ns
t_{CSS}	CS# Setup Time	1/2 t_{SCK}	-	ns
t_{CSHO}	CS# Hold Time	34	-	ns
t_{DISU}	Data In Setup Time	12	-	ns
t_{DIHO}	Data in Hold Time	12	-	ns
t_{DOV}	Data Output Valid	-	29	ns
t_{DOHO}	Data Output Hold Time	5	-	ns
t_{DODIS}	Data Output Disable Time	-	45	ns
t_A	Data Access Time	15	-	ns

Table 2-10: SPI Slave Interface characteristics (Read Access)

Parameter	Description	Min	Max	Units
f_{SCK}	SCK Clock Frequency	-	41	MHz
t_{SCKH}	SCK High Time	1/2 t_{SCK}	-	ns
t_{SCKL}	SCK Low Time	1/2 t_{SCK}	-	ns
t_{CSH}	CS# High Time	15	-	ns
t_{CSS}	CS# Setup Time	1/2 t_{SCK}	-	ns
t_{CSHO}	CS# Hold Time	34	-	ns
t_{DISU}	Data In Setup Time	12	-	ns
t_{DIHO}	Data In Hold Time	12	-	ns

Table 2-11: SPI Slave Interface characteristics (Write Only Access)

2.3.4.3 I²C Interface timing

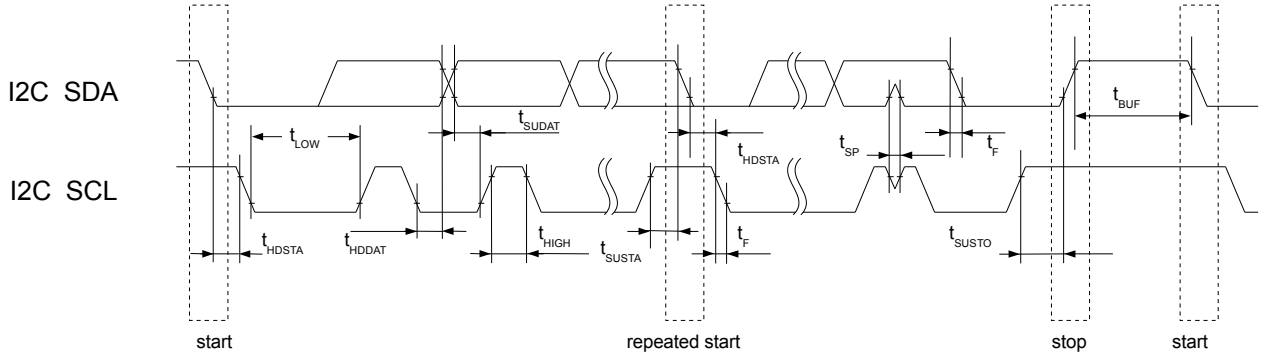


Figure 2-4: I2C Timing Diagram

The I2C timings depend on the accuracy of the external 10MHz reference clock and are therefore listed as typical values. All values specified for T_A=25°C.

Parameter	Description	Min.	Typ.	Max.	Units
f_{SCL}	SCL Clock Frequency Standard Mode Fast Mode	-	-	 100 400	kHz
t_{HIGH}	SCL High Time Standard Mode Fast Mode	-	 4.03 1.08	-	µs
t_{LOW}	SCL Low Time Standard Mode Fast Mode	-	 6.0 1.5	-	µs
t_{HDSTA}	Hold Time (repeated) START conditon Standard Mode Fast Mode	-	 4.0 1.0	-	µs
t_{HDDAT}[a]	Data Hold Time Standard Mode Fast Mode	-	 4.0 1.0	-	µs
t_{SUDAT}	Data Setup Time Standard Mode Fast Mode	-	 2.0 0.5	-	µs
t_{SUSTA}	Setup Time for repeated START conditon Standard Mode Fast Mode	-	 6.03 1.58	-	µs

Table 2-12: I2C Interface characteristics

Parameter	Description	Min.	Typ.	Max.	Units
t_{SUSTO}	Setup Time for STOP conditon Standard Mode Fast Mode	-	 4.03 1.08	-	µs
t_{BUF}	Bus Free Time Standard Mode Fast Mode	-	 10.0 2.5	-	µs
t_f	fall time of SDA and SCL Standard Mode Fast Mode[b]	-	-	 300 300	ns
t_{SP}	pulse width of spike supression Standard Mode Fast Mode[c]	-	-	 - 50	ns

Table 2-12: I2C Interface characteristics

a. max. valid time (t_{VD}) non-applicable, since device stretches the LOW period (t_{LOW}) of the SCL signal
b. output buffers without slope control for falling edges, use series resistors to slow down falling egdes if needed
c. valid for SCL signal, no spike supression on SDA signal

2.3.4.4 RESET and Boot Strap timing

The INAP378RAQ offers several boot strap pins to define, how the device will come up and check for a configuration after boot up or hardware reset. The correct boot strap selection is necessary for proper operation of the INAP378RAQ. For more information please refer to the INAP378RAQ user manual.

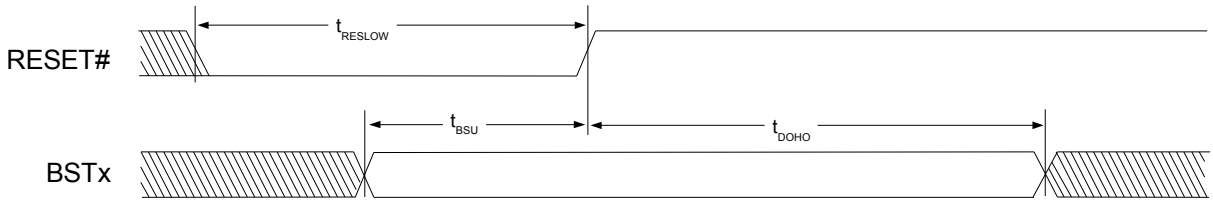


Figure 2-5: Reset and Boot Strap Timing Diagram

For a valid Reset Low Time (t_{RESLOW}) all supply voltages needs to be stable in the operating condition. At reset release (rising edge of RESET#) a stable reference clock is required. All values specified for T_A=25°C.

Parameter	Description	Min.	Typ.	Max.	Units
t_{RESLOW}	Reset Low Time	1	-	-	ms
t_{BSU}	Boot Strap In Setup Time	0	-	-	ns
t_{BHO}	Boot Strap in Hold Time	500	-	-	ns

Table 2-13: Boot Strap Reset Timing

2.3.4.5 I²S Audio Interface

f_{BCK} = 1 / t_{PERIOD}. All values specified for T_A=25°C.

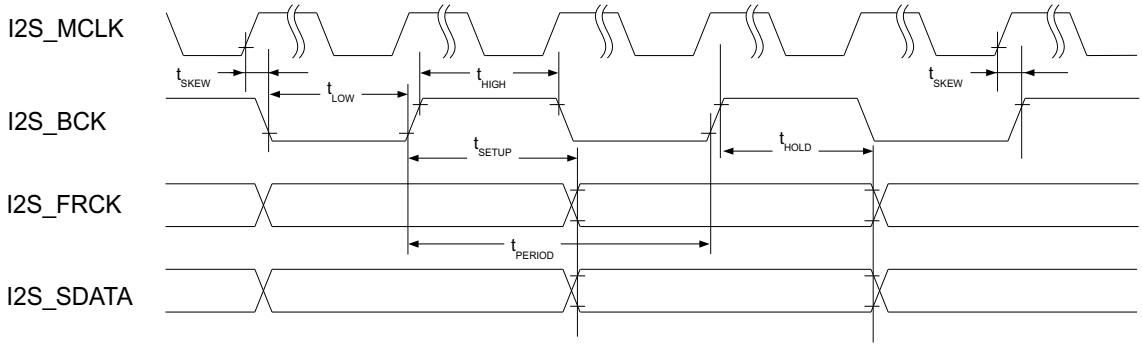


Figure 2-6: I²S Audio Interface Timing Diagram

Parameter	Description	Min	Max	Units
f_{BCK}	I²S_BCK frequency	0.75	26.78	MHz
f_{MCLK}	I²S_MCLK frequency	2.953	93.75	MHz
t_{SKEW}	Skew MCLK to BCK	-	t.b.d.	ns
t_{HIGH}	I²S_BCK high time	t.b.d.	-	ns
t_{LOW}	I²S_BCK low time	t.b.d.	-	ns
t_{SETUP}	Setup time BCK to SDATA	t.b.d.	-	ns
t_{HOLD}	Hold time BCK to SDATA	t.b.d.	-	ns

Table 2-14: I²S Audio Interface Timing

2.3.4.6 MCLK clock output

The granularity of the frequency output of MCLK is definded by pulse width. For further informations please refer to the INAP378RAQ user manual. All values specified for T_A=25°C.

Parameter	Description	Min	Max	Units
f_{MCLK_OUT}	MCLK output frequency	2.953	187.5	MHz

Table 2-15: MCLK output frequency range

2.3.4.7 GPIO Interface

2.3.4.7.1 GPIO Interface Downstream

At transmitter side GPIO data input ports are sampled asynchronously and transmitted to configurable GPIO output ports at receiver side. Sampling frequency can be flexible configured using parameters GPIO Bandwidth (gpio_bw_dwn) and GPIO halved (gpio_bw_div). For further information please refer to the INAP378RAQ user manual. All values specified for T_A=25°C.

Downstream Bandwidth	GPIO ports	GPIO Bandwidth	GPIO halved	Sampling Frequency.	Unit
3 GBit/s	1	high	off	26.768	MHz
3 GBit/s	1	low	off	6.696	MHz
3 GBit/s	1	high	on	13.393	MHz
3 GBit/s	1	low	on	3.348	MHz
3 GBit/s	2	high	off	13.393	MHz
3 GBit/s	2	low	off	3.348	MHz
3 GBit/s	2	high	on	6.696	MHz
3 GBit/s	2	low	on	unsupported	MHz
1.5 GBit/s	1	high	off	26.768	MHz
1.5 GBit/s	1	low	off	6.696	MHz
1.5 GBit/s	1	high	on	13.393	MHz
1.5 GBit/s	1	low	on	3.348	MHz
1.5 GBit/s	2	high	off	13.393	MHz
1.5 GBit/s	2	low	off	3.348	MHz
1.5 GBit/s	2	high	on	6.696	MHz
1.5 GBit/s	2	low	on	unsupported	MHz
1 GBit/s	1	high	off	17.857	MHz
1 GBit/s	1	low	off	4.468	MHz
1 GBit/s	1	high	on	8.929	MHz
1 GBit/s	1	low	on	2.232	MHz
1 GBit/s	2	high	off	8.929	MHz
1 GBit/s	2	low	off	2.232	MHz
1 GBit/s	2	high	on	4.464	MHz
1 GBit/s	2	low	on	1.116	MHz

Table 2-16: GPIO Interface Downstream

Downstream Bandwidth	GPIO ports	GPIO Bandwidth	GPIO halved	Sampling Frequency.	Unit
500 MBit/s	1	high	off	17.857	MHz
500 MBit/s	1	low	off	4.468	MHz
500 MBit/s	1	high	on	8.929	MHz
500 MBit/s	1	low	on	2.232	MHz
500 MBit/s	2	high	off	8.929	MHz
500 MBit/s	2	low	off	2.232	MHz
500 MBit/s	2	high	on	4.464	MHz
500 MBit/s	2	low	on	1.116	MHz

Table 2-16: GPIO Interface Downstream

2.3.4.7.2 GPIO interface upstream

Transmitter GPIO upstream interface outputs GPIO data coming from either one or two APIX2 receiver devices. Output frequency can be configured using parameter GPIO Bandwidth (gpio_bw_up). For further informations please refer to the INAP378RAQ user manual. All values specified for T_A=25°C.

Number of Rx	Upstream Bandwidth	GPIO ports	GPIO Bandwidth	Maximum Output frequency	Unit
1	187.5 MBit/s	1	high	13.39	MHz
1	187.5 MBit/s	1	low	3.35	MHz
1	187.5 MBit/s	2	high	13.39	MHz
1	187.5 MBit/s	2	low	3.35	MHz
1	62.5 MBit/s	1	high	4.46	MHz
1	62.5 MBit/s	1	low	1.12	MHz
1	62.5 MBit/s	2	high	4.46	MHz
1	62.5 MBit/s	2	low	1.12	MHz
2	187.5 MBit/s	1	high	6.69	MHz
2	187.5 MBit/s	1	low	3.35	MHz
2	187.5 MBit/s	2	high	6.96	MHz
2	187.5 MBit/s	2	low	3.35	MHz
2	62.5 MBit/s	1	high	2.23	MHz

Table 2-17: GPIO Interface Upstream

Number of Rx	Upstream Bandwidth	GPIO ports	GPIO Bandwidth	Maximum Output frequency	Unit
2	62.5 MBit/s	1	low	1.12	MHz
2	62.5 MBit/s	2	high	2.23	MHz
2	62.5 MBit/s	2	low	1.12	MHz

Table 2-17: GPIO Interface Upstream

2.3.5 Reference Clock

The INAP378RAQ requires an external clock source like a crystal or oscillator, acting as reference for the internal PLL.

Parameter	Description	Min.	Typ.	Max.	Unit
f_{ref_osc}	Nominal Reference Frequency	-	10	-	MHZ
F_{TOL}	Frequency Tolerance	-100	-	+100	ppm
ESR_{XTAL}	Equivalent Series Resistance	-	-	80	Ohm
	Drive Level	see Table 2-19			

Table 2-18: Reference clock requirements

The INAP378RAQ core clock frequency is generated by an internal PLL controlled by an external 10 MHz crystal. Alternatively a stable 10 MHz clock signal (3.3V CMOS TTL) can be directly connected to XTAL_IN with XTAL_OUT left open. Figure 2-7 shows a typical crystal design required for the oscillator circuit. The values for C1, C2 and R1 need to be selected to match the oscillation requirements of the crystal Q1.

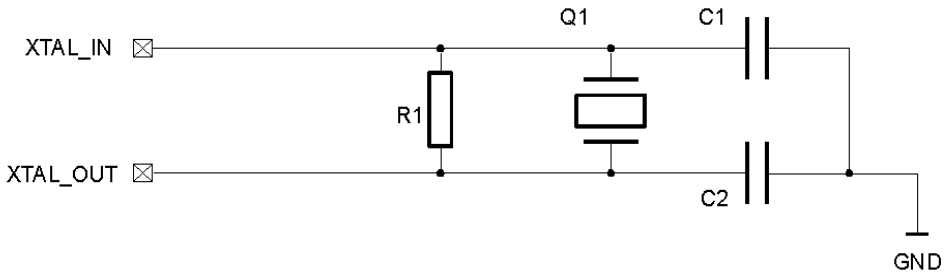


Figure 2-7: Crystal clock schematic example

For resonance at the correct frequency, the crystal needs to be loaded with its specified load capacitance C_L, which is the value of capacitance used in conjunction with the oscillation unit. The INAP378RAQ oscillator provides some of the load with internal capacitance which is specified within the range of 10pF to 12.5pF. The remainder is generated by the external capacitors and tuning capacitors labeled C1 and C2.

The load capacitance CL can be calculated from CL = Cint + C1//C2. E.g. selecting C1 and C2 with 15pF, CL can be calculated to CL = 12.5pF + 7.5pF = 20pF.

The crystal needs to be able to withstand the power dissipation, produced by the INAP378RAQ. The power dissipation depends on the ESR of the crystal and is reflected by the maximum drive level of the crystal. Table 2-19 illustrates the power dissipation of the INAP378RAQ and therefore the minimum drive level capabilities of the crystal at different crystal ESR levels.

Crystal ESR	INAP378RAQ Power dissipation / Minimum crystal drive level	Unit
30	77	µW
50	121	µW
80	179	µW

Table 2-19: Minimum Drive level

2.3.6 Power Up Sequencing

To avoid high IO currents, 1.8V supply voltages have to ramp before 3.3V supply on power-up. On power-down, 3.3V supply have to be powered down before 1.8V. On power-up all supply voltages have to rise steadily from GND level up to the VCC_{MIN} level without turn to negative direction. The ramping times must be within the limits as specified in Table 2-20. All 1.8V supplies have to be ramped up simultaneously starting from GND according Figure 1-13. Reset has to be held low until all supplies reached recommended operating conditions.

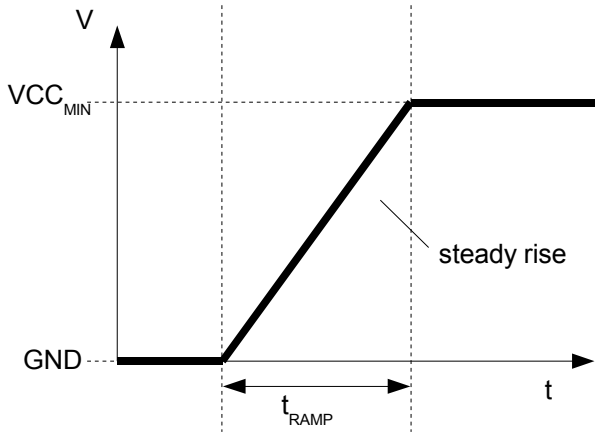


Figure 2-8: Steady voltage ramp-up

The INAP378RAQ tolerates the supplies to be ramped simultaneously. To avoid high IO currents, 1.8V supplies should ramp before 3.3V on power-up. On power-down, 3.3V should be powered down before 1.8V. The ramping times must be within the limits as specified in Table 2-20.

Supply	Ramp-Up time	
	Min	Max
All supplies	50µs	10ms

Table 2-20: Power supply ramping requirements

2.4 Typical operating characteristics

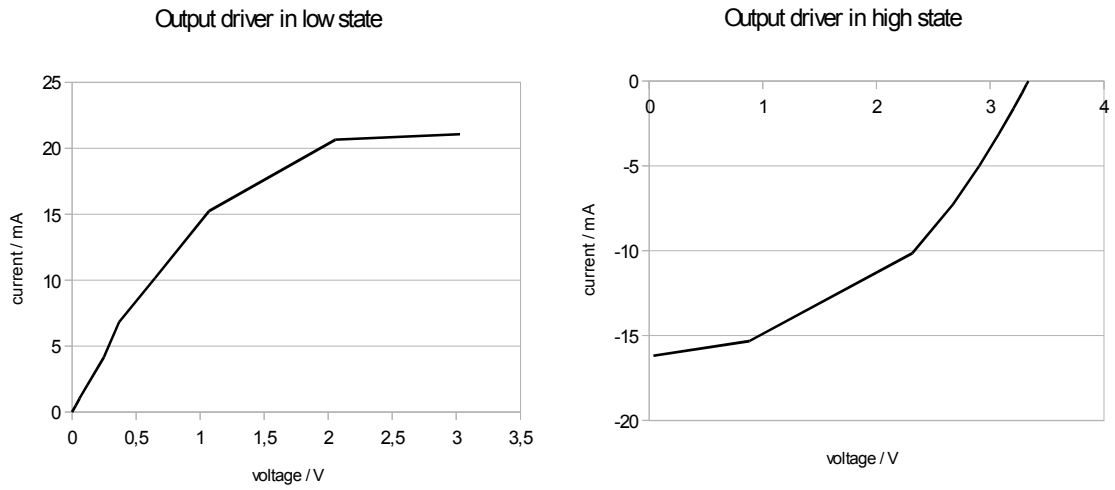


Figure 2-9: Typical device I-V curve for 3.3V data interface IO under nominal condictions

3.0 Pin description

Signal Name	Pin #	Type	Description
PX[19:1]	A2,B3,B4,A4, L2,H3,J1,J3, K2,J2,K1,H1, H2,K4,L3,M2, M3,L4,M5	O	Video Interface pin
BST2	M6	I/O [a]	BST2: Boot strap option 2 input (see Table 3-3)
SPI_S_SDO/ BST3	K8	I/O [a]	SPI_S_SDO: SPI Slave Data Output BST3: Boot strap option 3 input (see Table 3-3)
SPI_S_SDI	M9	I	SPI Slave Data Input
SPI_S_SCK	L9	I	SPI Slave Serial Clock Input
SPI_S_STALL/ BST4	M10	I/O [a]	SPI_S_STALL: High: SPI Slave not ready or buffer full Low: SPI Slave ready to receive data BST4: Boot strap option 4 input (see Table 3-3), only option 1 supported place pull-up of 10KOhm to DVDD (mandatory!)
SPI_S_CS0#	K9	I	SPI_S_CS0#: SPI Slave Chip-select 0 Input (Data channel 0)
SPI_S_CS1#	K10	I	SPI_S_CS1#: SPI Slave Chip-select 1 input (Data channel 1)
SPI_S_CS2#	L11	I	SPI Slave Chip-select 2 input (Configuration)
SPI_S_RW	L12	I	SPI_S_RW: SPI Slave Read/Write input, only used in single SPI mode
SPI_S_MB0/ BST1	K11	I/O	SPI_S_MB0: SPI Slave mailbox 0 output, indicating received data on data channel 0, only used in single SPI mode BST1: Boot strap option 1 input (see Table 3-3)
SPI_S_MB1/ BST6	J10	I/O [a]	SPI_S_MB1: SPI slave mailbox 1 output, indicating received data on data channel 1, only used in single SPI mode BST6: Boot strap option 6 input (see Table 3-3)
I²C_SCL	J11	I/O [b]	I²C_SCL: I²C Clock output
I²C_SD	J12	I/O [b]	I²C_SD: I²C Data pin
SD_DWN_IN_P	E11	I [c]	Serial Link, Downstream Serial Link input from TX
SD_DWN_IN_N	D12	I [c]	Serial Link, Downstream Serial Link input from TX
SD_UP_OUT_N	B12	O [c]	Serial Link, Downstream Serial Link output to TX

Table 3-1: Pin description

Signal Name	Pin #	Type	Description
SD_UP_OUT_P	B11	O [c]	Serial Link, Downstream Serial Link output to TX
XTAL_IN	A11	I	10MHz Oscillator input
XTAL_OUT	B10	O	10MHz Oscillator output
I2S_FRCK	B9	O	I2S Interface, Frame clock output
I2S_BCK	A9	O	I2S Interface, Bit clock output
I2S_SDATA	C8	O	I2S Interface, Data output
I2S_MCLK	C7	O	I2S Interface, Master Clock output
GPIO1	B7	I/O	GPIO1: General purpose I/O
GPIO0	A7	I/O	GPIO0: General purpose I/O
STATUS	A6	O	STATUS: Device status output
RESET#	C6	I	Reset
DVDD	B2,C5,L1,L10, M4	Power	Digital I/O power supply
AVDD_LVDS_PLL	F1	Power	LVDS PLL power supply
VDD	B8,G2,H11, M8	Power	Core supply
AVDD_LVDS	A5,L5	Power	LVDS I/O power supply
AVDD_LD	F10	Power	Common Mode voltage, connect to decoupling capacitor of 200nF
AVDD	C11,D11	Power	Serial Link core power supply
AVDD_VCO	D10	Power	Serial Link VCO Power supply
VDD_XTAL	C9	Power	10MHz Oscillator core supply
DVDD_XTAL	A10	Power	10MHz Oscillator digital supply
GND	A8,B5,C3,C10 ,C12,E12,G1, G3,G12,H10, K3,K5,K7,M11	GND	Ground

Table 3-1: Pin description

Signal Name	Pin #	Type	Description
reserved	K6,K12,B6	I	reserved, pull down with 100kOhm to GND
Exposed Pad		GND	must be connected to GND
NC	L6,M7,L7,L8, H12,G11,F11, F12,A3,B1,C1 ,C2,C4,D1,D2 ,D3,E1,E2,F3, E3,E10,F2, G10		do not connect, place pad for mechanical stability

Table 3-1: Pin description

a. boot strap pins are sampled on hardware reset and need to be pulled to a defined value. See INAP378RAQ user manual for the functional description.
b. n-channel open drain
c. CML interface

3.1 Reset

The pin RESET# triggers an asynchronous reset (active low) and can be activated any time. This reset erases all configuration settings. Please see Table 3-2 for the status of all pins during reset.

Signal Name	Pin #	Reset State	Functional State
PX[19:1]	A2,B3,B4,A4, L2,H3,J1,J3, K2,J2,K1,H1, H2,K4,L3,M2, M3,L4,M5	Tri-State	Output [a]
BST2	M6	Input	Output
SPI_S_SDO / BST3	K8	Input	Output
SPI_S_SDI	M9	Input	Input
SPI_S_SCK	L9	Input	Input
SPI_S_STALL / BST4	M10	Input	Output
SPI_S_CS0#	K9	Input	Input
SPI_S_CS1#	K10	Input	Input
SPI_S_CS2#	L11	Input	Input
SPI_S_RW	L12	Input	Input
SPI_S_MB0 / BST1	K11	Input	Output
SPI_S_MB1 / BST6	J10	Input	Output
I²C_SCL	J11	Tri-State	Tri-State / Output

Table 3-2: Reset States

Signal Name	Pin #	Reset State	Functional State
I²C_SD	J12	Tri-State	Tri-State / Input / Output
I2S_FRCK	B9	Output	Output
I2S_BCK	A9	Output	Output
I2S_SDATA	C8	Output	Output
I2S_MCLK	C7	Output	Output
GPIO1	B7	Input	Input / Output
GPIO0	A7	Input	Input / Output
STATUS	A6	Output	Output

Table 3-2: Reset States

a. Functional state depending on configuration. Tri-State if interface is powered down.

After reset release, the device checks pins BSTx and configures the internal blocks accordingly.

Pin	Description
BST1	0: Configuration via SPI (from host) or remote 1: Configuration via EEPROM
BST2	Only in case of EEPROM configuration 0: Configuration via I²C EEPROM 1: (not supported)
BST3	EEPROM Start address 0: 0x0 1: 0x100
BST4	0: (not supported) 1: APIX2 Mode
BST6	Default serial line driver configuration 0: 0 Meter cable 1: 10 Meter cable

Table 3-3: Boot strap options

4.0 Package Information

4.1 Pinout Diagram

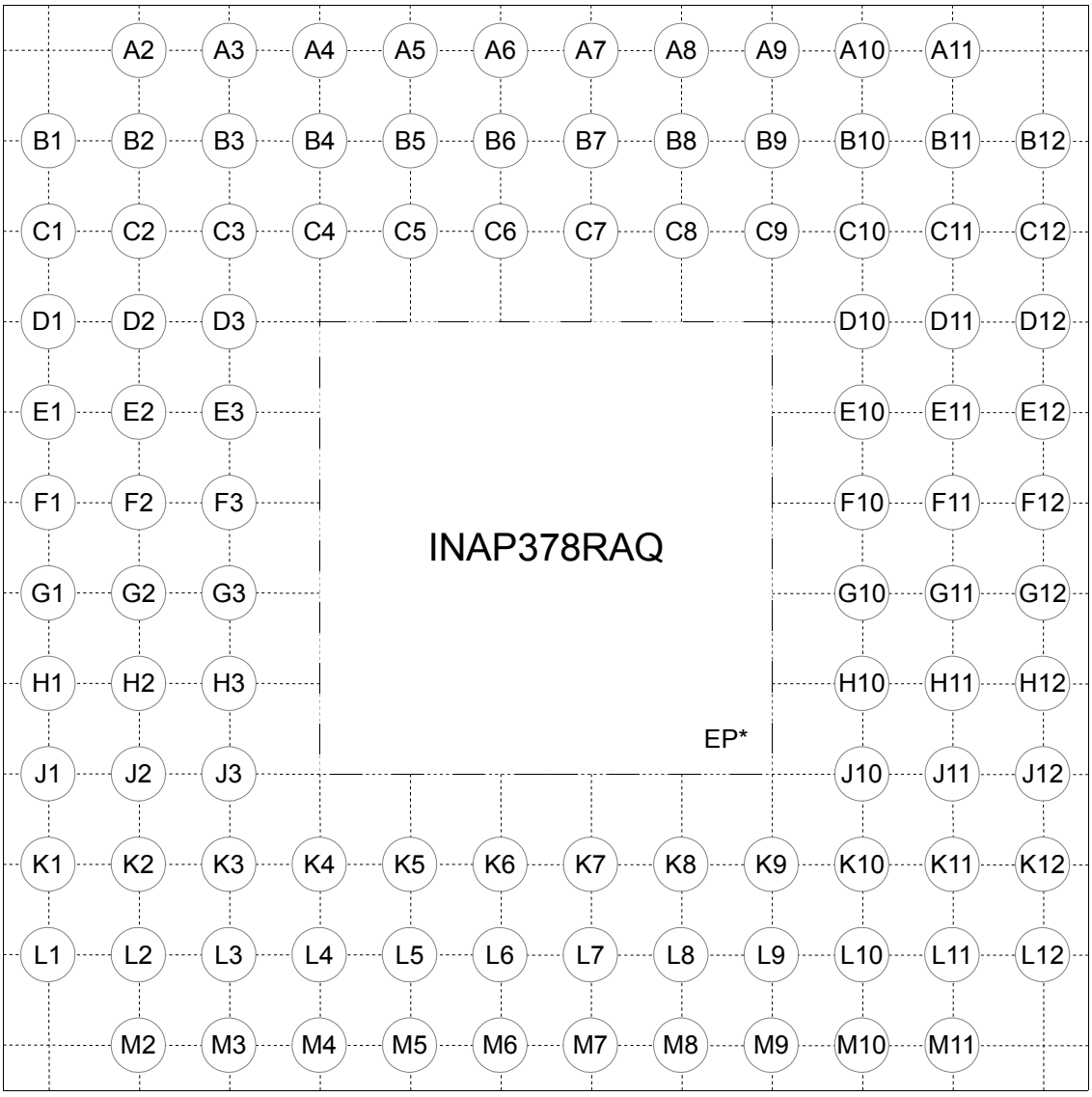


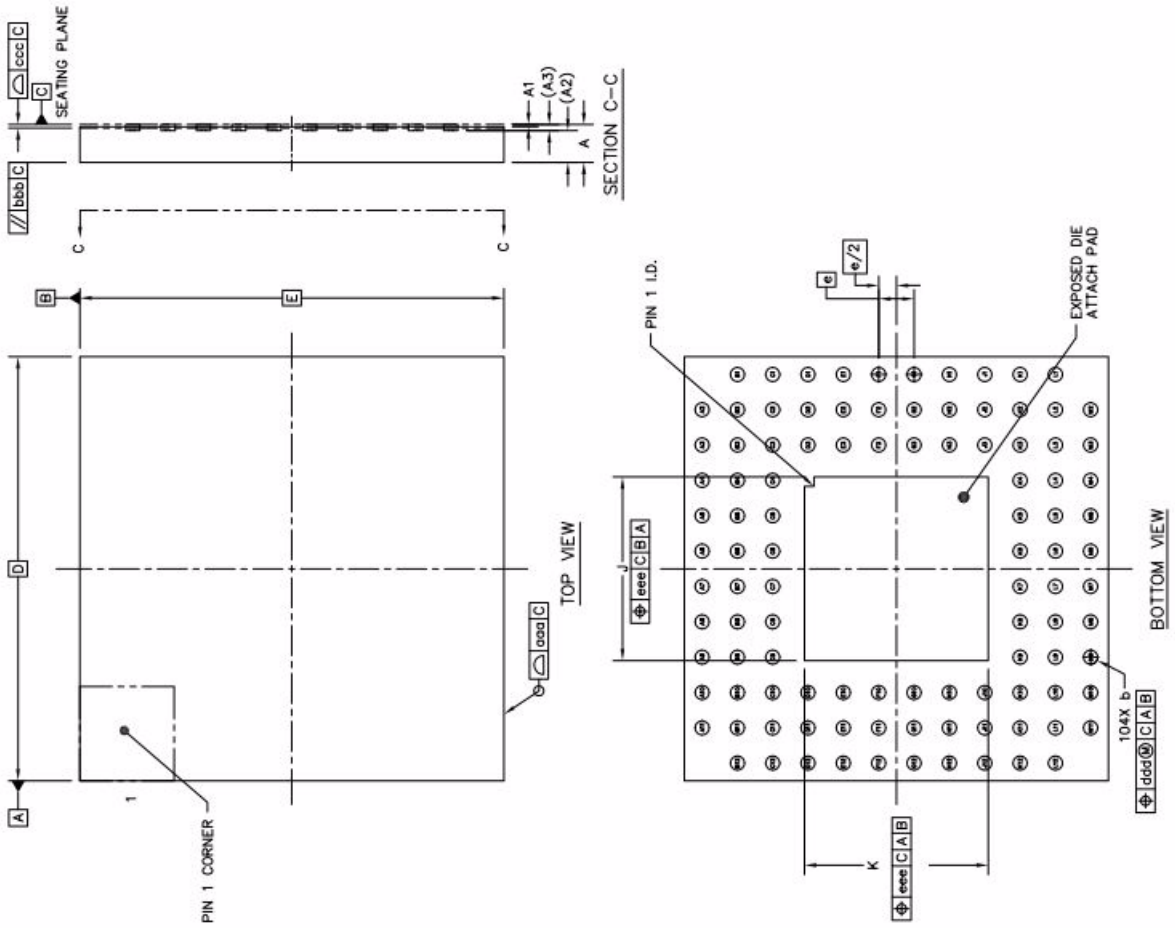
Figure 4-1: Pinout diagram, 104pin aQFN

* Exposed pad must be connected to GND

4.2 Package dimensions

	SYMBOL		MIN	NOM	MAX
TOTAL THICKNESS	A		---	---	0.85
STAND OFF	A1		0.02	0.05	0.08
MOLD THICKNESS	A2			0.675 REF	
L/F THICKNESS	A3			0.13 REF	
LEAD WIDTH	b		0.25	0.3	0.35
BODY SIZE	D			9 BSC	
	E			9 BSC	
LEAD PITCH	e			0.75 BSC	
EP SIZE	J	X	3.8	3.9	4
	K	Y	3.8	3.9	4
PACKAGE EDGE TOLERANCE	aaa			0.15	
MOLD FLATNESS	bbb			0.2	
COPLANARITY	ccc			0.08	
LEAD OFFSET	ddd			0.08	
EXPOSED PAD OFFSET	eee			0.1	

NOTES
1.0 COPLANARITY APPLIES TO LEADS, CORNER LEADS AND DIE ATTACH PAD.



5.0 Bibliography

[1] – openLDI Specification, National Semiconductors, Rev. 0.95

6.0 Revision History

Revision	Date	Changes
0.1	Feb 2013	• Initial Release

Table 6-1: Revision History

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