The allround automotive gigabit link

The next generation of Automotive Pixel Link (APIX) transmits encrypted high-bandwidth video streams

At the recent *embedded world 2012* show in Nuremberg, Inova Semiconductors together with Analog Devices for the first time presented transmission of HDCP-encrypted HD videos over APIX2. That opens the way for unrestricted use of this new 3 Gbit/s transmission standard – which already went on the road a few weeks back in series vehicles – in multimedia applications. Producers like Analog Devices and Fujitsu Semiconductor already announced at the show lead products of their own with APIX2 interface and HDCP capability.

By Roland Neumann and Michael Riedel

When Inova Semiconductors developed its APIX (Automotive Pixel Link) in 2006 the aim was to create a reliable and robust gigabit link for data transmission in vehicles. Unlike legacy, purely display interfaces APIX was for the first time to transmit not only digital video signals but at the same time – and independently of them – check and control data on the same cable. The first APIX with a data rate of 1 Gbit/s premiered in November 2008 in the new 7-series BMW, connecting a head-up display to a control unit. Since then APIX has gone into millions of vehicles, primarily as a display link but now also, from the first producers, to join up cameras in driver assistant systems.

1 Gbit/s data rate might have looked a secure bet for the future back then, but reality soon caught up. Together with electromobility, in-car infotainment with increasingly improved graphics and large, high-resolution displays is now a central focus in automotive electronics for major producers.

Inova Semiconductors responded to this with APIX2. Compared to APIX1, 3 Gbit/s treble the data rate on the downlink and 187.5 Mbit/s on the uplink too. APIX2 simultaneously trans-

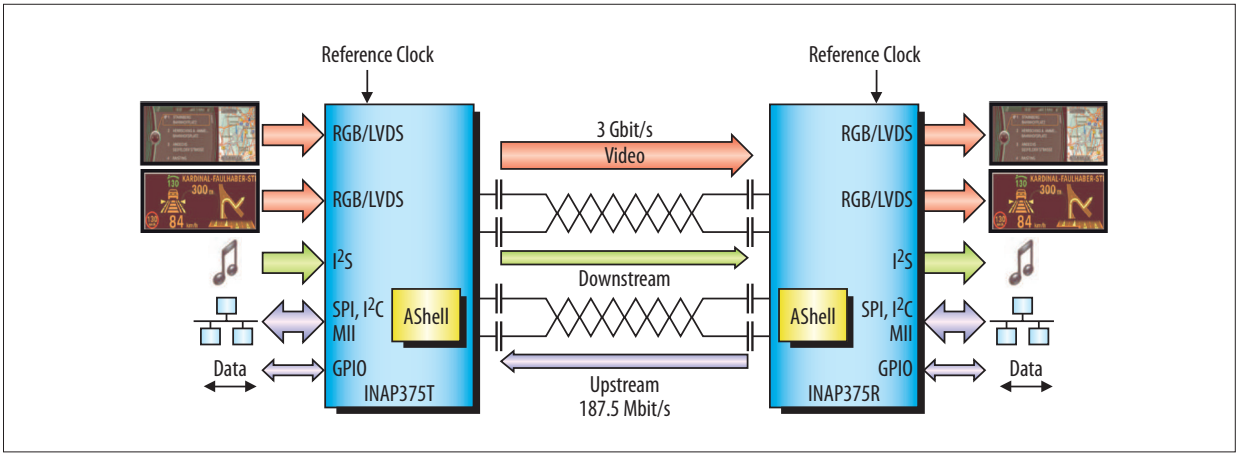

Fig. 1. Block diagram of 3 Gbit/s APIX2 link for simultaneous transmission of video, audio and other data including 100 Mbit/s Ethernet.

mits two separate video channels that are each freely configurable in resolution, color depth and frame rate. Plus, as many as eight digital audio channels (4 × stereo or 7.1, for surround sound for instance) can be transmitted over the I²S interface. Parallel to this, the integrated APIX2 communication channels enable high-grade data transfer. On these it is additionally possible to transmit control and checking data or – highly topical – to work HDCP authentication and encryption, specially protected by the integrated AShell2 (Automotive Shell) protocol. APIX2 also features a standard-compliant Media Independent Interface (MII), offering a Fast Ethernet physical layer (100 Mbit/s) that transports Ethernet data and protocols without restrictions (**Fig. 1**).

Special clock system between transmitter and receiver

APIX2 achieves this versatility through a clock system that sets it apart from legacy display links. Quite independently of frequency and quality of the pixel clock, e.g. jitter, a continuously working data link is set up between transmitter and receiver devices that in effect is like a conveyor belt (**Fig. 2**).

Data with different requirements in terms of transmission rate, latency, protection against transmission errors and with deviating dynamism of the data rate (burstiness) make exclusive use of a common transmission medium (cable). This is performed by a combination of statistical and deterministic multiplex, organizing and controlling timed allocation of the transmission channel to the different data streams of the application domain (video, I²S audio, GPIO, data). Here the available transmission rate is logically organized in a hierarchy of frames, consisting at the lowest level of micro packets. What is important here is, firstly, to make signalization of the occupancy of the frames resistant to transmission errors. And, secondly, to occupy a minimal share of transmission rate for the purpose, in other words to cut signalization and protocol overhead (**Fig. 3**).

For data streams consisting of bit-parallel words that are presented equidistant in time on the transmitter and must be read out in the same way on the receiver, like digital video/audio, the APIX2 receiver features clock synthesizers for optimal reconstruction of the timing gap between the data words.

Smart data safeguard

Extra emphasis was placed in development on protection of data, especially for safety-relevant applications. APIX2 consequently already satisfies major requirements for ASIL-compliant transmission to ISO 26262 standard.

The AShell2 that Inova developed for this purpose and integrated in the devices is a communication protocol implemented entirely in hardware to produce reliable data transmission

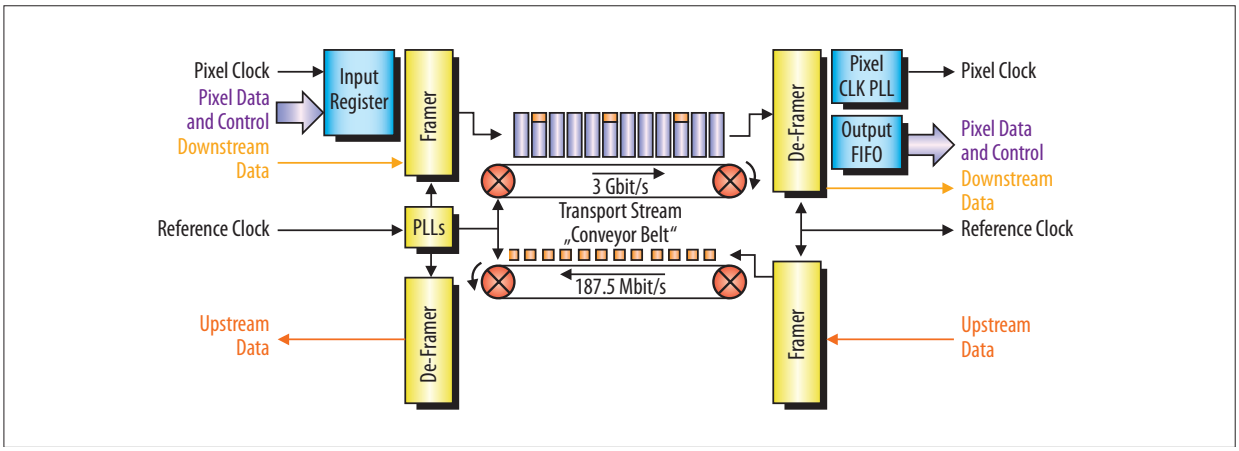

Fig. 2. Functional principle of APIX2: a "conveyor belt" that constantly transports all kinds of data packed in small containers.

between two AShell2 instances. It uses a cyclic redundancy check (CRC) to protect application data against errors during transmission on the serial channel. This CRC enables the receiver to detect transmission errors and then to force repetition of corrupted data by the transmitter through an automatic repeat request (ARQ) protocol.

In practical terms there is potential in transporting bits between the input of the transmitter device and the output of the receiver device for every serial transmission system to suffer errors. The causes are external physical effects of the environment, no matter whether bits in the transmission channel are corrupted, or the retiming of bits on the serial input of the receiver is so much affected that the wrong bit values are reconstructed.

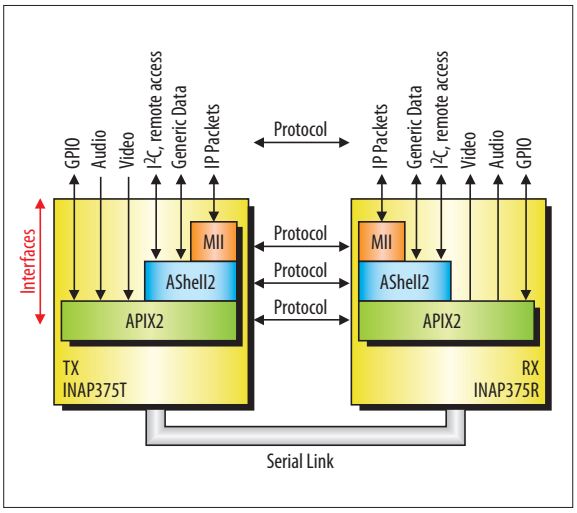

Fig. 3. Stacked communication layers in APIX2.

Errorfree transmission is nevertheless desirable or simply a necessity for most data streams in very many applications. So suitable measures have to be taken to prevent errors, to detect and/or correct them. If application data already contain inherent redundancy for instance, this can be done by weighting the plausibility of data extracted in the receiver. Or redundancy is added to the application data in the transmitter, i.e. extra information enabling error detection and possibly also correction.

But methods like these make the transmitter and receiver increasingly complex, produce data overheads, and limit serial transmission capacity for the real data of an application. What it takes, for a properly attuned technical solution, is a good model for the statistics of transmission errors to be expected, and the right grasp of what residual probability of errors an application can tolerate in its data. It is in most cases very difficult to define such fundamental parameters when developing a transmission system so that they match and can hold out in actual practice, especially if transmitter and receiver chips are to be an attractive fit in as many applications as possible. APIX2 uses some of the above methods to detect and correct errors, additionally implementing the AShell2 protocol layer for the non-specific data of an application as a way out of this dilemma. Only that information is permanently added to the data which enables error detection with very high probability — when an error is detected a protocol between the transmitter and receiver becomes active that is sustained until data are received entirely without errors. As long as transmission is not corrupted, this protocol produces virtually no overhead (approx. 1 percent) (**Table**).

Data that an application wants to send serially errorfree from the transmitter to the receiver are protected as above by the AShell2. The source and sink of these data are devices (e.g. MCU) of the common module that exchange the data with the APIX2 chips over SPI interfaces. If the data protection concept of an application also wants to safeguard this transmission path on the module against undetected errors, the APIX2 chip implements checksums (CRC) on its SPI

Errors (for given block size)	Probability of detecting error
up to 12 consecutive bits wrong	100 percent
1 bit wrong	100 percent
2 bits wrong (randomly distributed)	100 percent
3 bits wrong (randomly distributed)	100 percent
4 bits wrong (randomly distributed)	99.9 percent

Error detection rate of AShell2.

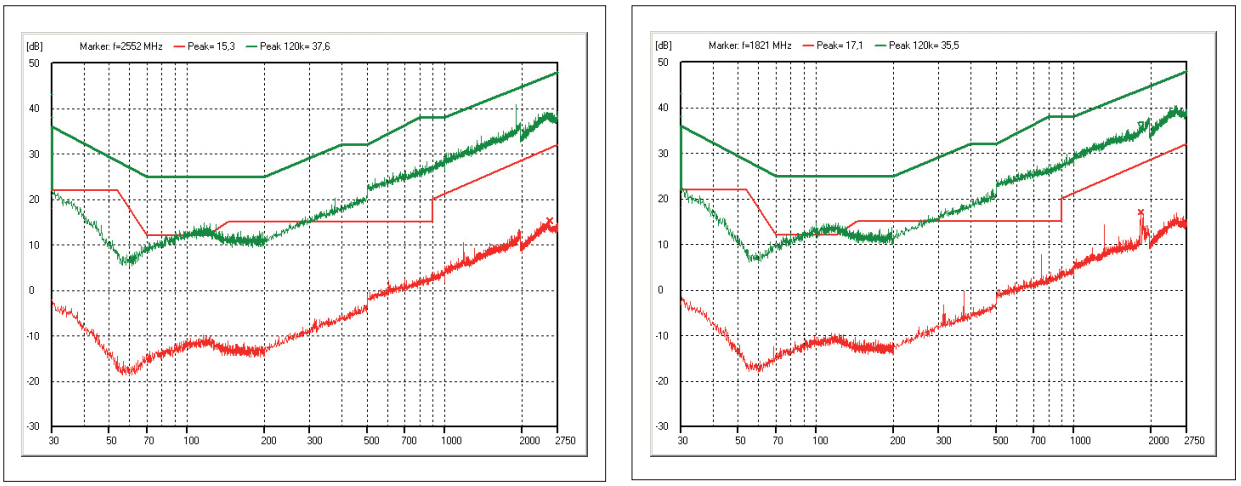

Fig. 4. EMI antenna measurement (radiation) on APIX2 link with 5-m STP cable and PRS12 signal. Left: open-circuit measurement in chamber with link down. Right: measurement at 3 Gbit/s downstream and 187.5 Mbit/s upstream.

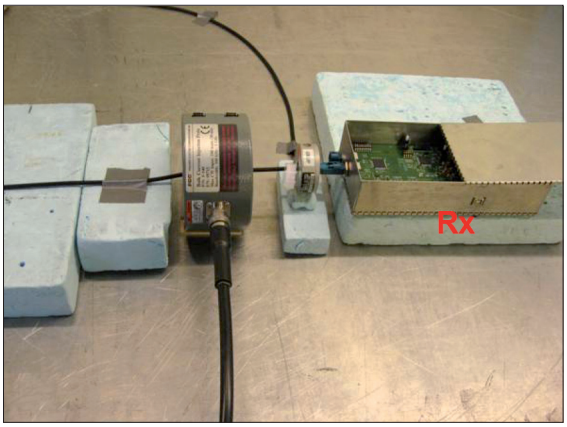

Fig. 5. Setup for BCI radiation immunity measurement in EMI laboratory.

interfaces for the transfered data that can be read out by the application and compared to the calculated values.

For a human observer the information in the pixels of video data usually contains a large amount of redundancy. Single, randomly occurring and randomly distributed bit errors in a frame are for the most part quite invisible. Although information describing video format – such as HSYNC, VSYNC, DE – is highly relevant, and many displays will respond with visible interference if signals of this kind are only briefly corrupted. APIX2 consequently provides extra protection of this information to transmit it errorfree.

The same effort is not devoted to protecting the video data however, so that the available serial transmission rate is not encumbered by unnecessary overhead.

Still, many an application will also demand information about errors in video data. Either to reject corrupted frames – or only those that are too heavily errored – or purely to have a criterion for permanent and dependable judgment of the quality of serial data transmission. For this purpose APIX2 implements a CRC over each horizontal picture line and transmits this to the receiver. The latter either indicates detected transmission errors on its status pin or passes the CRC to the sink of the video data so that in this way the path can be monitored as far as a frame buffer for instance.

The CRC polynomial that is used will detect burst errors up to 32 bits with a Hamming distance of 4 or 6 for frames with up to 1,364 24-bit pixels or 1,818 18-bit pixels per line. This means that up to four or six randomly distributed errors are detected to 100 percent. CRC-4 protection, as frequently used, only has a Hamming distance of 1 even if the CRC-4 polynomial is an optimum choice, i.e. it will only detect single bit errors to 100 percent although it generates 25 percent overhead for 16-bit wide camera data.

3 Gbit/s over copper cable

In addition to management and effective protection of all the different data and formats, APIX2 focused heavily on development of the analog 3-Gbit/s physical layer (PHY), responsible for physical transmission of data over copper cable. A requirement set by vehicle producers is use of the same low-priced cables for the higher 3 Gbit/s data rate as in transmission working at 1 Gbit/s. Nor are trade-offs expected in terms of reliability, EMI immunity and range. As part of a research project sponsored both on a federal basis and by the Bavarian state, Inova Semiconductors cooperated with the Fraunhofer IIS in developing a high-rel 3-Gbit/s PHY. Among other things this saw the creation and successful application of a process to simulate and continuously optimize EMI behavior during chip design already. Additionally, a special line code enables the generation of a constant, serial bit stream that is entirely independent of the type and content of transmitted data, and consequently shows no spectral lines caused by video content.

As a result APIX2 is virtually invisible in terms of electromagnetic radiation even at a maximum transmission rate of 3 Gbit/s downstream and 187.5 Mbit/s upstream (**Fig. 4**). APIX2 also sets new standards when it comes to immunity against interference fields. Even exposed to 350 mA RF interference current – a new critical value being specified by the first OEMs (the figure at present is still 100 mA) – transmission of data remains stable and reliable (**Fig. 5**).

In addition to actual chip development, Inova Semiconductors engineers looked very closely at the cable/connector interface – a central and critical element of the entire gigabit transmission system. Extra to its own thorough investigations, here Inova cooperated close-up with major OEMs, cable and connector manufacturers. This produced integrated and user-programmable, digital filters for the transmitter and receiver chips allowing optimum connectivity between transmission system and cable (**Fig. 6**). These filters plus an adaptive equalizer in the receiver automatically compensate aging effects in the cable and, together with built-in tests, allow assessment of momentary transmission quality. In this way deterioration of the transmission properties of a cable can be detected before the user notices a fault or the entire transmission fails.

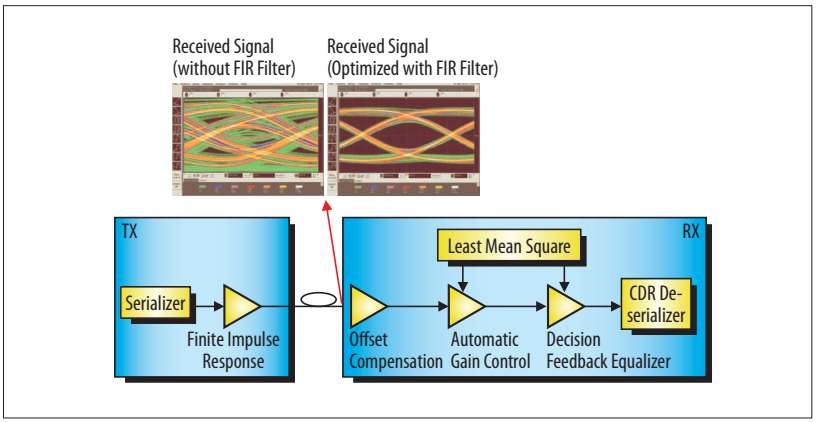

Fig. 6. Digital filters and equalizer in APIX2 produce optimum matching to STP copper cable and can also compensate aging effects.

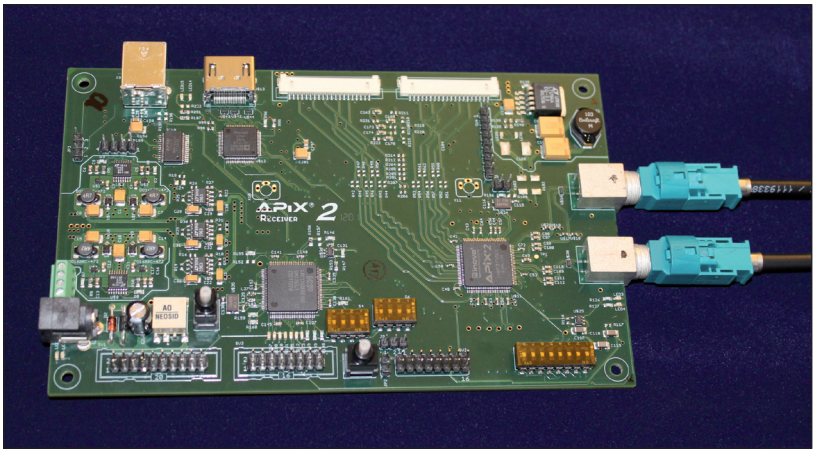

Fig. 7. New modular ADK2 development kit for APIX2 with APICO software for straightforward configuration and control of transmission system.

Inova recently introduced a special software tool to enable complete simulation of the transmission performance of a cable as a function of FIR and DFE settings. With this the user can not only optimize for their application but also consider marginal conditions in their settings with potential cable aging effects for example.

Modular application kit for developers

APIX2 presents a variety of interfaces and possible applications. For thorough evaluation of this platform Inova Semiconductors offers the modular ADK2 developer kit for straightforward operation by APICO software (**Fig. 7**, **Fig. 8**). The kit consists of a basic module ready including all essential functionality of APIX2, in particular video and audio transmission. Additional, plug-in adapter boards enable the user to implement an Ethernet link or use APIX2 as a camera link. Here Inova offers dual-chip camera modules from Taiwanese producer Supertech with APIX2 as well as Omnivision OV10630 megapixel sensors or Aptina MT9M024. This camera add-on will also operate seamlessly with Omnivision's Panther tool or DevWare from Aptina.

Semiconductor producers support APIX2

Now that APIX2 is in series, Inova Semiconductors is also looking to the first APIX2 derivates specially for multimedia applications and ultra-compact dual-chip cameras in driver assistant systems. Analog Devices and Fujitsu attended the *embedded world* show announcing their first APIX2 multimedia gateway and display controller products with HDCP functionality. Another major semiconductor producer is already working on a new APIX2 device to link high-performance in-car graphics processors.

At Inova Semiconductors meanwhile, initial studies are under way for upcoming APIX generations, to meet increasingly demanding requirements for infotainment systems in vehicles longterm, to 2020 and beyond, with a consistent APIX platform. *sj*

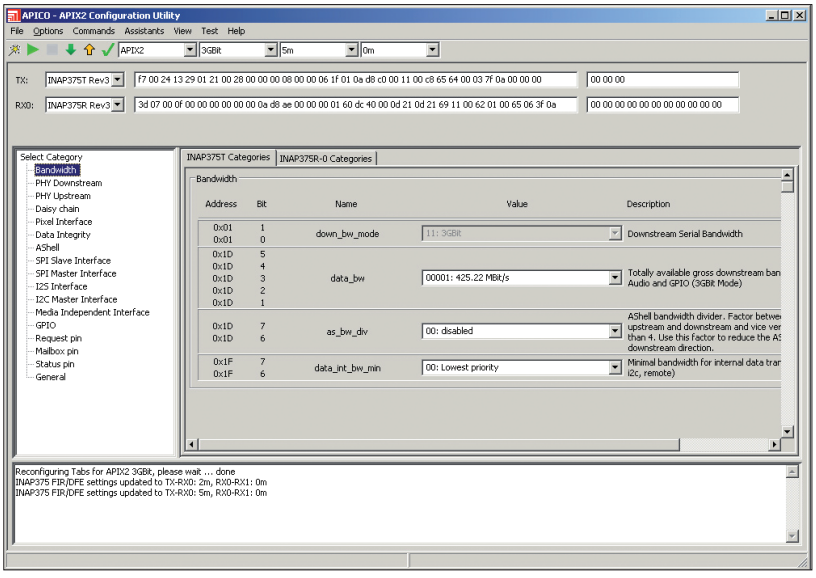

Fig. 8. User menu of APICO software.

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