3GBit/s APIX2 Receiver with HDCP Support

INAP395R

The INAP395R is an APIX2 receiver device supporting the reception of copyright protected digital entertainment content. The device incorporates the decryption mechanisms as well as the required keys to receive HDCP 1.4 encoded video and audio content over the APIX2 link. APIX2 is a DC-balanced, AC coupled low latency, point-to-point link over shielded twisted pair (STP) copper cables. Its scalable physical layer provides bandwidth from 500Mbit/s of up to 3 GBit/s at lowest EMI. The INAP395R offers a flexible video interface, optimized for TFT panels or graphic processing SoCs, with input interfaces such as parallel RGB or OpenLDI LVDS.

Software adjustable driver characteristics, selectable interfaces and configurable operating modes allow maximum transmission distances of up to 10m @ 3GBit/s. In addition to the video transmission, the INAP395R allows completely independent full duplex communication channels. Using the internal AShell protocol, data transfers such as panel control or touch control information are protected by error detection and retransmission mechanisms.

The INAP395R offers various interfaces to directly drive and connect to graphic display- or touch controllers. Besides an I^2C compliant interface, the link is optimized to carry low latency GPIO signals for reset or hardware signal switching. Various data integrity features like CRC on video data, monitoring of control signals support secure data transfer over the APIX2 link. The device is offered in a 100 pin LQFP package, and qualified according to the AEC-Q100 automotive standards.

Applications:

- Central Information Displays
- Rear-Seat Entertainment Systems
- Audio/Video Systems
- Device Gateways
- Infotainment Head Units

Features:

- Supports High-bandwidth Digital Content Protection according to HDCP 1.4
- Pin compatible to INAP375R
- video data rates up to 2591 MBit/s
- up to 187.5 MBit/s upstream link bandwidth
- Supports 2 independent HDCP encrypted video streams
- Configurable video interface
  - Parallel RGB (10,12,18 or 24 Bit)
  - openLDI compliant LVDS interface
    - Parallel Single Channel (18 or 24 Bit)
    - Dual Channel (18 or 24 Bit)
  - Parallel Bulk Data Mode (10,12,18,24 Bit)
- Video resolutions up to HD resolutions
- AShell protected full duplex communication channel
- Daisy chain output to a 2nd receiver
- Media Independent Interface
- Flexible data interface
  - SPI Master/slave
  - I^2C Master
- Low latency GPIOs
- I^2S Audio interface
  - supports 16/24/32 Bit word length
  - supports up to 192kHz sampling
  - TDM support for up to 8 channels
- Diagnostic Features:
  - Built-In PRBS Checker
  - Embedded diagnostics
- Up to 10m distance at 3 GBit/s

Package:

- 100 pin LQFP

Temperature/Quality:

- -40°C to +105°C
- AEC-Q100

1.0 Block diagram

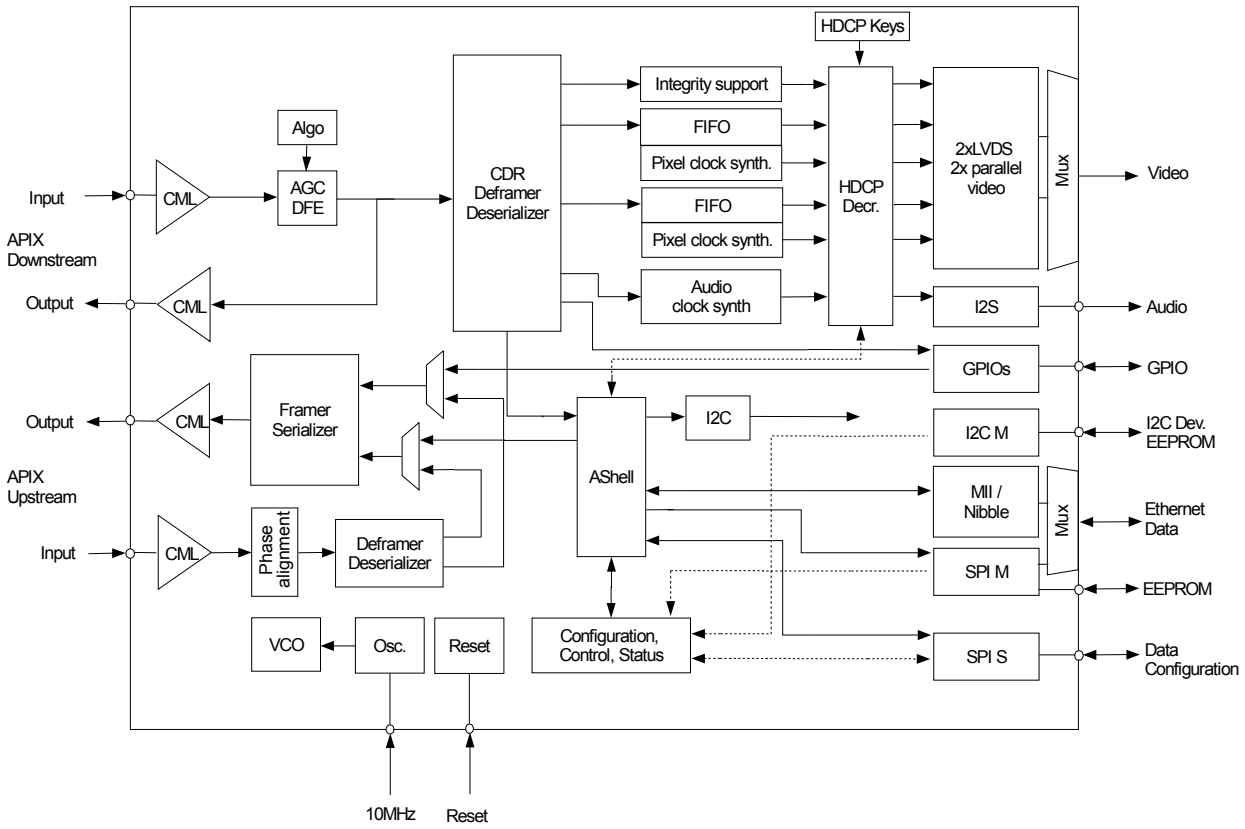


Figure 1-1: Block diagram

2.0 Electrical Characteristics

2.1 Absolute Maximum Ratings

The absolute maximum ratings define values beyond which damage to the device may occur. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The functional operation of the device at these or any other conditions beyond the recommended operating ratings is not guaranteed.

Parameter	Description	Min.	Max.	Units	Note
V_{DVDD}, V_{DVDD_XTAL}	DC Supply Voltage	-0.5	5.0	V	
V_{VDD}, V_{AVDD}, V_{AVDD_LVDS}, V_{VDD_XTAL}	Input Voltage	-0.5	3.0	V	
I_D	I/O Current (DC or transient any pin)	-20	+20	mA	
T_{stg}	Storage Temperature	-55	+150	° C	
T_{SLD} / T_{SLD}	Max Soldering Temperature		260	° C	40 seconds maximum
-	ESD Protection HBM JEDEC JESD22/A114	-3	+3	kV	R_D=1.5kΩ, C_S=100pF
-	ESD Protection CDM EIA/JEDEC JESD22/C101	-1	+1	kV	
-	ESD Protection MM EIA/JEDEC JESD22-A115A	-200	+200	V	

Table 2-1: Absolute maximum ratings

2.2 Recommended Operating Conditions

Parameter	Description	Min.	Typ.	Max.	Units
V_{VDD}, V_{VDD_XTAL}	Digital Core supply, Oscillator supply	1.71	1.8	1.89	V
V_{DVDD}, V_{DVDD_XTAL}	Digital IO Supply, Digital Oscillator supply	3.0	3.3	3.6	V
V_{AVDD}, V_{AVDD_VCO}	CML PHY supply voltage, VCO supply	1.71	1.8	1.89	V
$V_{AVDD\_LVDS\_PLL}$, V_{AVDD_LVDS}	LVDS PLL & Core supply	1.71	1.8	1.89	V
V_{SUPPLY_NOISE}	Analog and Digital Supply Noise			50	mV
T_a	Ambient Temperature	-40	-	+105	° C

Table 2-2: Recommended operating conditions

2.3 Electrical Characteristics

2.3.1 Serial Interface

2.3.1.1 Downstream interfaces

The INAP395R offers two serial interfaces in downstream direction. The downstream input interface expects serial data coming from an APIX transmitter device.

Parameter	Description	Min.	Typ.	Max.	Unit
V_{diff_in}	Differential input voltage range	±60 [a]	-	±500	mV
V_{cmm_SDIN}	Serial input common mode range	V_{AVDD} - 0.5V + (V_{diff_in}/2)	-	V_{AVDD} + 0.5V - (V_{diff_in}/2)	V
$J_{acceptance}$	Random Jitter acceptance	-	-	±7.5	mUI

Table 2-3: Downstream input interface characteristics (SD_DWN_IN_P, SD_DWN_IN_N)

[a] Min value at 0.3/0.7 UI

The optional downstream output interface acts as transmitter output to a second connected APIX2 Rx device. Specified with a load of 50Ω.

Parameter	Description	Min.	Typ.	Max.	Unit
$V_{out\_nom\_dwn}$	Downstream differential output voltage	±100	-	±500	mV

Table 2-4: Downstream output interface characteristics (SD_DWN_OUT_P, SD_DWN_OUT_N)

2.3.1.2 Upstream interfaces

The INAP395R offers two serial interfaces in upstream direction. The upstream output interface transmits serial data to a connected APIX transmitter device. Specified with a load of 50Ω.

Parameter	Description	Min.	Typ.	Max.	Unit
$V_{out\_nom\_up}$	Upstream differential output voltage	-	-	±500	mV

Table 2-5: Upstream output interface characteristics (SD_UP_OUT_P, SD_UP_OUT_N)

The optional upstream input interface expects serial data coming from a second connected APIX2 receiver.

Parameter	Description	Min.	Typ.	Max.	Unit
V_{diff_in}	Differential Input Voltage Range	±60	-	±500	mV
V_{cmm_SDIN}	Serial input common mode range	V_{AVDD} - 0.5V + (V_{diff_in}/2)	-	V_{AVDD} + 0.5V - (V_{diff_in}/2)	

Table 2-6: Upstream input interface characteristics (SD_UP_IN_P, SD_UP_IN_N)

2.3.2 Supply Current

Parameter	Description	Typ.	Max.	Unit
$I_{VDD} + I_{VDD\_XTAL}$	Digital Core & Oscillator Supply Current	95	150	mA
$I_{DVDD} + I_{DVDD\_XTAL}$	Digital IO & Oscillator Supply Current	60	120	mA
$I_{AVDD\_LVDS} + I_{AVDD\_LVDS\_PLL}$	LVDS Core & PLL Supply Current	-	30	mA
I_{AVDD}	CML PHY Supply Current	130	210	mA
I_{AVDD_VCO}	VCO Supply Current	5	15	mA

Table 2-7: Supply current

2.3.3 Pixel Interface

The INAP395R's pixel interface can be configured to RGB or/and LVDS outputs. For further informations please refer to the INAP395R user manual.

2.3.3.1 RGB Interface

Parameter	Description	Test Condition	Min.	Max.	Units
V_{OH}	Output High Voltage	IOH= -4mA	2.4	-	V
V_{OL}	Output Low Voltage	IOL= 4mA	-	0.4	V

Table 2-8: RGB characteristics

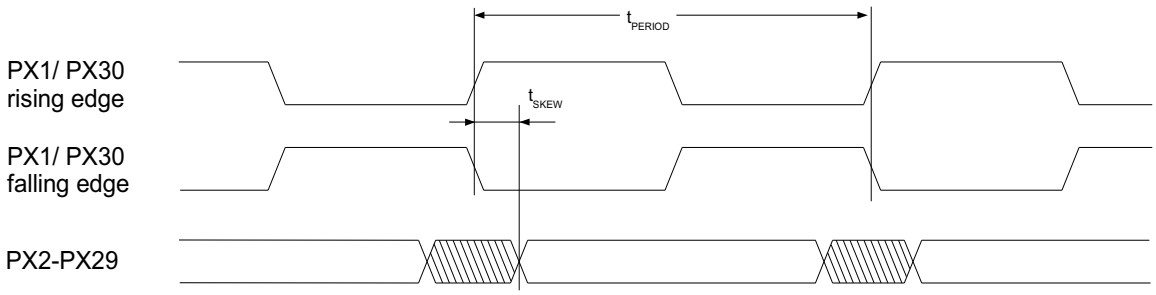


Figure 2-1: RGB Interface Timing

The active edge of pixel clock can be set to rising or falling. For further information please refer to the INAP395R user manual. f_{PIXEL_CLOCK} is the reciprocal of t_{PERIOD} . All values specified for T_A=25°C.

Parameter	Description	Test Condition	Min.	Max.	Units
f_{PIXEL_CLOCK}	Pixel Clock Output Frequency		5	120	MHz
t_{SKEW}	Skew Pixel Clock Active Edge To Pixel Data		-2	1	ns

Table 2-9: RGB Interface timing

2.3.3.2 LVDS Interface

LVDS interface according to TIA/EIA644 specification. Exceptions are listed at Table 2-10.

Parameter	Description	Min.	Max.	Units
V_{OD}	Differential Output Voltage	247	454	mV
V_{OS}	Offset Voltage	1.125	1.375	V
V_{COD}	|Change to V_{OD}|	-	50	mV
V_{COS}	|Change to V_{Os}|	-	50	mV
I_{SA}	Short Circuit Current	-	24	mA
V_{TH}	Receiver Threshold Voltage	-	+100	mV
f_{LVDS_CLK}	LVDS Clock Frequency	5	80	MHz

Table 2-10: LVDS interface exceptions to TIA/EIA644 specification

2.3.4 Data Interface

2.3.4.1 General Characteristics

The following characteristics are valid for SPI, SBDOWN, SBUP, GPIO, I^2S, MII / Nibble data and I^2C functionality. The pins I2C_SCL/INBOUND_TS and I2C_SD/OUTBOUND_TS are open drain outputs and require external pull up circuitry. All values specified for T_A=25°C.

Parameter	Description	Test Condition	Min.	Max.	Units
V_{IH}	Input High Voltage		2.0	V_{DVDD}	V
V_{IL}	Input Low Voltage		0	0.8	V
I_{IH_PD}	Pull Down Current [a]	Vin = V_{DVDD}	30	120	µA
I_{IH}	Input High Current	Vin = V_{DVDD}	-10	10	µA
I_{IL}	Input Low Current	Vin = 0 V	-10	10	µA
V_{OH}	Output High Voltage [b]	IOH= -3mA, Figure 2-14	2.4	-	V
V_{OL}	Output Low Voltage	IOL= 3mA, Figure 2-14	-	0.4	V
t_{RO}	Output Rise Time [b]	C_L=5pF	-	2.6	ns
t_{FO}	Output Fall Time [b]	C_L=5pF	-	2.1	ns

Table 2-11: General IO Characteristics

a. pins with internal pull down to GND
b. not relevant for open drain outputs

2.3.4.2 SPI Slave Interface timing

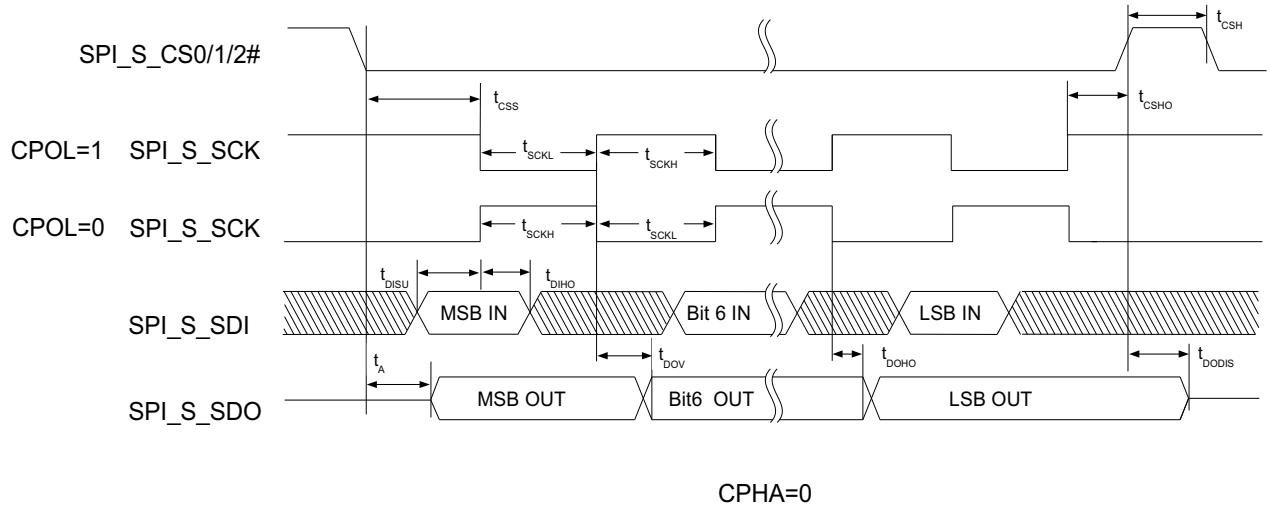


Figure 2-2: SPI Slave Timing Diagram (CPHA=0)

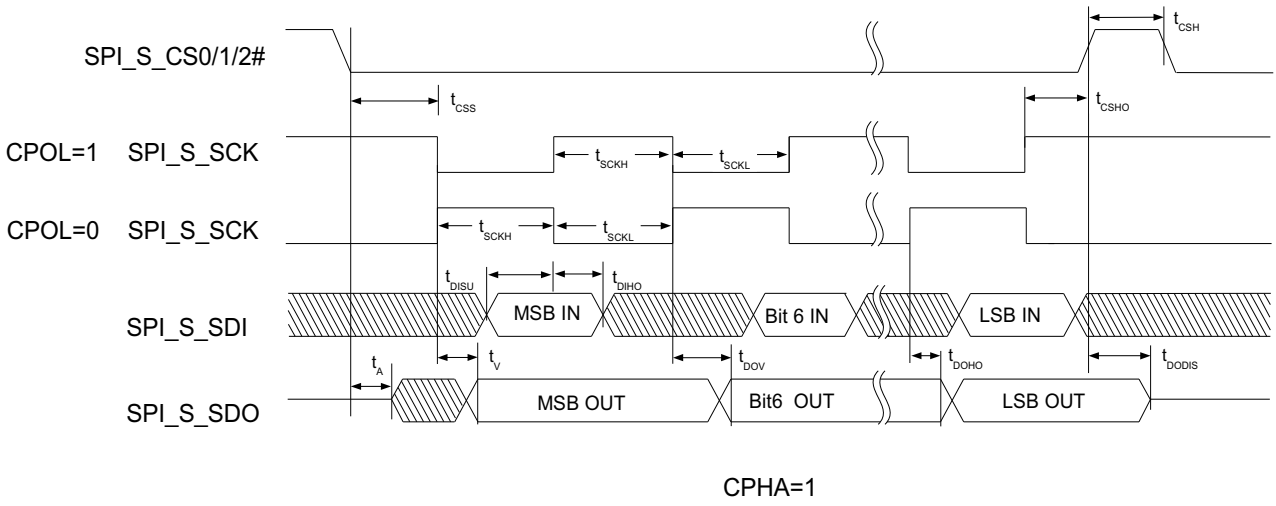


Figure 2-3: SPI Slave Timing Diagram (CPHA=1)

The SPI Slave interface can be flexibly configured with the parameters cfg_spi_s_cpol, cfg_spi_s_cpha. For further informations please refer to the INAP395R user manual.

All values specified for T_A=25°C.

Parameter	Description	Min	Max	Units
f_{SCK}	SCK Clock Frequency	-	15	MHz
t_{SCKH}	SCK High Time	33	-	ns
t_{SCKL}	SCK Low Time	33	-	ns
t_{CSH}	CS# High Time	15	-	ns
t_{CSS}	CS# Setup Time	33	-	ns
t_{CSHO}	CS# Hold Time	34	-	ns
t_{DISU}	Data In Setup Time	12	-	ns
t_{DIHO}	Data in Hold Time	12	-	ns
t_{DOV}	Data Output Valid Time	-	29	ns
t_{DOHO}	Data Output Hold Time	5	-	ns
t_{DODIS}	Data Output Disable Time	-	45	ns
t_A	Data Access Time	15	-	ns

Table 2-12: SPI Slave Interface characteristics (Read Access)

Parameter	Description	Min	Max	Units
f_{SCK}	SCK Clock Frequency	-	41	MHz
t_{SCKH}	SCK High Time	12	-	ns
t_{SCKL}	SCK Low Time	12	-	ns
t_{CSH}	CS# High Time	15	-	ns
t_{CSS}	CS# Setup Time	12	-	ns
t_{CSHO}	CS# Hold Time	34	-	ns
t_{DISU}	Data In Setup Time	12	-	ns
t_{DIHO}	Data In Hold Time	12	-	ns

Table 2-13: SPI Slave Interface characteristics (Write Only Access)

2.3.4.3 SPI Master Interface timing

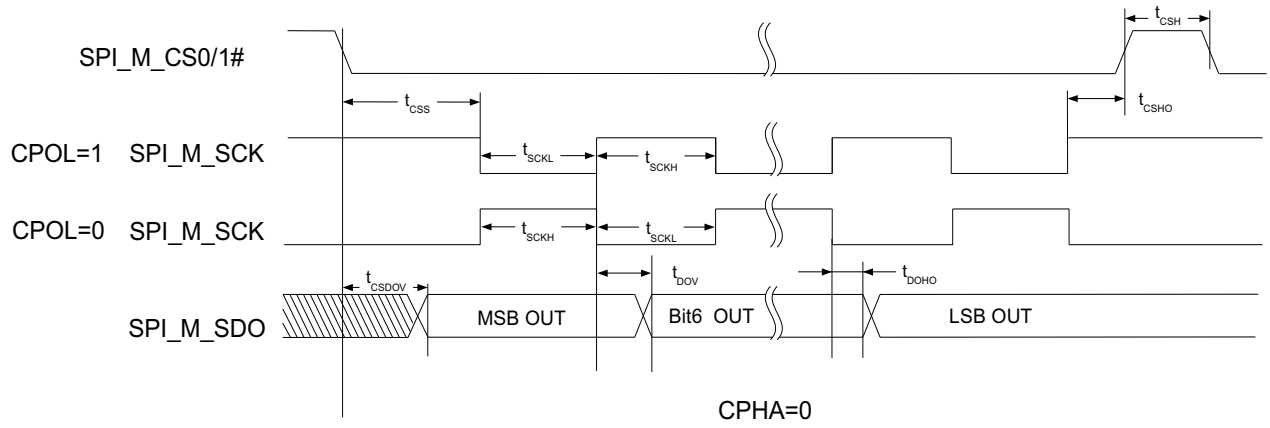


Figure 2-4: SPI Master Timing Diagram (CPHA=0)

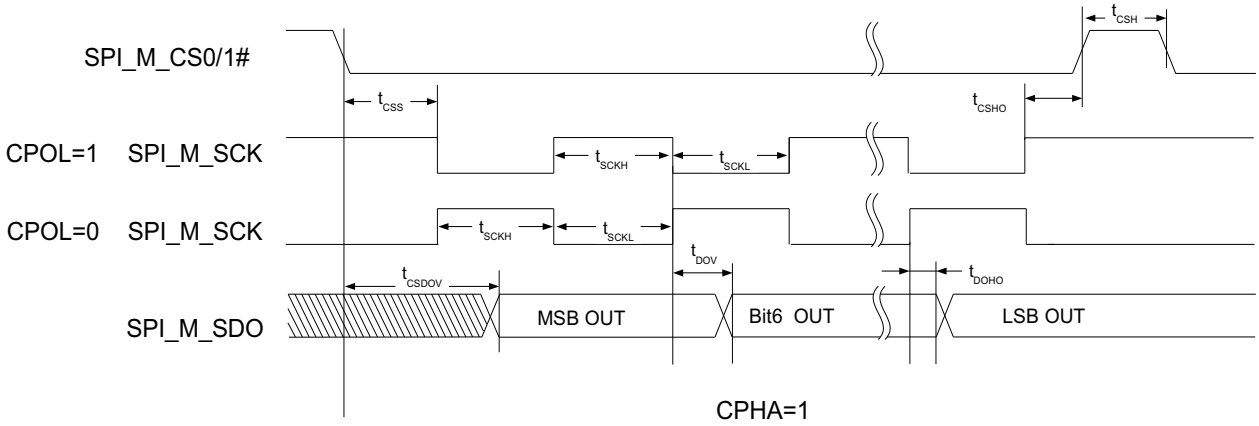


Figure 2-5: SPI Master Timing Diagram (CPHA=1)

The SPI Master interface can be flexible configured with the parameters cfg_spi_m_cpol, cfg_spi_m_cpha, cfg_spi_m_clock_div, cfg_spi_m_cs_delay and cfg_byte_cnt. For further informations please refer to the INAP395R user manual.

Core clock frequency is 187.5MHz. All values specified for T_A=25°C.

Parameter	Description	Min.	Max.	Units
f_{SCK}[a]	SCK Clock Frequency	0.011	23.44	MHz
t_{SCKH}	SCK High Time	12	-	ns
t_{SCKL}	SCK Low Time	16	-	ns

Table 2-14: SPI Master Interface characteristics

Parameter	Description	Min.	Max.	Units
t_{CSH}	CS# High Time	6	-	ns
t_{CSS}[b]	CS# Setup Time (configurable)	85	-	ns
t_{CSHO}	CS# Hold Time	30	-	ns
t_{DOV}	Data Output Valid Time	-	10	ns
t_{DOHO}	Data Output Hold Time	-5	-	ns
t_{CSDOV}	CS To Data Valid Time	-	100	ns

Table 2-14: SPI Master Interface characteristics

a. can be configured from core clock/16384 to core clock/8 by cfg_spi_m_clock_div
b. can be configured from 16 to 48 core clock cycles by cfg_spi_m_cs_delay and depends on CPOL, CPHA

2.3.4.4 SPI EEPROM Master Interface timing

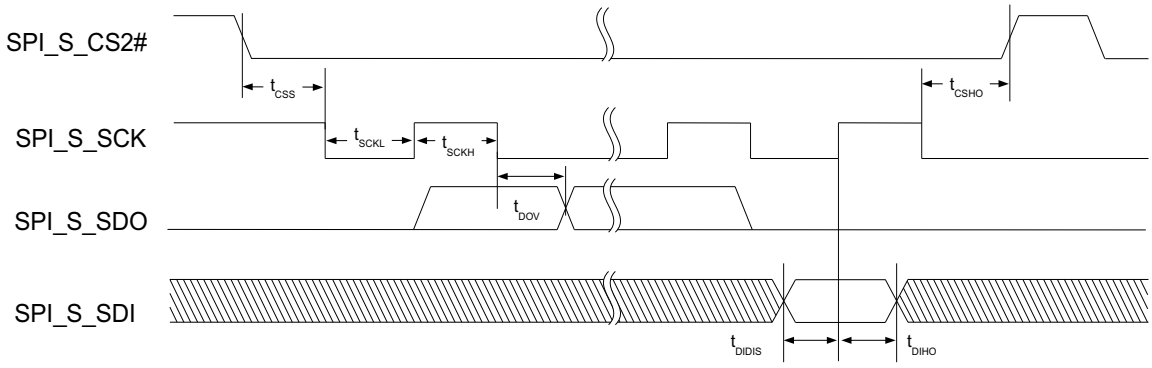


Figure 2-6: SPI EEPROM Master Timing Diagram

The SPI Master timings depend on the accuracy of the external 10MHz reference clock and are therefore listed as typical values. For the EEPROM Master Timing the internal parameters are used: CPOL=0, CPHA=0, t_{CSS} delay = 48 wait core cycles and divider = core clock/128. All values specified for T_A=25°C.

Parameter	Description	Min	Max.	Units
f_{SCK}	SCK Clock Frequency	-	1.46	MHz
t_{SCKH}	SCK High Time	-	341	ns
t_{SCKL}	SCK Low Time	-	341	ns
t_{CSS}	CS# Setup Time	597	-	ns
t_{CSHO}	CS# Hold Time	30	-	ns
t_{DISU}	Data In Setup Time	30	-	ns
t_{DIHO}	Data In Hold Time	30	-	ns
t_{DOV}	Data Output Valid Time	-5	5	ns

Table 2-15: SPI Master EEPROM Interface characteristics

2.3.4.5 I²C Interface timing

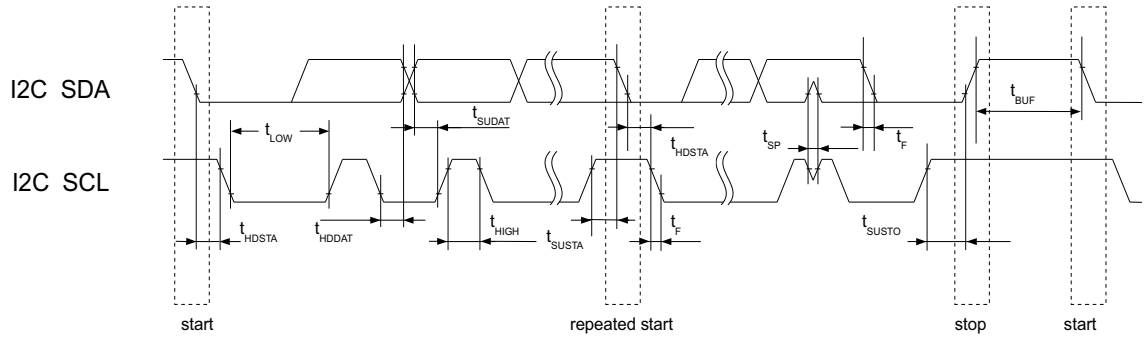


Figure 2-7: I²C Timing Diagram

The I²C timings depend on the accuracy of the external 10MHz reference clock and are therefore listed as typical values. All values specified for T_A=25°C.

Parameter	Description	Min.	Typ.	Max.	Units
f_{SCL}	SCL Clock Frequency Standard Mode Fast Mode	-	-	 100 400	kHz
t_{HIGH}	SCL High Time Standard Mode Fast Mode	-	 4.03 1.08	-	µs
t_{LOW}	SCL Low Time Standard Mode Fast Mode	-	 6.0 1.5	-	µs
t_{HDSTA}	Hold Time (repeated) START condition Standard Mode Fast Mode	-	 4.0 1.0	-	µs
t_{HDDAT}[a]	Data Hold Time Standard Mode Fast Mode	-	 4.0 1.0	-	µs
t_{SUDAT}	Data Setup Time Standard Mode Fast Mode	-	 2.0 0.5	-	µs
t_{SUSTA}	Setup Time for repeated START condition Standard Mode Fast Mode	-	 6.03 1.58	-	µs

Table 2-16: I²C Interface characteristics

Parameter	Description	Min.	Typ.	Max.	Units
t_{SUSTO}	Setup Time for STOP condition Standard Mode Fast Mode	-	 4.03 1.08	-	µs
t_{BUF}	Bus Free Time Standard Mode Fast Mode	-	 10.0 2.5	-	µs
t_f	fall time of SDA and SCL Standard Mode Fast Mode[b]	-	-	 300 300	ns
t_{SP}	pulse width of spike suppression Standard Mode Fast Mode[c]	-	-	 - 50	ns

Table 2-16: I²C Interface characteristics

a. max. valid time (t_{VD}) non-applicable, since device stretches the LOW period (t_{LOW}) of the SCL signal
b. output buffers without slope control for falling edges, use series resistors to slow down falling edges if needed
c. valid for SCL signal, no spike suppression on SDA signal

2.3.4.6 RESET and Boot Strap timing

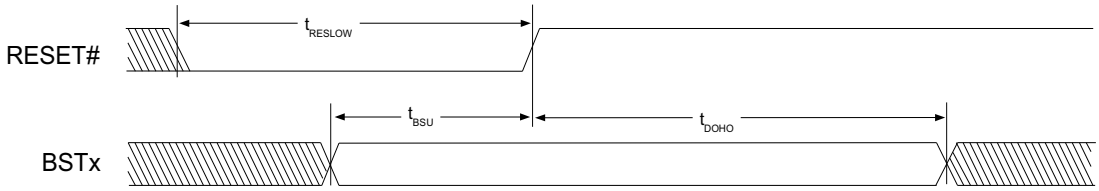


Figure 2-8: Reset and Boot Strap Timing Diagram

For a valid Reset Low Time (t_{RESLOW}) all supply voltages needs to be stable in the operating condition. At reset release (rising edge of RESET#) a stable reference clock is required. All values specified for T_A=25°C.

Parameter	Description	Min.	Typ.	Max.	Units
t_{RESLOW}	Reset Low Time	1	-	-	ms
t_{BSU}	Boot Strap In Setup Time	0	-	-	ns
t_{BHO}	Boot Strap In Hold Time	500	-	-	ns

Table 2-17: Boot Strap Reset Timing

2.3.4.7 GPIO Interface

2.3.4.7.1 GPIO Interface Downstream

The GPIO interface is only available in APIX2 mode. Receiver GPIO downstream interface outputs GPIO data coming from a connected APIX2 transmitter device. Maximum output frequency can be configured using parameters GPIO Bandwidth (gpio_bw_dwn) and GPIO halved (gpio_bw_div). For further information please refer to the INAP395R user manual. All values specified for T_A=25°C.

Downstream Bandwidth	GPIO ports	GPIO Bandwidth	GPIO halved	Maximum Output Frequency	Unit
3 GBit/s	1	high	off	13.260	MHz
3 GBit/s	1	low	off	3.340	MHz
3 GBit/s	1	high	on	6.660	MHz
3 GBit/s	1	low	on	1.670	MHz
3 GBit/s	2	high	off	6.660	MHz
3 GBit/s	2	low	off	1.670	MHz
3 GBit/s	2	high	on	3.330	MHz
3 GBit/s	2	low	on	unsupported	MHz
1 GBit/s	1	high	off	8.450	MHz
1 GBit/s	1	low	off	2.220	MHz
1 GBit/s	1	high	on	4.450	MHz
1 GBit/s	1	low	on	1.110	MHz
1 GBit/s	2	high	off	4.440	MHz
1 GBit/s	2	low	off	1.110	MHz
1 GBit/s	2	high	on	2.220	MHz
1 GBit/s	2	low	on	0.550	MHz
500 MBit/s	1	high	off	8.450	MHz
500 MBit/s	1	low	off	1.110	MHz
500 MBit/s	1	high	on	4.450	MHz
500 MBit/s	1	low	on	1.110	MHz
500 MBit/s	2	high	off	4.440	MHz
500 MBit/s	2	low	off	1.110	MHz
500 MBit/s	2	high	on	2.220	MHz
500 MBit/s	2	low	on	0.550	MHz

Table 2-18: GPIO Interface Downstream

2.3.4.7.2 GPIO interface upstream

At receiver side GPIO data upstream input ports are sampled asynchronously and transmitted to configurable GPIO output ports at transmitter side. Transmitter GPIO upstream interface outputs GPIO data coming from either one or two APIX2 receiver devices. For further informations please refer to the INAP395R user manual. All values specified for T_A=25°C.

Number of Rx	Upstream Bandwidth	GPIO Ports	GPIO Bandwidth	Sampling Frequency	Unit
1	187.5 MBit/s	1	high	13.39	MHz
1	187.5 MBit/s	1	low	3.35	MHz
1	187.5 MBit/s	2	high	13.39	MHz
1	187.5 MBit/s	2	low	3.35	MHz
1	62.5 MBit/s	1	high	4.46	MHz
1	62.5 MBit/s	1	low	1.12	MHz
1	62.5 MBit/s	2	high	4.46	MHz
1	62.5 MBit/s	2	low	1.12	MHz
2	187.5 MBit/s	1	high	6.69	MHz
2	187.5 MBit/s	1	low	3.35	MHz
2	187.5 MBit/s	2	high	6.96	MHz
2	187.5 MBit/s	2	low	3.35	MHz
2	62.5 MBit/s	1	high	2.23	MHz
2	62.5 MBit/s	1	low	1.12	MHz
2	62.5 MBit/s	2	high	2.23	MHz
2	62.5 MBit/s	2	low	1.12	MHz

Table 2-19: GPIO Interface Upstream

2.3.4.8 I²S Audio Interface

f_{BCK} = 1 / t_{PERIOD}. BCK duty cycle D = t_{HIGH} / t_{PERIOD} * 100%. All values specified for T_A=25°C.

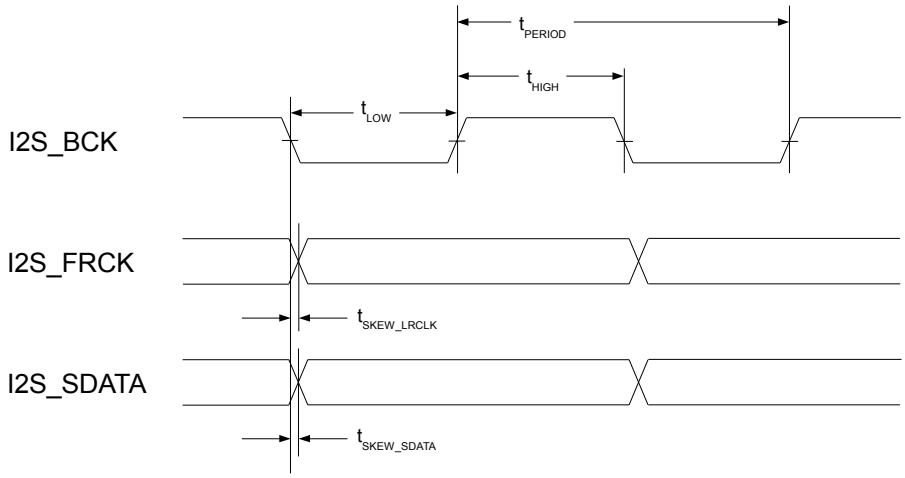


Figure 2-9: I²S Audio Interface Timing Diagram

Parameter	Description	Min	Max	Units
f_{BCK}	I²S_BCK frequency	0.75	25.574	MHz
f_{MCLK}	I²S_MCLK frequency	2.953	93.75	MHz
t_{HIGH}/t_{LOW}	I²S_BCK Duty Cycle	45:55	55:45	% duty cycle
t_{SKEW_FRCK}	Skew between I2S_BCK and I2S_FRCK		5	ns
t_{SKEW_SDATA}	Skew between I2S_BCK and I2S_Data		5	ns

Table 2-20: I²S Audio Interface Timing

2.3.4.9 MII / NIBBLE Interface Timings

f_{MII_CLK} = 1 / t_{PERIOD}. All values specified for T_A=25°C.

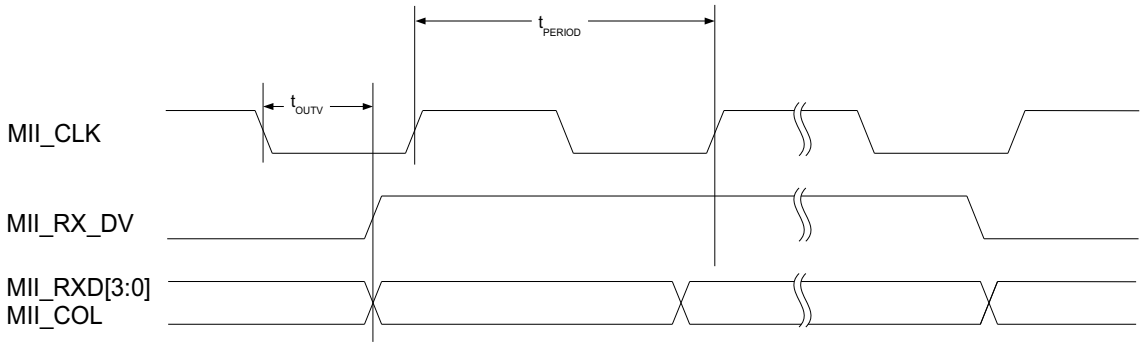


Figure 2-10: MII / NIBBLE Interface Timing Diagram Transmit

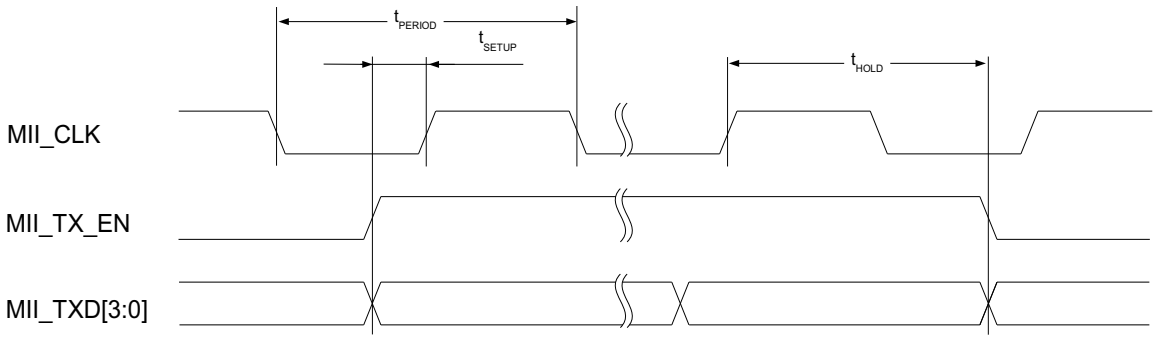


Figure 2-11: MII / NIBBLE Interface Timing Diagram Receive

Parameter	Description	Min	Typ	Max	Units
f_{MII_CLK}	Clock Frequency	3.125	-	93.75	MHz
f_{MII_CLK}	Clock Frequency (100BASE-T)	-	25	-	MHz
t_{SETUP}	Setup Time	9	-	-	ns
t_{HOLD}	Hold Time	0	-	-	ns
t_{OUTV}	Data Output Valid	1	-	7	ns

Table 2-21: MII / NIBBLE Interface Timings

2.3.5 Reference Clock

The INAP395R requires an external clock source like a crystal or oscillator, acting as reference for the internal PLL.

Parameter	Description	Min.	Typ.	Max.	Unit
f_{ref_osc}	Nominal Reference Frequency	-	10	-	MHZ
F_{TOL}	Frequency Tolerance	-100	-	+100	ppm
ESR_{XTAL}	Equivalent Series Resistance	-	-	80	Ohm
	Drive Level	see Table 2-23			

Table 2-22: Reference clock requirements

The INAP395R core clock frequency is generated by an internal PLL controlled by an external 10 MHz crystal. Alternatively a stable 10 MHz clock signal (3.3V CMOS TTL) can be directly connected to XTAL_IN with XTAL_OUT left open. Figure 2-12 shows a typical crystal design required for the oscillator circuit. The values for C1, C2 and R1 need to be selected to match the oscillation requirements of the crystal Q1.

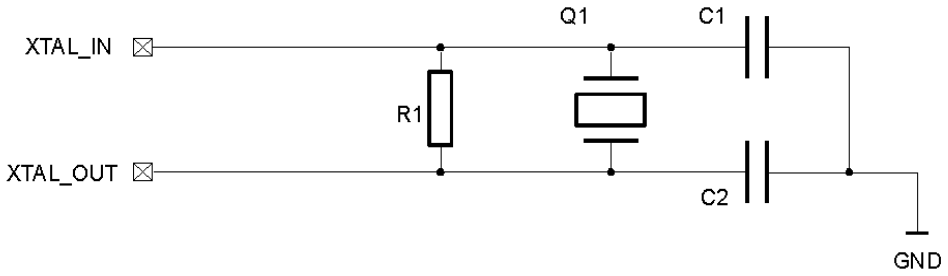


Figure 2-12: Crystal clock schematic example

For resonance at the correct frequency, the crystal needs to be loaded with its specified load capacitance C_L, which is the value of capacitance used in conjunction with the oscillation unit. The INAP395R oscillator provides some of the load with internal capacitance which is specified within the range of 10pF to 12.5pF. The remainder is generated by the external capacitors and tuning capacitors labeled C1 and C2.

The load capacitance C_L can be calculated from $C_L = C_{int}$ + C1//C2. E.g. selecting C1 and C2 with 15pF, C_L can be calculated to C_L = 12.5pF + 7.5pF = 20pF.

The crystal needs to be able to withstand the power dissipation, produced by the INAP395R. The power dissipation depends on the ESR of the crystal and is reflected by the maximum drive level of the crystal. Table 2-23 illustrates the power dissipation of the INAP395R and therefore the minimum drive level capabilities of the crystal at different crystal ESR levels.

Crystal ESR	INAP395R Power dissipation / Minimum crystal drive level	Unit
30	77	µW
50	121	µW
80	179	µW

Table 2-23: Minimum Drive level

2.3.6 Power Up Sequencing

To avoid high IO currents, 1.8V supply voltages have to ramp before 3.3V supply on power-up. On power-down, 3.3V supply have to be powered down before 1.8V. On power-up all supply voltages have to rise steadily from GND level up to the VCC_{MIN} level without turn to negative direction. The ramping times must be within the limits as specified in Table 2-24. All 1.8V supplies have to be ramped up simultaneously starting from GND according Figure 2-13. Reset has to be held low until all supplies reached recommended operating conditions.

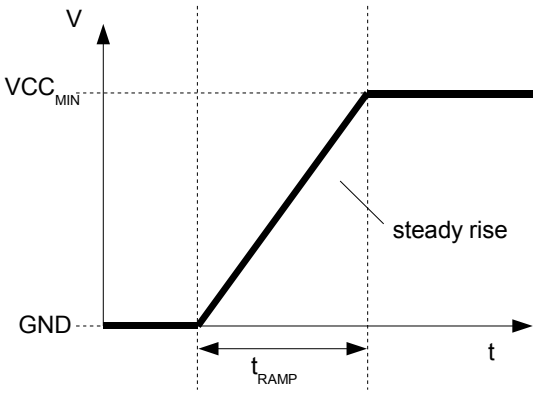


Figure 2-13: Steady voltage ramp-up

Parameter	Description	Min.	Typ.	Max.	Unit
t_{RAMP}	Supply Ramp Up Time for all supplies GND to VCC-min	0.05	1	10	ms

Table 2-24: Power supply ramp-up time

2.4 Typical Operating Characteristics

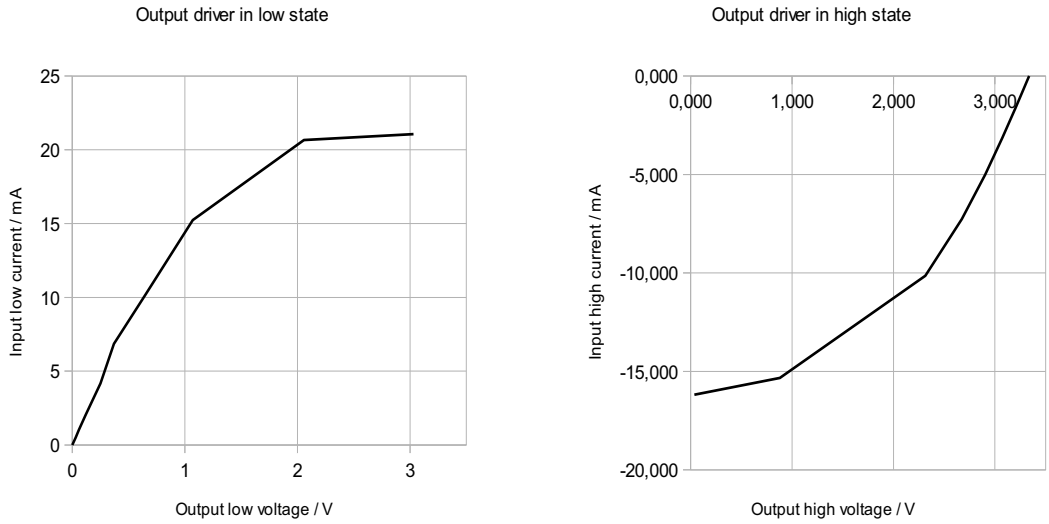


Figure 2-14: typical general IO characteristics

3.0 Pin Description

Signal Name	Pin #	Type	Description
PX[30:1]	82,83,78,79, 80,81,84,85, 73,72,86,75, 74,71,70,1,93, 94,97,98,95, 96,91,92,4,3, 2,5,6,10	O	Video Interface pin
SPI_M_SDO/ MII_CLK/ BST5	11	I/O	SPI_M_SDO: SPI Master Data Output MII_CLK: MII Interface Clock Output BST5: Boot strap option 5 input
SPI_M_SDI/ MII_TX_EN	12	I	SPI_M_SDI: SPI Master Data Input MII_TX_EN: MII Transmit Enable Input
SPI_M_SCK/ MII_RXD1/ BST2	13	I/O	SPI_M_SCK: SPI Master Serial Clock Output MII_RXD1: MII Receive Data Output 1 BST2: Boot strap option 2 input
SPI_M_CS0#/ MII_RXD0	14	O	SPI_M_CS0#: SPI Master Chip-select 0 Output (Data Channel 0) MII_RXD0: MII Receive Data Output 0
SPI_M_CS1#/ MII_RXD3/	15	O	SPI_M_CS1#: SPI Master Chip-select 1 Output (Data Channel 1) MII_RXD3: MII Receive Data Output 3
SPI_M_CS2#	18	O	SPI_M_CS2#: SPI Master Chip-select 2 Output (Configuration)
SPI_S_SDO/ BST3	19	I/O	SPI_S_SDO: SPI Slave Data Output BST3: Boot strap option 3 input
SPI_S_SDI	20	I [a]	SPI Slave Data Input
SPI_S_SCK	21	I [a]	SPI Slave Serial Clock Input
SPI_S_STALL/ MII_STALL MII_COL/ BST4	22	I/O	SPI_S_STALL: High: SPI Slave not ready or buffer full Low: SPI Slave ready to receive data MII_STALL: High: Nibble IF not ready or buffer full Low: Nibble IF ready to receive data MII_COL: MII Collision Detect output BST4: Boot strap option 4 input
SPI_S_CS0#/ MII_TXD0/ SBUP_DATA0	23	I [a]	SPI_S_CS0#: SPI Slave Chip-select 0 Input (Data channel 0) MII_TXD0: MII Transmit Data Input 0 SBUP_DATA0: APIX1 Upstream data input 0

Table 3-1: Pin description

Signal Name	Pin #	Type	Description
SPI_S_CS1#/ MII_TXD1/ SBUP_DATA1	26	I [a]	SPI_S_CS0#: SPI Slave Chip-select 1 input (Data channel 1) MII_TXD1: MII Transmit Data input 1 SBUP_DATA1: APIX1 Upstream data input 1
SPI_S_CS2#	27	I [a]	SPI Slave Chip-select 2 input (Configuration)
SPI_S_RW/ MII_TXD2	28	I	SPI_S_RW: SPI Slave Read/Write input, only used in single SPI mode MII_TXD2: MII Transmit Data Input 2
SPI_S_MB0/ MII_RXD2/ SBDWN_DATA0/ BST1	29	I/O	SPI_S_MB0: SPI Slave mailbox 0 output MII_RXD2: MII Receive Data Output 2 SBDWN_DATA0: APIX1 Downstream data output 0 BST1: Boot strap option 1 input
SPI_S_MB1/ MII_RX_DV/ SBDWN_DATA1/ BST6	30	I/O	SPI_S_MB1: SPI slave mailbox 1 output MII_RX_DV: MII Receive Data Valid output SBDWN_DATA1: APIX1 Downstream data output 1 BST6: Boot strap option 6 input
MII_TXD3	31	I	MII_TXD3: MII Transmit Data Input 3
I2C_SCL/ INBOUND_TS	32	I/O [b]	I2C_SCL: I^2C Clock output INBOUND_TS: Inbound Nibble Data Target select output
I2C_SD/ OUTBOUND_TS	33	I/O [b]	I2C_SD: I^2C Data pin OUTBOUND_TS: Outbound Nibble Data Target select input
SD_UP_IN_P	36	I [c]	Serial Link, Upstream Serial Link Input from 2^{nd} RX
SD_UP_IN_N	37	I [c]	Serial Link, Upstream Serial Link Input from 2^{nd} RX
SD_DWN_OUT_N	39	O [c]	Serial Link, Downstream Serial Link output to 2^{nd} RX
SD_DWN_OUT_P	40	O [c]	Serial Link, Downstream Serial Link output to 2^{nd} RX
SD_DWN_IN_P	43	I [c]	Serial Link, Downstream Serial Link input from TX
SD_DWN_IN_P	44	I [c]	Serial Link, Downstream Serial Link input from TX
SD_UP_OUT_N	49	O [c]	Serial Link, Upstream Serial Link output to TX
SD_UP_OUT_P	50	O [c]	Serial Link, Upstream Serial Link output to TX
XTAL_IN	52	I	10MHz Oscillator input
XTAL_OUT	53	O	10MHz Oscillator output
I2S_FRCK	56	O	I^2S Interface, Frame clock output
I2S_BCK	57	O	I^2S Interface, Bit clock output
I2S_SDATA	58	O	I^2S Interface, Data output

Table 3-1: Pin description

Signal Name	Pin #	Type	Description
I2S_MCLK	61	O	I^2S Interface, Master Clock output
GPIO1/SBDWN_CLK	62	I/O	GPIO1: General purpose I/O SBDWN_CLK: Sampling clock output for SBDWN_DATA[1:0] (APIX1 Mode) DEBUG Interface: Debug Output Pin1
GPIO0	63	I/O	GPIO0: General purpose I/O DEBUG Interface: Debug Output Pin0
STATUS	64	O	STATUS: Device status output
RESET#	66	I [d]	Reset
DVDD	7,24,69,77,99	Power	Digital I/O power supply
AVDD_LVDS_PLL	87	Power	LVDS PLL power supply
VDD	17,35,59, 89	Power	Core supply
AVDD_LVDS	9,67	Power	LVDS I/O power supply
AVDD	45,48	Power	Serial Link core power supply
AVDD_VCO	47	Power	Serial Link VCO Power supply
VDD_XTAL	54	Power	10MHz Oscillator core supply
DVDD_XTAL	55	Power	10MHz Oscillator digital supply
GND_XTAL	51	GND	10MHz Oscillator Ground
GND	8,16,25,34,38, 42,46,60,68, 76,88,90, 100	GND	Ground
Exposed PAD (EP)	-	GND	must be connected to GND-plane
TEST	65	I [a]	reserved, pull down external over 100kOhm to GND
AVDD_LD	41	O	Common Mode voltage, connect to decoupling capacitor (1µF), not a power supply pin!!

Table 3-1: Pin description

a. with internal pull-down
b. n-channel open drain
c. CML interface
d. schmitt trigger input

3.1 Reset

The pin RESET# triggers an asynchronous reset (active low) and can be activated any time. This reset erases all configuration settings. Please see Table 3-2 for the status of all pins during reset.

Signal Name	Reset State	Functional State
PX[30:1]	Tri-State	Output
SPI_M_SDO / MII_CLK / BST5	Input	Output
SPI_M_SDI / MII_TX_EN	Input	Input
SPI_M_SCK / MII_RXD1 / BST2	Input	Output
SPI_M_CS0# / MII_RXD0	Output	Output
SPI_M_CS1# / MII_RXD3/	Output	Output
SPI_M_CS2#	Output	Output
SPI_S_SDO / BST3	Input	Output
SPI_S_SDI	Input	Input
SPI_S_SCK	Input	Input
SPI_S_STALL / MII_COL / BST4	Input	Output
SPI_S_CS0# / MII_TXD0 / SBDWN_DATA0	Input	Input
SPI_S_CS1# / MII_TXD1 / SBDWN_DATA1	Input	Input
SPI_S_CS2#	Input	Input
SPI_S_RW / MII_TXD2	Input	Input
SPI_S_MB0 / MII_RXD2 / SBUP_DATA0 / BST1	Input	Output
SPI_S_MB1 / MII_RX_DV / SBUP_DATA1 / BST6	Input	Output
MII_TXD3	Input	Input
I2C_SCL / INBOUND_TS	Tri-State	Tri-State / Output
I2C_SD / OUTBOUND_TS	Tri-State	Tri-State / Input / Output
I2S_FRCK	Output	Output
I2S_BCK	Output	Output
I2S_SDATA	Output	Output
I2S_MCLK	Tri-State	Tri-State / Output

Table 3-2: Reset States

Signal Name	Reset State	Functional State
GPIO1 / SBDWN_CLK	Input	Input / Output
GPIO0 / SBUP_CLK	Input	Input / Output
STATUS	Output	Output

Table 3-2: Reset States

4.0 Package Information

4.1 Pinout Diagram

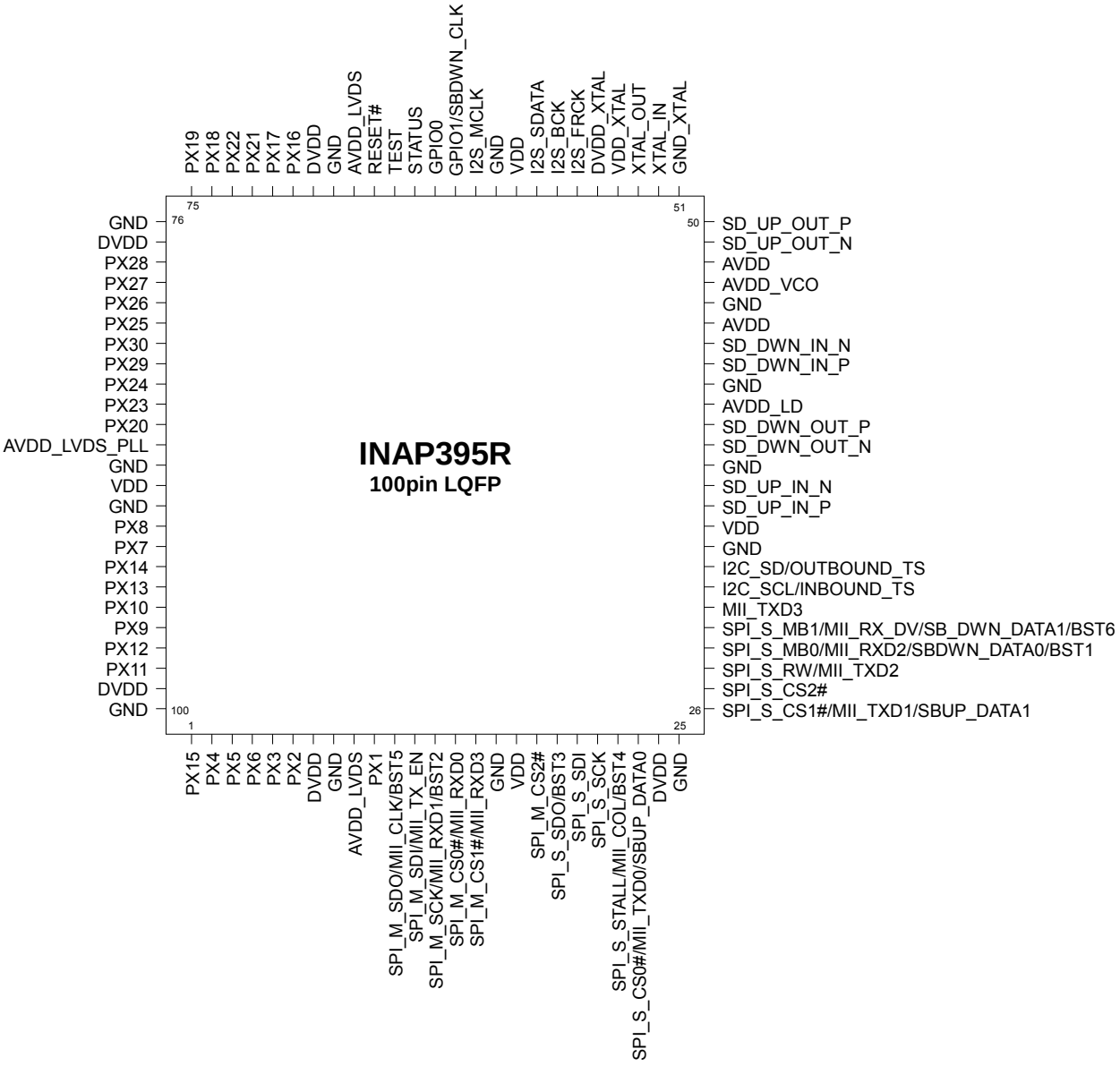
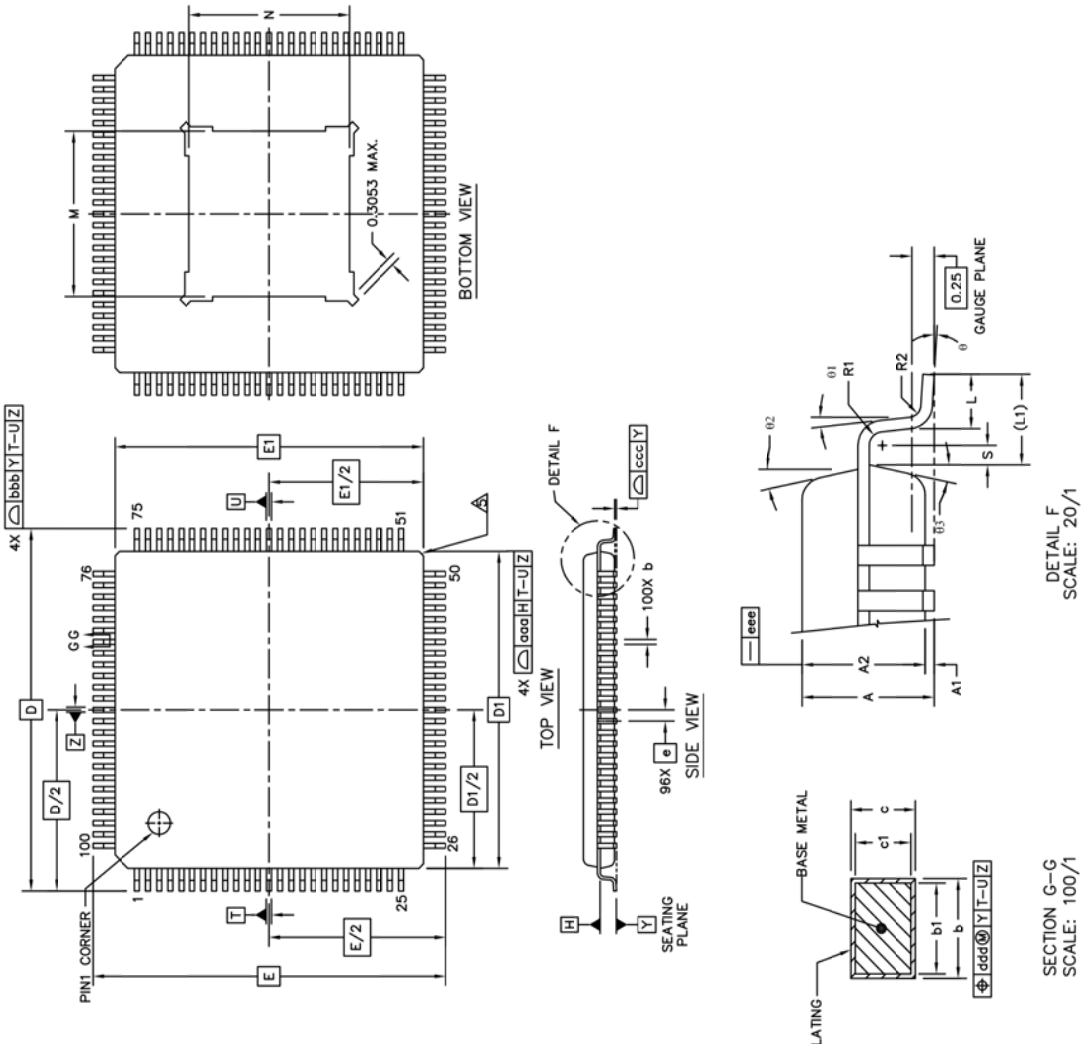


Figure 4-1: Pinout diagram, 100pin LQFP

* Exposed PAD connect to GND-plane

4.2 Package Dimensions

SYMBOL		MIN	NOM	MAX
TOTAL THICKNESS	A	---	---	1.6
STAND OFF	A1	0.05	---	0.15
MOLD THICKNESS	A2	1.35	1.4	1.45
LEAD WIDTH(PLATING)	b	0.17	0.22	0.27
LEAD WIDTH	b1	0.17	0.2	0.23
L/F THICKNESS(PLATING)	c	0.09	---	0.2
L/F THICKNESS	c1	0.09	---	0.16
BODY SIZE	X	D	16 BSC	
	Y	E	16 BSC	
	X	D1	14 BSC	
	Y	E1	14 BSC	
LEAD PITCH		e	0.5 BSC	
		L	0.45	0.6	0.75
FOOTPRINT		L1		1 REF	
		θ	0°	3.5°	7°
		θ1	0°	---	---
		θ2	11°	12°	13°
		θ3	11°	12°	13°
		R1	0.08	---	---
		R2	0.08	---	0.2
		S	0.2	---	---
EP SIZE	X	M	7.2	7.3	7.4
	Y	N	7.2	7.3	7.4
PACKAGE EDGE TOLERANCE		aaa		0.2	
LEAD EDGE TOLERANCE		bbb		0.2	
COPLANARITY		ccc		0.08	
LEAD OFFSET		ddd		0.08	
MOLD FLATNESS		eee		0.05	



5.0 Bibliography

[1] – openLDI Specification, National Semiconductor, Rev. 0.95

[2] – INAP395R User Manual

6.0 Revision History

Revision	Date	Changes
0.1	August 2012	Initial Preliminary Datasheet Release
1.0	March 2015	Updated to characterization data

Table 6-1: Revision History

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