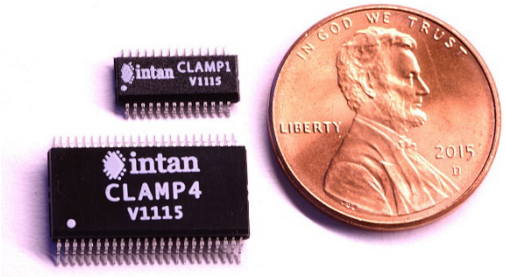
CLAMP1
CLAMP4

Voltage/Current Clamp Amplifier Chips



26 August 2016

Features

- Fully integrated current-sensing voltage clamp amplifiers and voltage-sensing current clamp amplifiers with industry-standard serial peripheral interface (SPI)
- Voltage clamp operation holds electrode potential while sensing current in the picoamp to microamp range
- Low input-referred current noise: 2.1 pA_{rms} over 5 kHz bandwidth using CLAMP1 at highest sensitivity
- Current clamp operation sources or sinks constant current through electrode while sensing voltage in the microvolt to millivolt range
- Low input-referred voltage noise: 12 μV_{rms} over 10 kHz bandwidth using CLAMP1 at highest sensitivity
- Fast transient capacitance compensation: 0-20 pF range
- Seamless operation with industry-standard 16- or 18-bit ADC; CLAMP chip provides all control signals
- Available with one voltage/current clamp (CLAMP1) or four independent voltage/current clamps (CLAMP4)

Applications

- Miniaturized headstages for patch clamp electrophysiology and intracellular recording
- High-throughput planar patch clamp for pharmacological screening
- Electronics for nanopore sequencing
- Lipid bilayer membrane amplifiers
- Current sensing from arrays of FET sensors or photodiodes
- Fast-scan cyclic voltammetry (FSCV) for the detection of neurotransmitters and other organic molecules
- Amperometry for electrochemical detection

Description

The Intan Technologies CLAMP microchips are integrated precision instruments capable of voltage clamp and current clamp operation. All analog instrumentation required for traditional “patch clamp” electrophysiological experiments is integrated onto a single piece of silicon. Electrodes or other sensors are connected to one side of the chip, and digitized data is read from a serial bus on the other side. The chip is configured and controlled through this standard serial peripheral interface (SPI) bus.

The CLAMP1 and CLAMP4 chips contain one and four Clamp Units, respectively. Each Clamp Unit can act as a voltage clamp amplifier or a current clamp amplifier. Voltage clamp operation holds the electrode potential at desired levels while sensing the resulting current waveform. Current clamp operation sources or sinks current through the electrode while sensing the resulting voltage waveform.

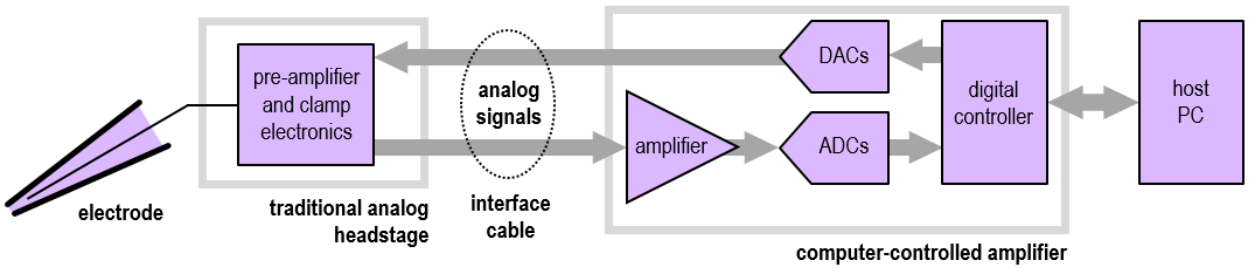
The clamp voltage range is wide enough (±1.275V) to support both intracellular recordings and electrochemical measurements such as amperometry or fast-scan cyclic voltammetry (FSCV). A low noise floor (2.1 pA_{rms} in the most sensitive range) allows tiny membrane currents to be resolved.

The current clamp can produce currents up to ±127 nA with step sizes as small as 5 pA. This allows for flexible delivery of currents while observing voltages across a wide ±300 mV range with a noise floor as low as 12 μV_{rms}.

The CLAMP1 chip is packaged in a standard 28-pin SSOP surface mount package; the CLAMP4 chip is packaged in a 48-pin SSOP. Each CLAMP chip uses an industry-standard external ADC and a small number of passive support components to form a complete electrode-to-digital interface. The small footprint and low power consumption of the CLAMP chips enable the miniaturization of front end electronics for miniature patch clamp headstages, high-throughput planar patch clamp instruments, and other electrophysiological and electrochemical sensors.

System Architecture

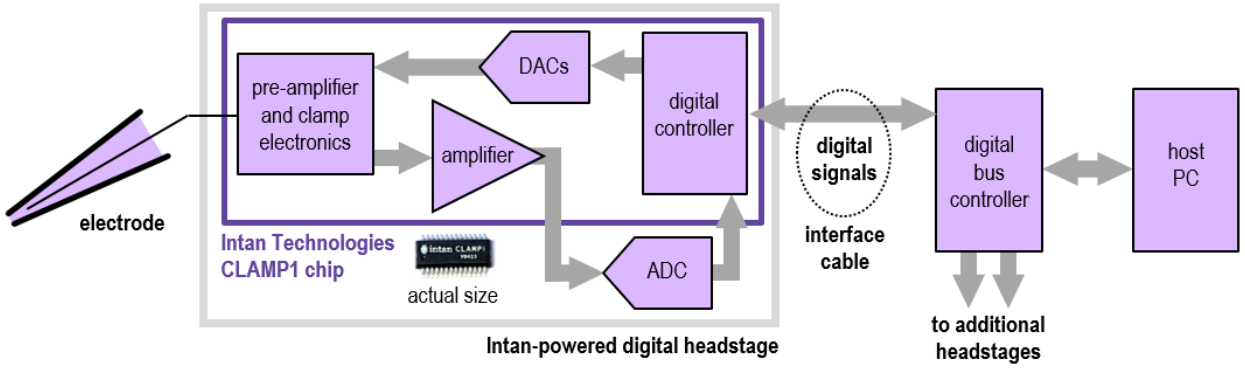
Traditional Analog Patch Clamp Amplifier



The diagram above shows the major functional components of a traditional patch clamp amplifier system. A **traditional analog headstage** module contains sensitive analog electronics that act as a pre-amplifier with voltage clamp and current clamp capability. In voltage clamp mode, the headstage measures the electrode current and converts this to a proportional small voltage. In current clamp mode, the headstage buffers the electrode voltage but provides no additional amplification. Voltage and current clamp control is provided by analog voltages that indicate the desired clamping levels.

The headstage is connected to a remote **computer-controlled amplifier** via a shielded **interface cable** that carries small analog voltages (typically in the millivolt range) and is thus susceptible to noise pickup. The amplifier module is a rack-mounted box that contains additional analog **amplifiers**, analog-to-digital converters (**ADCs**), digital-to-analog converters (**DACs**), and a **digital controller** that coordinates control of these devices. The amplifier module is interfaced to a **host PC** that sequences particular experiments and records the resulting data.

Intan-Powered Digital Patch Clamp Amplifier

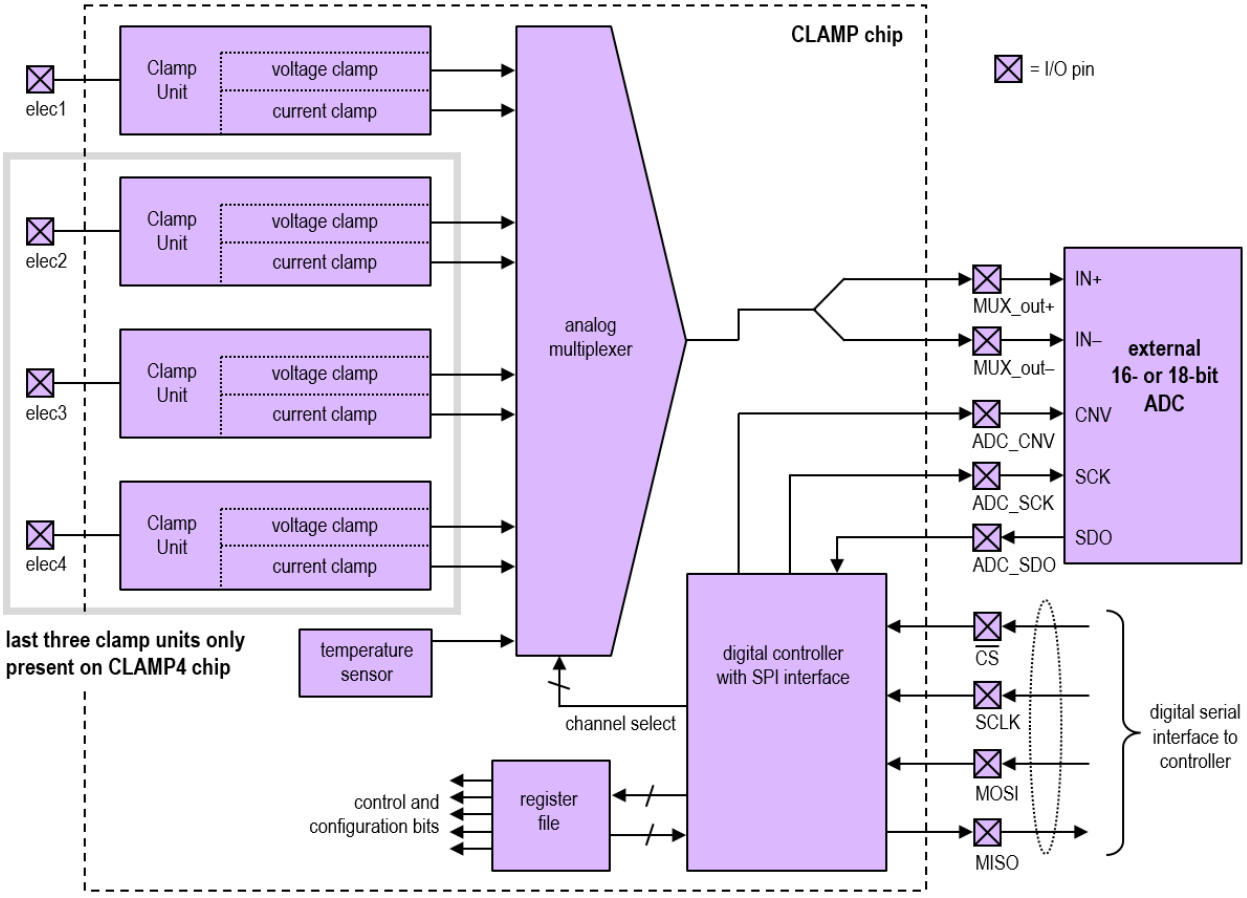


The CLAMP chips from Intan Technologies combine all analog circuitry and many digital control blocks on a single chip, permitting the construction of **Intan-powered digital headstages** (see diagram above). A small circuit board containing an Intan CLAMP chip, a single ADC, and a small number of support components form a complete patch clamp amplifier with a purely digital interface. **The Intan-powered digital "headstage" is actually a complete, miniaturized patch clamp amplifier.** Thanks to the integration of nearly all patch clamp circuit elements onto a single silicon chip (see "actual size" inset above), the Intan-powered patch clamp amplifier can be smaller than many traditional analog headstages that perform only a small fraction of the total amplification task.

The digital interface cable uses a standard serial communication protocol (SPI) supported by nearly all microcontrollers, and is no longer susceptible to noise pickup. Sensitive analog signals are digitized at the source, not several meters away. The need for a large computer-controlled amplifier module is completely eliminated, replaced by a simple **digital bus controller** (typically a microcontroller or FPGA) that can easily control many digital headstages simultaneously.

If the CLAMP1 chip shown above is replaced with a CLAMP4 chip then each headstage can perform independent voltage clamp and current clamp measurements on four different electrodes simultaneously. Controlling multiple CLAMP4 chips with a digital bus controller allows for the construction of compact, inexpensive, high-channel-count patch clamp amplifiers for sophisticated electrophysiological experiments or automated pharmacological screening systems.

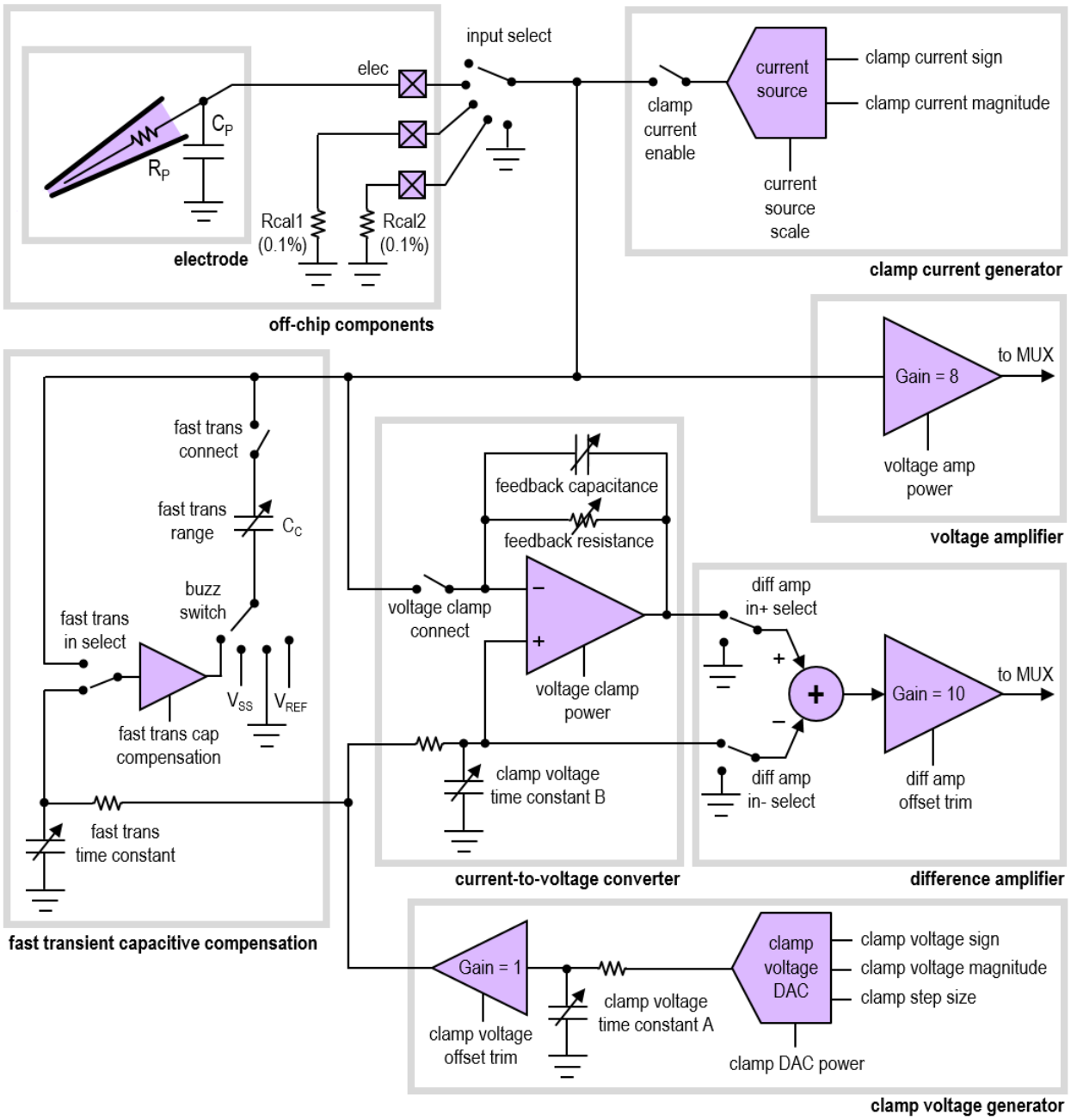
Chip Diagram



Each CLAMP chip contains one or four Clamp Units which are capable of acting as a voltage clamp (setting electrode voltage and measuring current) or a current clamp (setting electrode current and measuring voltage). Each clamp unit amplifies tiny electrode currents and voltages (and converts currents into a proportionally scaled voltage) and passes these amplified voltages through an analog multiplexer (MUX) to a shared external analog-to-digital converter (ADC). The CLAMP chip controls the industry-standard 16- or 18-bit ADC and directs the selected signals through the analog MUX to be digitized. The digital output from the ADC is read back into the CLAMP chip and returned over a single digital SPI interface. This bidirectional serial bus is used to configure and control the CLAMP chip (by means of an on-chip array of registers) and to read the digitized currents and voltages.

The simplified block diagram above shows the organization of these functional blocks, along with relevant I/O pins. The CLAMP1 chip contains a single Clamp Unit while the CLAMP4 chip contains four Clamp Units.

Clamp Unit Diagram

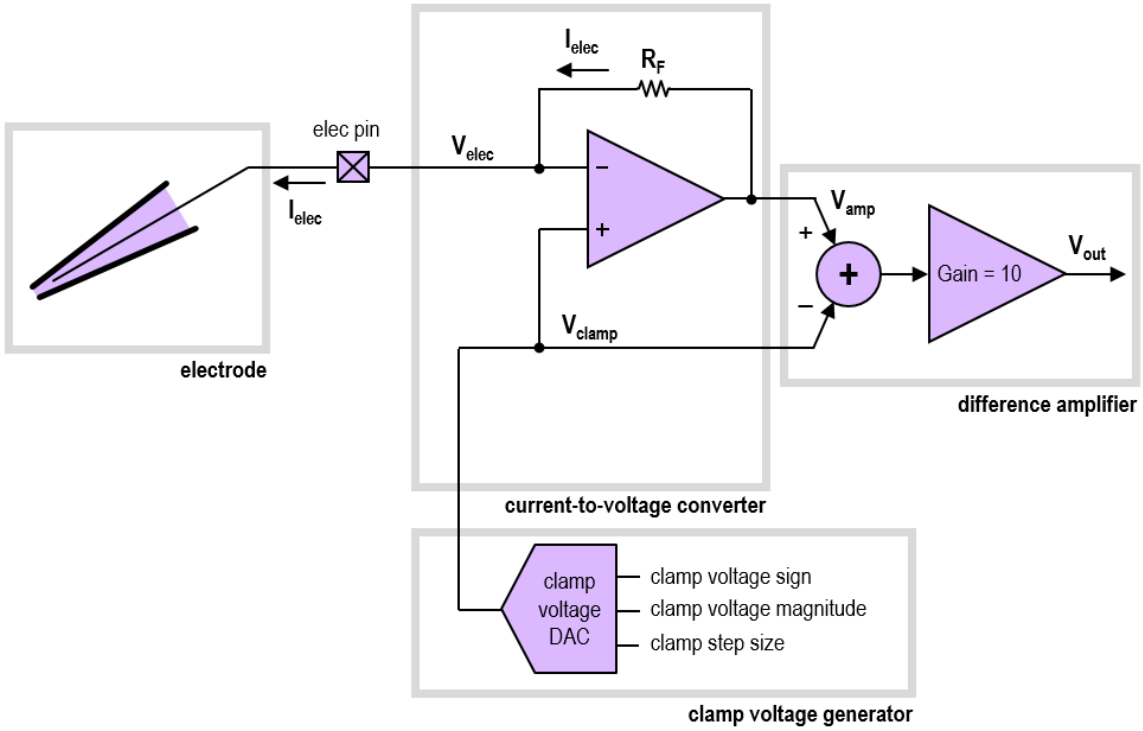


Each CLAMP chip contains one or four Clamp Units (see previous page). Each Clamp Unit, diagrammed below, contains voltage clamp and current clamp circuitry. An electrode (or other sensor) is connected directly to the Clamp Unit, and two precision resistors (Rcal1 and Rcal2) may be added for self-calibration procedures described later. The electrode voltage (in current clamp mode) or current (in voltage clamp mode) is measured and passed to an analog multiplexer (MUX) that connects a selected signal to a shared analog-to-digital converter (ADC).

Voltage clamp capability is provided by a **clamp voltage generator**, a **current-to-voltage converter**, and a **difference amplifier**. Current clamp capability is provided by a **current clamp generator** and a **voltage amplifier**. An optional **fast transient capacitive compensation** circuit can be used in either voltage clamp or current clamp mode, or it can provide a "buzz" function to facilitate cell penetration. The operation of these components is described in detail in the following sections.

Theory of Operation: Voltage Clamp

Referring to the detailed diagram on page 4, a Clamp Unit is placed into voltage clamp mode by setting the **input select** switch to the electrode pin, opening the **current clamp enable** switch, and closing the **voltage clamp connect** switch. (See the Switching Between Voltage Clamp and Current Clamp section for more details.) If we ignore the fast transient capacitive compensation circuit for now, the following simplified diagram shows the relevant circuit modules of a Clamp Unit configured as a voltage clamp.



The core of the voltage clamp is a low-noise operational amplifier (op amp) configured as a **current-to-voltage converter**. A resistor R_F provides negative feedback, ensuring that the electrode voltage V_{elec} is driven to the same potential as the positive input of the op amp (V_{clamp}), which is generated by the digital-to-analog converter (DAC) in the **clamp voltage generator**.

Any current I_{elec} flowing through the electrode must flow through R_F since the op amp inputs draw no current. This generates a voltage $R_F I_{elec}$ across the feedback resistor. Since V_{elec} is held equal to V_{clamp} by feedback, the output of the op amp V_{amp} is equal to $V_{clamp} + R_F I_{elec}$. A **difference amplifier** subtracts V_{clamp} from V_{amp} and amplifies the signal by a factor of 10, producing an output V_{out} equal to $10 \cdot R_F I_{elec}$. Since R_F is known, the electrode current I_{elec} is easily derived from the output voltage that is digitized by the ADC.

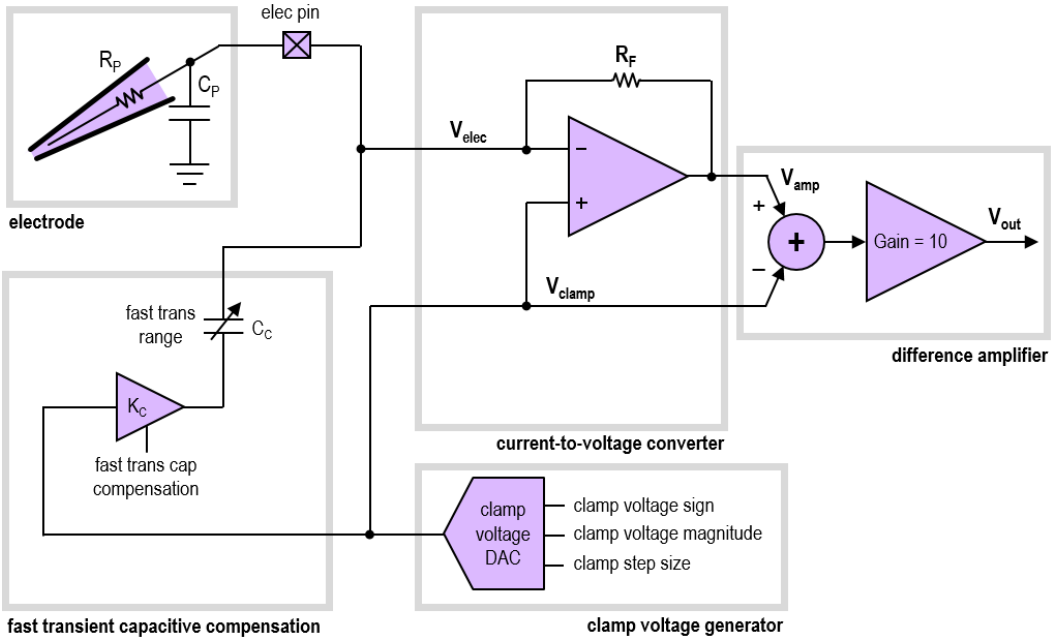
Each clamp voltage generator contains a 9-bit clamp voltage DAC that can be configured with a step size of 2.5 mV (for a range of ±637.5 mV) or 5.0 mV (for a range of ±1.275 V). The value of the feedback resistor R_F can also be set to one of five different values: 200 kΩ, 2 MΩ, 20 MΩ, 40 MΩ, or 80 MΩ. Larger values of R_F lower the noise floor for current measurement but reduce the range of currents than can be sensed. The difference amplifier has linear behavior for output voltages in the range of ±2.4 V. This limits the voltage across R_F that can be sensed to ±0.24 V. With R_F set to 80 MΩ the current measurement range is limited to ±3.0 nA. If R_F is set to its minimum value of 200 kΩ the measurement range extends to ±1.2 µA, but the noise floor is higher.

As shown in the detailed Clamp Unit diagram on page 4, a variable feedback capacitor C_F is tied in parallel with R_F. This capacitor can be set to values ranging from zero to 51 pF in 0.2 pF steps. It limits the bandwidth of the current-to-voltage converter to a frequency of $1 / (2\pi \cdot R_F C_F)$, which is useful for reducing noise and preventing aliasing during ADC sampling. C_F is typically adjusted to limit the bandwidth of the current-to-voltage converter to 10 kHz.

The detailed Clamp Unit diagram also shows variable RC low-pass filters that set clamp voltage time constants A and B. These filters are used to smooth the sharp transitions between clamp voltage steps and limit the magnitude of transient electrode currents.

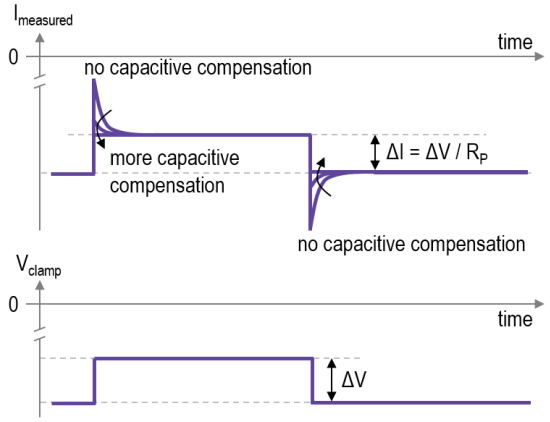
Voltage Clamp with Capacitive Compensation

Real electrodes, particularly glass pipette electrodes used in patch clamp electrophysiology, have undesired but unavoidable electrical properties: parasitic capacitance (labeled C_P below) and series resistance (labeled R_P). The parasitic capacitance C_P typically falls in the range of 5-15 pF and produces fast transient current artifacts when the voltage clamp is stepped from one voltage to another and this capacitance is charged or discharged. Each Clamp Unit contains a **fast transient capacitive compensation** module that can reduce or eliminate these artifacts.



As shown above, the fast transient capacitive compensation module consists of a variable-gain amplifier (with gain K_C) and a compensation capacitor C_C that is internally connected to the electrode pin. When the clamp voltage V_{clamp} switches from one level to another, the electrode voltage V_{elec} follows, with the op amp providing (through R_F) any current required to make V_{elec} track V_{clamp}. With no capacitive compensation, the op amp must supply transient bursts of current to charge and discharge C_P, shown in the plot below. The compensation circuit applies an amplified version of V_{clamp} to C_C, which injects a transient current onto the V_{elec} node. If the gain of the compensation amplifier is set correctly then this injected current can cancel out the current pulled by C_P in response to the electrode voltage change.

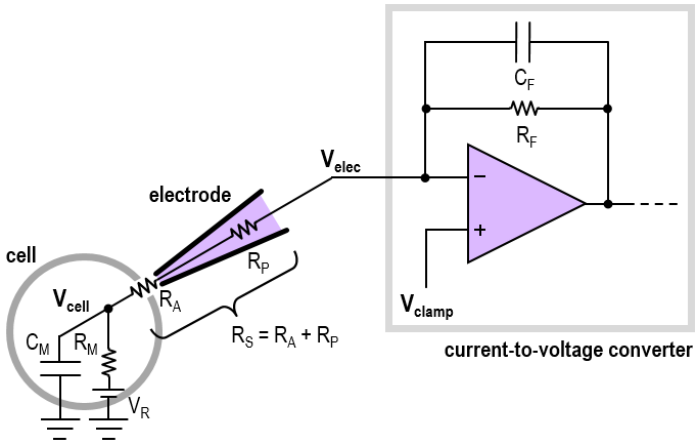
It can be shown that perfect cancellation is achieved when the compensation amplifier gain K_C is equal to $C_P/C_C + 1$. Each CLAMP chip has a range of values for K_C and C_C to support cancellation of C_P in the range of 0-20 pF. In practice, fast transient capacitive compensation is usually tuned when the pipette is placed into bath, before contact with a cell is made. As shown in the plot below, a voltage step is applied to the electrode and the capacitive compensation is adjusted to eliminate the transient peaks in the measured current. The pipette series resistance R_P is easily measured during this procedure as well. Note that excessive compensation ($K_C > C_P/C_C + 1$) can cause increased noise levels and instability.



Using Voltage Clamp to Estimate Membrane Parameters

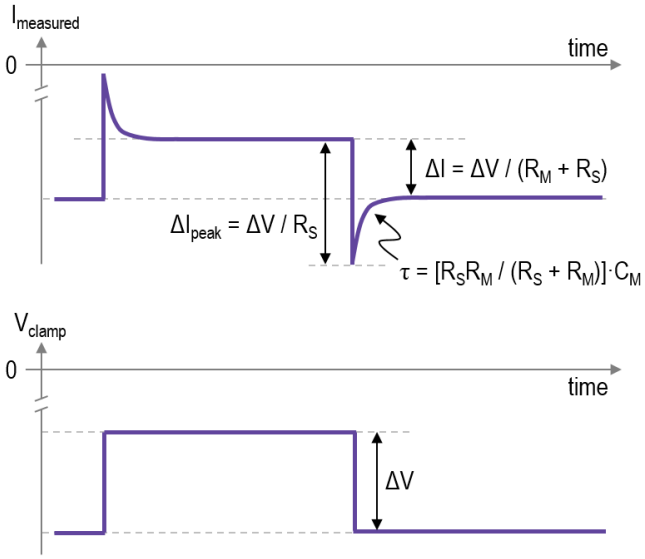
In whole-cell patch clamp electrophysiology, the electrode is electrically connected to the inside of a cell as shown in the diagram below. The tiny opening in the cell membrane creates a large access resistance R_A which adds to the pipette resistance R_P. The resulting series resistance R_S can have a value in the tens of megohms. To first order, the cell's membrane behaves as a capacitance C_M (typically in the tens of picofarads) with some parallel resistance R_M (typically in the hundreds of megohms) in series with a reversal potential V_R (usually in the range of -30 mV to -90 mV). These membrane parameters, as well as the series resistance R_S, can be estimated using a simple voltage clamp measurement.

Note that the electrode parasitic capacitance C_P is not shown in the diagram below because it is assumed that this element has already been cancelled by the fast transient capacitance compensation circuitry prior to cell contact.



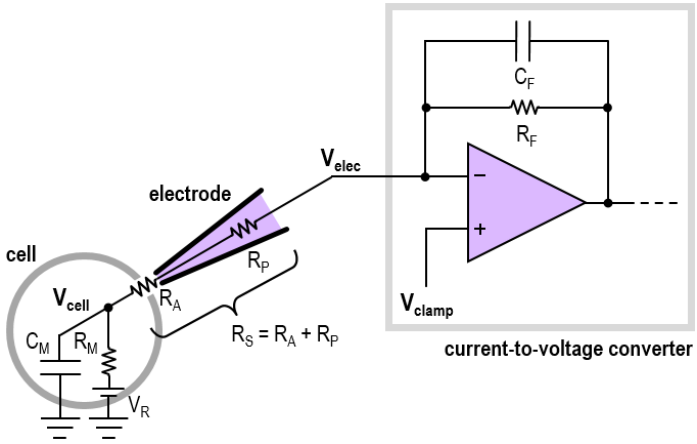
After breaking into a cell, the voltage clamp is typically set to a value near the cell's expected resting potential (e.g., -70 mV) to prevent the activation of voltage-gated ion channels. A small voltage step is applied around this potential (e.g., a step from -70 mV to -60 mV) and the resulting current is measured. The plot below shows a typical clamp voltage profile and measured current waveform. The current takes the form of a decaying exponential with a time constant τ: $i(t) = I_0 \cdot \exp(-t/\tau) + I_1$. (These exponential current peaks are much wider and slower than the "fast transient" peaks caused by uncompensated electrode capacitance C_P; see page 6.)

If an exponential curve is fit to the data, the membrane parameters R_M and C_M can be estimated, along with the series resistance R_S. (It is best to calculate ΔI_{peak} using the exponential fit instead of the raw data, since the exact amplitude of the current peak is sensitive to second-order effects like amplifier bandwidth and noise.) The cell's reversal potential V_R can be estimated as $V_{clamp} - I_{measured} \cdot (R_S + R_M)$, assuming the electrode forms a tight gigaseal to the cell with negligible leakage to the bath.



Voltage Clamp and Series Resistance Compensation

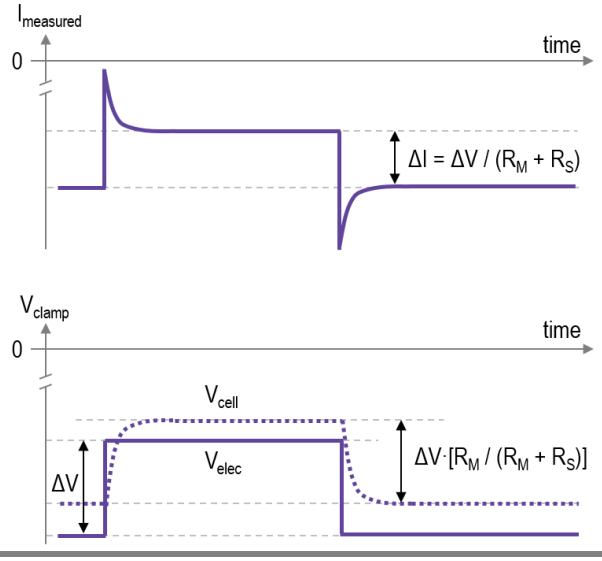
The electrode resistance R_P and cell access resistance R_A form a series resistance R_S that has typical values in the range of 5-50 MΩ. During voltage clamp measurements, any whole-cell current flowing through the electrode causes a voltage drop across this resistance equal to $I_{elec}R_S$. This causes the intracellular voltage V_{cell} to deviate from the desired clamp voltage $V_{elec} = V_{clamp}$. Currents can reach the low nanoamp range in some cells, causing voltage drops across the electrode of 10 mV or more.



Assuming the series resistance R_S has been measured using the techniques described on the previous page, the voltage drop across the electrode can be calculated from the measured current. Traditional patch clamp amplifiers often include a series resistance compensation circuit that uses feedback to shift the clamp voltage higher or lower in real time to compensate for the instantaneous voltage drop across the electrode. This method employs positive feedback, and care must be taken to prevent oscillations; typically, only a fraction of the total series resistance is compensated. Additionally, the speed of the feedback loop must be limited to ensure stability, so rapid voltage drops across the electrode (caused by rapid current pulses in the cell) go largely uncompensated.

The CLAMP chips do not contain series resistance compensation circuitry. In theory, one could implement a compensatory feedback loop using the real time current measurements to adjust the clamp voltage generator. In practice, the minimum step size of the clamp voltage DAC (2.5 mV) is too large to provide smooth feedback. Even though real-time series resistance compensation is not implemented on the CLAMP chips, the actual intracellular voltage V_{cell} may be calculated in real time using the clamp voltage, the measured current, and the value of R_S.: $V_{cell} = V_{clamp} – I_{measured}R_S$.

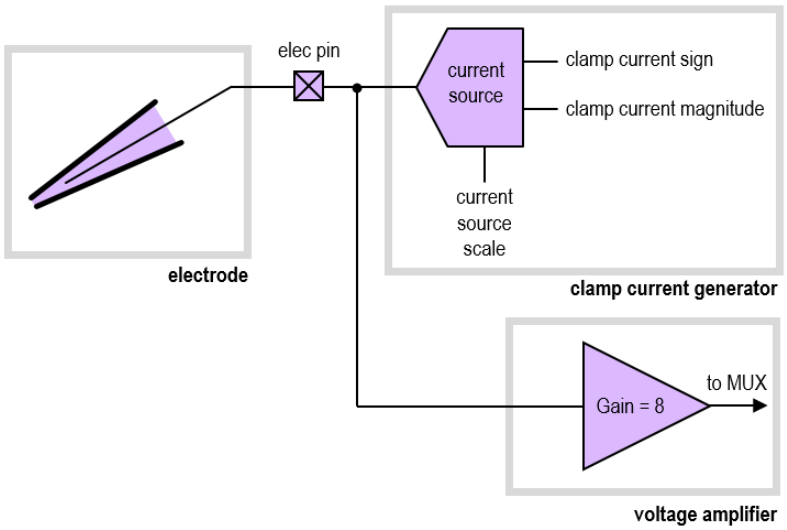
If the cell membrane parameters are estimated using the techniques described on the previous page then a form of “predictive” series resistance compensation can be implemented. The plot below shows the effects of finite series resistance a typical voltage clamp measurement. The actual intracellular voltage is attenuated from the desired clamp voltage by a factor of $R_M / (R_M + R_S)$.



If R_M and R_S have been previously measured then the clamp voltage levels can be adjusted to produce the desired intracellular voltage. This technique is limited by the fact that R_M can change dynamically in response to voltage-gated or ligand-gated ion channels. However, even traditional series resistance compensation is limited in its ability to respond to rapid changes in membrane current.

Theory of Operation: Current Clamp

Referring to the detailed diagram on page 4, a Clamp Unit is placed into current clamp mode by setting the **input select** switch to the electrode pin, closing the **current clamp enable** switch, and opening the **voltage clamp connect** switch. (See the Switching Between Voltage Clamp and Current Clamp section for more details.) If we ignore the fast transient capacitive compensation circuit for now, the following simplified diagram shows the relevant circuit modules of a Clamp Unit configured as a current clamp.



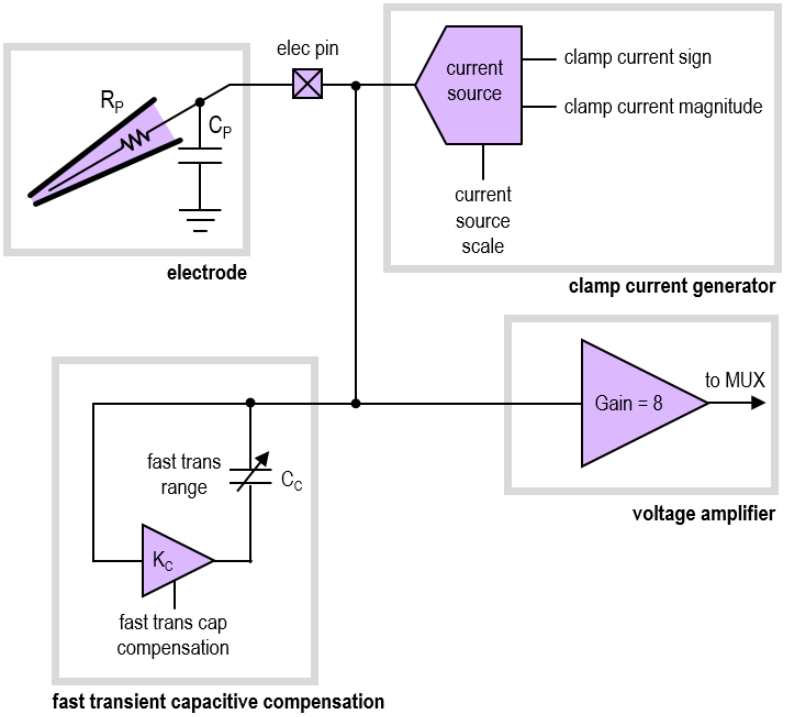
The **clamp current generator** consists of a programmable current source that forces current into or out of the electrode. A low-noise **voltage amplifier** draws no input current and provides a modest gain of 8 to boost the signal before digitization by the ADC.

The current source consists of a current-output DAC with 7-bit magnitude control and 1-bit sign to select positive or negative current. The scale of the current source can be adjusted to set step sizes ranging from 5 pA (for a range of ±635 pA) to 1 nA (for a range of ±127 nA).

The voltage amplifier can has linear behavior for output voltages in the range of ±2.4 V. With its gain of 8, this limits the range of electrode voltages that can be sensed to ±300 mV. The noise floor of the voltage amplifier is 12 μV_{rms} over a bandwidth of 10 kHz.

Current Clamp with Capacitive Compensation

As discussed on page 6, real electrodes have unavoidable parasitic capacitances (denoted C_P in the diagram below) and series resistances (R_P). In current clamp operation, these elements create an RC low-pass filter that attenuates high-frequency components of the membrane voltage that is being measured.



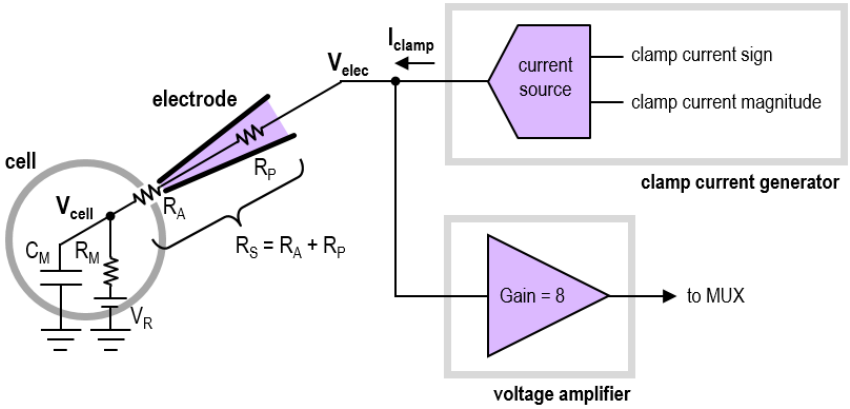
For glass pipette patch clamp electrodes, C_P typically falls in the range of 5-15 pF and R_P lies between 3-8 MΩ (and the access resistance in whole-cell recording can add to this series resistance significantly). Assuming values of C_P = 10 pF and R_P = 6 MΩ gives us a low-pass filter with a cutoff frequency of $1 / (2\pi \cdot R_P C_P)$ = 2.7 kHz, well below the 10 kHz bandwidth often used for cell membrane recordings.

Luckily this parasitic capacitance can be neutralized by using the **fast transient capacitance compensation** circuit first introduced on page 6, but with the compensation amplifier input tied to the electrode pin internally. If the compensation gain K_C is set to C_P/C_C + 1 then the effective capacitance on the electrode pin is reduced to zero. Care must be taken when adjusting this parameter, however, because this compensation technique uses positive feedback which can create large voltage oscillations that will likely damage a cell if the compensation is set too high (creating an effective negative capacitance on the electrode pin).

It is also important to note that the optimum compensation setting in current clamp mode will not, in general, be the same as the optimum compensation setting in voltage clamp mode. This is due to the small change in capacitance on the electrode pin node caused by opening and closing the **current clamp enable** switch and the **voltage clamp connect** switch. A compensation setting 0.60 pF lower is needed for current clamp mode. The optimum compensation value obtained in voltage clamp mode will typically cause oscillations in current clamp mode.

Current Clamp and Bridge Balance

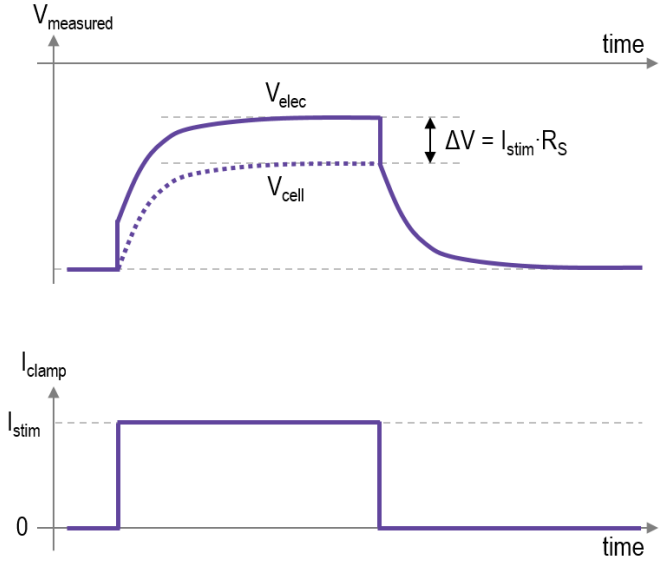
When applying current pulses through real electrodes connected to cells, the measured membrane potential is corrupted by an artifact caused by the voltage drop across the electrode. Referring to the diagram below, we would like to apply a current signal I_{clamp} and measure an electrode voltage V_{elec} equal to the intracellular potential V_{cell}. However, the clamp current flows through a series resistance R_S comprised of the pipette resistance R_P and the access resistance R_A. This leads to a voltage offset ΔV that is equal to $I_{clamp} \cdot R_S$.



The plot below shows an example of this phenomenon for a simple clamp current that starts at zero and pulses to I_{stim}. Luckily, the intracellular potential V_{cell} can be recovered from the measured electrode voltage V_{elec} by subtracting the clamp current (at every instant in time) multiplied by R_S, which was previously measured using the technique described on page 8. In the old days of purely analog instrumentation, this subtraction was performed using an analog circuit in a technique called **bridge balance** or **series resistance compensation**. With modern computing power it is much easier to perform this subtraction after the electrode voltage has been digitized.

Note that the current applied via the current source is exactly the same with or without bridge balance; the cell stimulation is not affected, only the interpretation of the measured data.

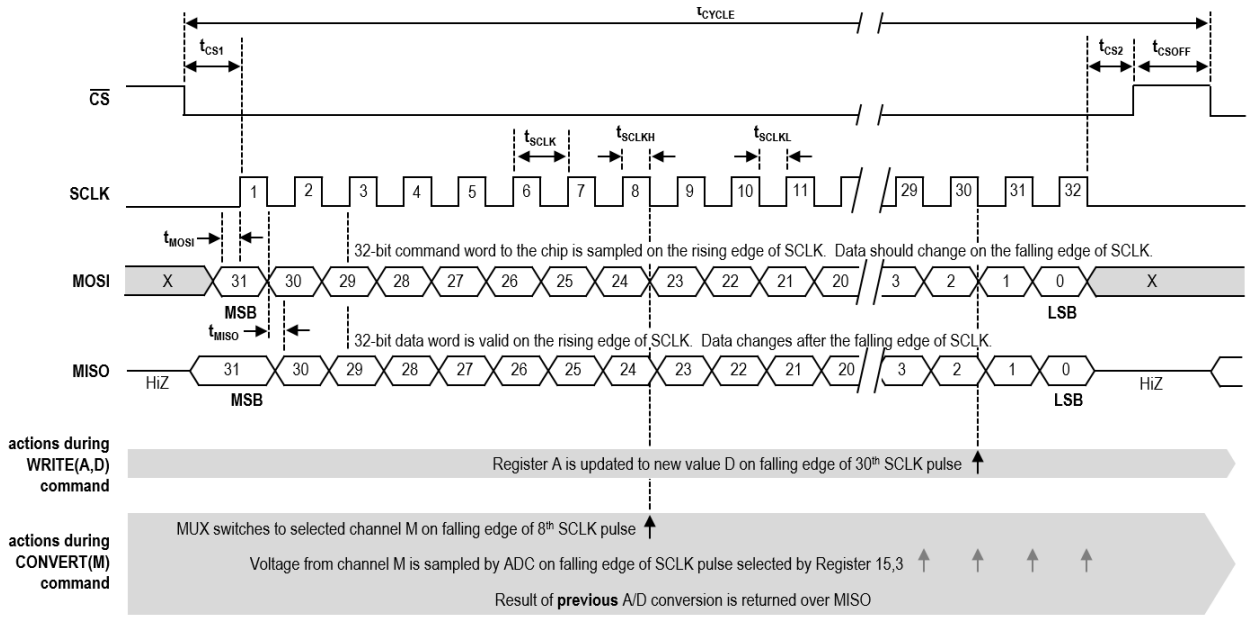
The voltage amplifier in each Clamp Unit has a wide linear range of ±300 mV, so even large ΔV offsets should not saturate the measurements (e.g., a large 1 nA pulse through a high series resistance of 80 MΩ produces a ΔV of only 80 mV).



SPI Bus Signals

CLAMP chips communicate using a standard SPI interface consisting of four signals: an active-low chip select ($\overline{CS}$); a serial data clock (SCLK) with a base value of zero; a "Master Out, Slave In" data line (MOSI) to receive commands from the master device; and a "Master In, Slave Out" data line (MISO) to results from the commands to the master device. The CLAMP chip always functions as the SPI slave device. During each chip select cycle, 32-bit data words are transferred in each direction, MSB first. As shown below, the CLAMP samples MOSI on the rising edge of SCLK. The master should sample MISO on the rising edge of SCLK. (The master device SPI interface should be configured with SPI options CPOL=0 and CPHA=0.) Also note that the sampling of MISO should be adjusted to account for any cable propagation delays. The $\overline{CS}$ line must be pulsed high between every 32-bit data transfer, even when the command word does not request an analog-to-digital conversion.

Timing Diagram



SPI BUS TIMING SPECIFICATIONS

T_A = 25ºC, V_{DD} = 2.22V, V_{SS} = -1.28V unless otherwise noted.

SYMBOL	PARAMETER	MIN	MAX	UNIT	COMMENTS
t_{SCLK}	SCLK Period	83.3		ns	Maximum SCLK frequency is 12 MHz
t_{SCLKH}	SCLK Pulse Width High	41.7		ns	
t_{SCLKL}	SCLK Pulse Width Low	41.7		ns	
t_{CS1}	$\overline{CS}$ Low to SCLK High Setup	41.7		ns	
t_{CS2}	SCLK Low to $\overline{CS}$ High Setup	41.7		ns	
t_{CSOFF}	$\overline{CS}$ High Duration	2200		ns	
t_{MOSI}	MOSI Data Valid to SCLK High Setup	20		ns	
t_{MISO}	SCLK or $\overline{CS}$ Falling Edge to MISO Data Valid		12	ns	
t_{CYCLE}	Total Cycle Time Between ADC Samples	5000		ns	Maximum sample rate is 200 kS/s, or 50 kS/s per channel for 4 multiplexed channels.

SPI Command Words

Each CLAMP chip responds to four basic commands: read from a RAM or ROM register, write to a RAM register, perform an analog-to-digital conversion on a previously selected signal; or write to a RAM register while simultaneously performing an analog-to-digital conversion. Each chip contains 60 nine-bit RAM registers that configure various aspects of chip behavior and several nine-bit ROM registers that store basic properties of the chip.

The CLAMP uses a non-pipelined communication protocol for register reading and writing; each command sent over the MOSI line generates a 32-bit result that is transmitted over the MISO line during the same SPI cycle.

The CLAMP uses a pipelined communication protocol for analog-to-digital conversions. When receiving a CONVERT(M) or WRITE/CONVERT(A, D, M) command, the on-chip MUX switches to channel M on the falling edge of the 8th SCLK pulse. The ADC samples channel M on falling edge of the SCLK pulse selected by Register 15,3. The analog-to-digital conversion is performed during the next CONVERT or WRITE/CONVERT command, and the result is relayed to the master over the MISO line during that SPI cycle. Thus, every CONVERT command must be followed by another CONVERT command in order to read the result of the previous analog-to-digital conversion.

The CLAMP commands are described by the following bit patterns:

32-bit command structure:

`CCMMMMMM AAAAAAAA DDDDDDDD Dxxxxxxx`

`CC` = 2-bit command

`MMMMMM` = 6-bit MUX select

`AAAAAAAA` = 8-bit register address

`DDDDDDDDD` = 9-bit register data

`xxxxxxx` = don't care

CC bits	Command	MISO result
00	Register read: **READ(A)** Read value R from register A	00000000 00000000 0000000R RRRRRRRR
01	Register write: **WRITE(A, D)** Write value D to register A	00000000 00000000 00000000 00000000
10	ADC conversion **CONVERT(M)** Initiate A/D conversion from MUX address M; return result of previous A/D conversion.	00000000 00000000 RRRRRRRR RRRRRRRR (16-bit ADC mode) 00000000 000000RR RRRRRRRR RRRRRRRR (18-bit ADC mode)
11	Register write + ADC conversion: **WRITE/CONVERT(A, D, M)** Write value D to register A and initiate A/D conversion from MUX address M; return result of previous A/D conversion	00000000 00000000 RRRRRRRR RRRRRRRR (16-bit ADC mode) 00000000 000000RR RRRRRRRR RRRRRRRR (18-bit ADC mode)

On-Chip RAM Registers

Each CLAMP1 chip contains 18 nine-bit RAM configuration/control registers; the CLAMP4 chip contains 60 RAM registers. **Upon power-up, all RAM registers contain indeterminate data and should be promptly configured by the SPI master device**.

Individual bits in a register can be changed only by rewriting the entire nine-bit contents. Therefore, it is recommended that the SPI master device maintain a copy of CLAMP register contents in its memory so bitwise operations can be performed there before writing the updated byte to the chip using a WRITE command on the SPI bus.

The RAM registers present in each CLAMP chip are described below. The detailed functions of some programmable variables are described later in the datasheet. Note: All multi-bit variables have their most significant bits (MSBs) on the left in the diagrams below, towards the direction of the register MSB D[8]. Bits marked X have no function but should be set to zero for compatibility with any future chip versions.

RAM registers are updated on the falling edge of the 30th SCLK pulse during the corresponding WRITE or WRITE/CONVERT command.

Clamp Unit Registers

The CLAMP1 chip contains one Clamp Unit, while the CLAMP4 chip contains four identical Clamp Units with independent controls. Each Clamp Unit contains independent circuitry for both voltage clamp and current clamp control and sensing. Each Clamp Unit contains 14 registers used for control and configuration. These registers are repeated across the chip for each Clamp Unit N+1, where N ranges from 0 to 3 in CLAMP4 and should be fixed at 0 for CLAMP1

Each 32-bit SPI command word contains an 8-bit address field. The top four bits of this field designate the Clamp Unit N+1 (e.g., setting the top four bits to 0000 addresses the **elec1** pin, setting the top four bits to 0001 addresses the **elec2** pin, etc.), and the bottom four bits designate the register number listed below (i.e., 0 through 13).

Register N,0: Clamp Voltage DAC

D[8]	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
clamp voltage sign	clamp voltage magnitude [7:0]							

clamp voltage sign: Setting this bit to zero selects negative clamp voltages. Setting this bit to one selects positive clamp voltages.

clamp voltage magnitude [7:0]: This variable sets the voltage magnitude of a DAC used to generate the clamp voltage. This variable, along with **clamp voltage sign**, must be updated at regular intervals to create desired waveforms. Note that this DAC must be enabled by setting **clamp DAC power** in Register N,1. The step size of this DAC is controlled by the **clamp step size** bit in Register N,1.

Register N,1: Clamp Voltage DAC Configuration

D[8]	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
X	X	clamp DAC power	clamp step size	clamp voltage time constant A [4:0]				

clamp DAC power: Setting this bit to zero shuts down the clamp voltage DAC and can be used to reduce power consumption when voltage clamp mode is not used. Under normal operation this bit should be set to one.

clamp step size: Setting this bit to one sets the clamp voltage DAC step size to 5 mV with a range of ±1.275 V. Setting this bit to zero sets the clamp voltage DAC step size to 2.5 mV with a range of ±0.6375 V.

clamp voltage time constant A [4:0]: This variable sets the time constant of a low-pass filter connected to the output of the clamp voltage DAC. The step size of this variable is 0.5 µs, so the time constant may be set within the range of 0 – 15.5 µs. A typical value of this time constant for most general voltage-clamp applications is 10 µs. For rapid voltage changes (e.g., FSCV), smaller time constants can be used.

Register N,2: Clamp Voltage DAC Offset Trim

D[8]	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
X	X	X	clamp voltage offset trim [5:0]					

clamp voltage offset trim [5:0]: This variable trims the DC level of the clamp voltage DAC to compensate for imperfections in fabricated circuit components on the chip. Setting this variable to 32 sets the trim to zero. Every step above this value adds a DC shift of approximately 0.27 mV; every step below this value subtracts 0.27 mV. The total trim range is thus +8.37 mV (with this variable set to 63) to -8.64 mV (with this variable set to zero). This variable should be set during a self-calibration sequence run after the chip is powered up, before the voltage clamp circuit is used. (See Self-Calibration Routines section for details.)

Register N,3: Current-to-Voltage Feedback Resistance; Clamp Voltage Time Constant B

D[8]	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
X	clamp voltage time constant B [4:0]					feedback resistance [2:0]		

clamp voltage time constant B [4:0]: This variable sets the time constant of a low-pass filter connected to the input of the voltage clamp amplifier. The step size of this variable is 0.05 µs, so the time constant may be set within the range of 0 – 1.55 µs. A typical value of this time constant for most general voltage-clamp applications is 0.50 µs.

feedback resistance [2:0]: This variable sets the value of the feedback resistor used to convert current to voltage during voltage-clamp operation. The variable should only be set to one of five values:

variable value	feedback resistance	current measurement range	current noise floor (BW = 5 kHz, 50 kS/s sampling)	current noise floor (BW = 5 kHz, 200 kS/s sampling)
1	200 kΩ	±1.2 µA	91 pA_{rms}	58 pA_{rms}
2	2 MΩ	±120 nA	13 pA_{rms}	8.3 pA_{rms}
3	20 MΩ	±12 nA	3.2 pA_{rms}	2.1 pA_{rms}
4	40 MΩ	±6 nA	2.3 pA_{rms}	1.4 pA_{rms}
5	80 MΩ	±3 nA	1.6 pA_{rms}	1.0 pA_{rms}

More information on the dependence of current noise floor on feedback resistance can be found in the Sampling and Processing Waveform Data section.

Register N,4: Current-to-Voltage Feedback Capacitance; Voltage Clamp Power

D[8]	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
voltage clamp power	feedback capacitance [7:0]							

voltage clamp power: Setting this bit to zero shuts down the voltage clamp amplifier and can be used to reduce power consumption when voltage clamp mode is not used. Under normal operation this bit should be set to one.

feedback capacitance [7:0]: This variable sets the value of the capacitor in parallel with the feedback resistor in the current-to-voltage converter circuit. The product of this capacitance and the feedback resistance (selected in Register N,3) sets a time constant that limits the bandwidth of the voltage clamp amplifier. The step size of this variable is 0.2 pF; the feedback capacitance can be set within the range of 0 – 51 pF.

Register N,5: Voltage Clamp Difference Amplifier Configuration

D[8]	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
X	diff amp in+ select	diff amp in- select	diff amp offset trim [5:0]					

diff amp in+ select: Setting this bit to zero connects the positive input of the gain-of-10 difference amplifier to the output of the voltage clamp amplifier; this is the normal mode of operation. Setting this bit to one connects the positive input of the difference amplifier to ground. This can be used by self-calibration algorithms to measure and trim any DC offset in the difference amplifier.

diff amp in- select: Setting this bit to zero connects the negative input of the gain-of-10 difference amplifier to the clamp voltage; this is the normal mode of operation. Setting this bit to one connects the negative input of the difference amplifier to ground. This can be used by self-calibration algorithms to measure and trim any DC offset in the difference amplifier.

diff amp offset trim [5:0]: This variable trims the DC level of the difference amplifier to compensate for imperfections in fabricated circuit components on the chip. Setting this variable to 32 sets the trim to zero. Every step above this value adds a DC shift of approximately 2.7 mV to the output of the current-to-voltage converter; every step below this value subtracts 2.7 mV. The total trim range is thus +83.7 mV (with this variable set to 63) to -86.4 mV (with this variable set to zero). This variable should be set during a self-calibration sequence run after the chip is powered up, before the voltage clamp circuit is used. (See Self-Calibration Routines section for details.)

Register N,6: Fast Transient Capacitive Compensation Magnitude

D[8]	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
fast trans in select	fast trans cap compensation [7:0]							

fast trans in select: Setting this bit to zero connects the input of the fast transient capacitive compensation circuitry to the clamp voltage. This is the normal mode of operation for voltage clamp operation. Setting this bit to one connects the input to the main input from the off-chip electrode. This enables capacitive compensation in current clamp mode. If fast transient capacitive compensation is not used, this bit should be set to zero.

fast trans cap compensation [7:0]: This variable sets the magnitude of capacitance to be compensated by the fast transient capacitive compensation circuitry. This variable should always have a value in the range of 55 – 255; values between 0 and 54 should not be used. Setting this variable to 55 selects zero capacitance compensation. The step size of this variable is set by the **fast trans range** variable in Register N,8.

Register N,7: Fast Transient Capacitive Compensation Configuration; Clamp Configuration

D[8]	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
fast trans power	clamp current enable	voltage clamp connect	fast trans connect	fast trans time constant [4:0]				

fast trans power: Setting this bit to zero shuts down the fast transient capacitive compensation circuitry and can be used to reduce power consumption when fast transient compensation is not used. Under normal operation this bit should be set to one.

clamp current enable: Setting this bit to one enables the current source to drive a specified current onto the electrode. Setting this bit to zero sets the current source output to zero. The current source can be enabled to establish a current clamp or to subtract a large background current in voltage clamp mode.

voltage clamp connect: Setting this bit to one connects the input of the voltage clamp amplifier to the main input from the off-chip electrode. Setting this bit to zero disconnects the voltage clamp amplifier, as should be done in current clamp mode.

fast trans connect: Setting this bit to one connects the fast transient capacitive compensation circuitry to the main input from the off-chip electrode. Setting this bit to zero disconnects this circuitry, which can be done if capacitive compensation is not enabled.

fast trans time constant [4:0]: This variable sets the time constant of a low-pass filter connected to the input of the fast transient capacitive compensation circuitry. The step size of this variable is 0.05 µs, so the time constant may be set within the range of 0 to 1.55 µs. A typical value of this time constant for most applications is 0.50 µs, but this is typically adjusted by the user to fine-tune capacitive compensation.

Register N,8: Input Select; Fast Transient Configuration; Voltage Amplifier Power

D[8]	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
X	voltage amp power	fast trans range [1:0]		buzz switch [1:0]		input select [2:0]		

voltage amp power: Setting this bit to zero shuts down the voltage amplifier and can be used to reduce power consumption when current clamp mode is not used. Under normal operation this bit should be set to one.

fast trans range [1:0]: This variable selects the magnitude of C_C, the capacitor used to implement fast transient capacitive compensation. The following table lists the values of C_C and the resulting compensation range achievable (i.e., with the maximum value of **fast trans cap compensation** in Register N,6) for each setting.

variable value	C_C	fast transient compensation step size	fast transient compensation range
0	2.75 pF	0.05 pF	0 – 10 pF
1	3.85 pF	0.07 pF	0 – 14 pF
2	4.40 pF	0.08 pF	0 – 16 pF
3	5.50 pF	0.10 pF	0 – 20 pF

buzz switch [1:0]: This variable controls a 4-way switch at the bottom of fast transient compensation capacitor C_C that can be used to switch between different voltages to create a "buzz" function. The following table lists the signals driving C_C for each value of this variable. Under normal operation this variable should be set to 0. (See Zap and Buzz Functions section for more details.)

variable value	signal driving C_C
0	fast transient compensation amplifier
1	**GND** (0 V)
2	**VREF** (+1.28 V)
3	**VSS** (-1.28 V)

input select [2:0]: This variable selects the input signal that is routed to the patch clamp circuit assembly. Various settings of this variable are useful in self calibration routines. Under normal operation, this variable should be set to 4.

variable value	input signal to patch clamp circuit
0 – 3	open circuit
4	electrode pin (**elec**)
5	calibration resistor 1 pin (**Rcal1**)
6	calibration resistor 2 pin (**Rcal2**)
7	short to ground

Register N,9: Clamp Current Source

D[8]	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
X	clamp current sign	clamp current magnitude [6:0]						

clamp current sign: Setting this bit to one drives current out of the chip. This is considered positive current. Setting this bit to zero pulls current (i.e., positive charges) into the chip. This is considered negative current.

clamp current magnitude [6:0]: This variable sets the magnitude of the current source (i.e., the magnitude of the current produced is **clamp current magnitude** × step size). The step size of the current source is controlled by the Registers N,10 through N,13. This variable, along with **clamp current sign**, must be updated at regular intervals to create desired waveforms

Registers N,10 – N,13: Clamp Current Source Scale

Register N,10

D[8]	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
X	X	negative current scale coarse [6:0]						

Register N,11

D[8]	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
X	negative current scale fine [7:0]							

Register N,12

D[8]	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
X	X	positive current scale coarse [6:0]						

Register N,13

D[8]	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
X	positive current scale fine [7:0]							

negative current scale coarse [6:0]
negative current scale fine [7:0]
positive current scale coarse [6:0]
negative current scale fine [7:0]

These variables set the step size of the current source that is controlled by Register N,9. The positive and negative current scale are set independently to allow for corrections of small current imbalances caused by device mismatch during chip fabrication. Every coarse step is equal to approximately 60 fine steps. **Larger** values in coarse or fine registers produce **smaller** currents. The values of these variables should be adjusted during self-calibration (see Self-Calibration Routines section for details). The following table lists approximate "starting values" for these registers.

current source step size	coarse register value	fine register value
5 pA	70	128
50 pA	8	75
500 pA	0	107
1 nA	0	62

Global RAM Registers

In addition to the registers contained in each Clamp Unit, each CLAMP chip also contains four global RAM registers that set various chip-wide parameters. These global registers are addressed by setting the top four bits of the address field to 15.

Register 15,0: Temperature Sensor

D[8]	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
X	X	X	X	X	tempS3	tempS2	tempS1	tempen

tempS1, **tempS2**, and **tempS3:** These bits control switches in the on-chip temperature sensor, whose output may be sampled by the ADC on MUX channel 63. The detailed operation of the temperature sensor is described in the Temperature Sensor section later in the datasheet. When the temperature sensor is not in use, these bits should each be set to zero.

tempen: Setting this bit to one enables the on-chip temperature sensor. Power consumption may be reduced by setting this bit to zero to disable the sensor.

Register 15,1: Global Bias A

D[8]	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
X	global bias A [7:0]							

global bias A [7:0]: This variable sets a set of bias currents that are used by circuit components across the chip. This variable should always be set to 86. This variable should be set before any self-calibration routines are performed on the Clamp Units.

Register 15,2: Global Bias B

D[8]	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
X	X	X	global bias B [5:0]					

global bias B [5:0]: This variable sets a set of bias currents that are used by circuit components across the chip. This variable should always be set to 29. This variable should be set before any self-calibration routines are performed on the Clamp Units.

Register 15,3: ADC Configuration; Auxiliary Digital Output

D[8]	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
X	X	digout HiZ	digout	weak MISO	ADC timing [2:0]			18 bit ADC

digout HiZ: The CLAMP chips have an auxiliary digital output pin **auxout** that may be used to activate off-chip circuitry. Setting this bit to one puts the digital output into high impedance (HiZ) mode.

digout: This bit is driven out of the auxiliary CMOS digital output pin **auxout**, provided that the **digout HiZ** bit is set to zero. See the Auxiliary Digital Output section for details.

weak MISO: If this bit is set to zero, the MISO line goes to high impedance mode (HiZ) when $\overline{CS}$ is pulled high, allowing multiple chips to share the same MISO line so long as only one of their chip select lines is activated at any time. If only one CLAMP chip will be using a MISO line, this bit may be set to one, and when $\overline{CS}$ is pulled high the MISO line will be driven weakly by the chip. This can prevent the line from drifting to indeterminate values between logic high and logic low. **This pin has no effect in LVDS communication mode.**

ADC timing [2:0]: This variable adjusts the timing of the rising edge of the **ADC_CNV** pulse sent to the external ADC. The input to the ADC is sampled at this time. (The falling edge of the **ADC_CNV** pulse always occurs on the falling edge of the 7th SCLK pulse; the analog MUX switches on the falling edge of the 8th SCLK pulse.) The user must ensure that the **ADC_CNV** pulse is held low for a sufficiently long period of time to satisfy the timing specifications of the ADC used with the CLAMP chip.

Note that during a WRITE/CONVERT command, the new register value is updated on the falling edge of the 30th SCLK pulse. By adjusting the value of the **ADC timing** variable, the ADC can be made to sample just before, just after, or coincident with the register update.

This variable should typically be set to 5.

variable value	timing of ADC_CNV pulse rising edge
0	falling edge of 25th SCLK pulse
1	falling edge of 26th SCLK pulse
2	falling edge of 27th SCLK pulse
3	falling edge of 28th SCLK pulse
4	falling edge of 29th SCLK pulse
5	falling edge of 30th SCLK pulse
6	falling edge of 31st SCLK pulse
7	falling edge of 32nd SCLK pulse

18 bit ADC: If an 18-bit ADC is connected to the CLAMP chip, this bit must be set to one for proper operation. If a 16-bit ADC is connected, this bit must be set to zero.

On-Chip ROM Registers

Each CLAMP chip contains the following global ROM registers that provide information on the identity and capabilities of the chip.

Registers 15,7 – 15,11: Company Designation

The read-only registers 15,7 through 15,11 contain the characters INTAN in ASCII. The contents of these registers can be read to verify the fidelity of the SPI interface.

Register 15,12: Future Expansion

This register is reserved for future expansion. Its current value is zero.

Register 15,13: Die Revision

D[8]	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
die revision [8:0]								

die revision [8:0]: This read-only variable encodes a die revision number which is set by Intan Technologies to encode various versions of a chip.

Register 15,14: Number of Clamp Units

D[8]	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
number of clamp units [8:0]								

number of clamp units [8:0]: This read-only variable encodes the total number of Clamp Units on the chip. This register is set to 1 for the CLAMP1 chip and 4 for the CLAMP4 chip.

Register 15,15: Intan Technologies Chip ID

D[8]	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
0	chip ID [7:0]							

chip ID [7:0]: This read-only variable encodes a unique Intan Technologies ID number indicating the type of chip. The chip ID for the CLAMP1 and CLAMP4 chips is 129.

MUX Addressing

The CLAMP chip contains an analog multiplexer (MUX) that routes one selected analog signal to the external ADC. The MUX address is selected using a six-bit field in each 32-bit SPI command word. The following table lists the valid values for MUX addresses:

MUX address	MUX output to external ADC
0	Clamp Unit 0, current measurement
1	Clamp Unit 0, voltage measurement
2	Clamp Unit 1, current measurement (CLAMP4 only)
3	Clamp Unit 1, voltage measurement (CLAMP4 only)
4	Clamp Unit 2, current measurement (CLAMP4 only)
5	Clamp Unit 2, voltage measurement (CLAMP4 only)
6	Clamp Unit 3, current measurement (CLAMP4 only)
7	Clamp Unit 3, voltage measurement (CLAMP4 only)
63	temperature sensor

Sampling and Processing Waveform Data

Measured waveforms from voltage clamp or current clamp measurements are generated by repeatedly issuing CONVERT commands to the CLAMP chip at a regular interval corresponding to the desired ADC sampling rate. In most applications it is convenient to issue WRITE/CONVERT commands instead, as these allow registers to be changed (e.g., to change the clamp voltage or clamp current) without interrupting the steady rate of ADC conversions. If the CLAMP4 chip is being used with multiple Clamp Units active, the signals from the Clamp Units should be sampled in round robin fashion (e.g., channel 0, channel 1, channel 2, channel 3, channel 0, channel 1,…) such that each channel is sampled at the desired rate.

The minimum recommended sample rate for each Clamp Unit is 50 kS/s. If all four Clamp Units of a CLAMP4 chip are sampled at this rate, the ADC will have a total sampling rate of 200 kS/s. In response to a CONVERT or CONVERT/WRITE command received on the SPI bus, the CLAMP chip sends the proper control signals to the analog MUX and external ADC to digitize a particular signal, reads the result from the ADC, and returns this result over the SPI bus in the format described in the SPI Command Words section.

The ADC result will be a signed integer ranging from -32,768 to +32,767 in the case of a 16-bit ADC, or from -131,072 to +131,071 in the case of an 18-bit ADC. The MUX output voltage (the differential voltage between the **MUX_out+** and **MUX_out–** pins) can be derived from this number by multiplying by the ADC reference voltage of +2.56V (if the schematics presented in this datasheet are followed) and dividing by 2^{N-1} for an N-bit ADC:

$$MUX\_out = (result \times 2.56V) / 2^{N-1}$$

When operating in current clamp mode, the electrode voltage is derived by dividing the MUX output voltage by 8, the gain of the voltage amplifier. When operating in voltage clamp mode, the electrode current is derived by dividing the MUX output voltage by $10 \cdot R_F$, where R_F is the exact value of the selected feedback resistance measured during chip self-calibration. (The factor of 10 must be included to account for the gain of the difference amplifier; see Clamp Unit Diagram for details.)

Bessel Filtering and Downsampling

After each waveform has been sampled, it should be digitally low-pass filtered using a Bessel filter to limit the bandwidth of the signal to 10 kHz or less. Bessel filters are preferred over other filter types (e.g., Butterworth, Chebyshev) due to their superior time-domain performance and low overshoot. In the 20th century Bessel filters were built directly into instruments using analog circuits but today it is better to implement them digitally to take advantage of the flexibility and linearity of digital filter algorithms.

A 4th-order Bessel filter provides a good balance between steepness of attenuation (80 dB/decade beyond the cutoff frequency) and computational complexity. Page 24 shows MATLAB code that applies a 4th-order Bessel low-pass filter to a signal. (This simple code should be readable even to non-MATLAB users.)

Typically, intracellular voltage measurements taken in current clamp mode are bandlimited to 10 kHz. Current measurements taken in voltage clamp mode are often bandlimited to 5 kHz, but a cutoff frequency of 2 kHz or less can be used to reduce noise at the expense of frequency response. In the case of white noise, reducing the bandwidth by a factor of N reduces the rms noise floor by a factor of $\sqrt{N}$. The CLAMP chip amplifiers produce noise with more energy at low frequencies, so the noise reduction is less than $\sqrt{N}$ in practice. After filtering with a high-order (4th order or higher) Bessel filter, the signal can be downsampled by a factor of K by selecting every Kth sample from the filtered waveform and discarding the other samples. A signal should never be downsampled to a sampling rate less than twice the Bessel filter's cutoff frequency. For example, if you sampled a Clamp Unit at 50 kS/s and then apply a 5-kHz Bessel low-pass filter, you can then safely downsample the signal by a factor of five to 10 kS/s, but no further.

The CLAMP chips have integrated low-pass filters with cutoff frequencies of approximately 20 kHz, which is slightly below the 25 kHz Nyquist frequency limit set by 50 kS/s ADC sampling. The Nyquist sampling criterion dictates that any analog signal should be bandlimited to half the ADC sampling rate before digitization to prevent aliasing. While the on-chip low-pass filters attenuate a great deal of the signal beyond 25 kHz, they are not sharp, high-order filters, so some residual high-frequency noise is aliased, which adds to the noise floor at lower frequencies. This increase in noise due to aliasing can be reduced if higher sampling rates are used: 100 kS/s or 200 kS/s per channel.

Channels that are sampled at these higher sampling rates can be downsampled by a factor of K by first applying a Bessel low-pass filter with a cutoff frequency of 10 kHz or less, and then selecting every Kth sample from the resulting waveform.

Tables on the following page show typical rms noise floor levels for current measurements (in voltage clamp mode) and voltage measurements (in current clamp mode) at sampling rates of 50 kS/s/channel, 100 kS/s/channel, and 200 kS/s/channel after Bessel low-pass filters of 2 kHz, 5 kHz, or 10 kHz are applied. Peak-to-peak noise levels are roughly five to six times the rms noise level.

Voltage Measurement Noise Floor (range = ±300 mV)

Bessel Filter Cutoff Frequency	Per-Channel Sampling Rate				
	50 kS/s	100 kS/s	200 kS/s	50 kS/s, C_{aa} = 4.7 nF	200 kS/s, C_{aa} = 4.7 nF
2 kHz	25 μV_{rms}	19 μV_{rms}	15 μV_{rms}	7.6 μV_{rms}	6.9 μV_{rms}
5 kHz	38 μV_{rms}	28 μV_{rms}	22 μV_{rms}	11 μV_{rms}	9.2 μV_{rms}
10 kHz	54 μV_{rms}	37 μV_{rms}	30 μV_{rms}	15 μV_{rms}	12 μV_{rms}

Current Measurement Noise Floor with R_F = 80 MΩ (range = ±3 nA)

Bessel Filter Cutoff Frequency	Per-Channel Sampling Rate				
	50 kS/s	100 kS/s	200 kS/s	50 kS/s, C_{aa} = 4.7 nF	200 kS/s, C_{aa} = 4.7 nF
2 kHz	1.4 pA_{rms}	1.0 pA_{rms}	0.96 pA_{rms}	1.3 pA_{rms}	0.87 pA_{rms}
5 kHz	3.0 pA_{rms}	2.8 pA_{rms}	3.0 pA_{rms}	3.1 pA_{rms}	2.8 pA_{rms}
10 kHz	6.7 pA_{rms}	8.0 pA_{rms}	9.2 pA_{rms}	8.6 pA_{rms}	8.1 pA_{rms}

Current Measurement Noise Floor with R_F = 40 MΩ (range = ±6 nA)

Bessel Filter Cutoff Frequency	Per-Channel Sampling Rate				
	50 kS/s	100 kS/s	200 kS/s	50 kS/s, C_{aa} = 4.7 nF	200 kS/s, C_{aa} = 4.7 nF
2 kHz	1.8 pA_{rms}	1.4 pA_{rms}	1.3 pA_{rms}	1.6 pA_{rms}	1.1 pA_{rms}
5 kHz	3.0 pA_{rms}	2.4 pA_{rms}	2.4 pA_{rms}	2.6 pA_{rms}	2.1 pA_{rms}
10 kHz	4.8 pA_{rms}	4.2 pA_{rms}	4.7 pA_{rms}	4.7 pA_{rms}	4.2 pA_{rms}

Current Measurement Noise Floor with R_F = 20 MΩ (range = ±12 nA)

Bessel Filter Cutoff Frequency	Per-Channel Sampling Rate				
	50 kS/s	100 kS/s	200 kS/s	50 kS/s, C_{aa} = 4.7 nF	200 kS/s, C_{aa} = 4.7 nF
2 kHz	1.9 pA_{rms}	1.9 pA_{rms}	1.9 pA_{rms}	1.8 pA_{rms}	1.6 pA_{rms}
5 kHz	3.0 pA_{rms}	3.1 pA_{rms}	3.2 pA_{rms}	3.0 pA_{rms}	2.7 pA_{rms}
10 kHz	4.5 pA_{rms}	4.5 pA_{rms}	5.1 pA_{rms}	4.6 pA_{rms}	4.3 pA_{rms}

Current Measurement Noise Floor with R_F = 2 MΩ (range = ±120 nA)

Bessel Filter Cutoff Frequency	Per-Channel Sampling Rate				
	50 kS/s	100 kS/s	200 kS/s	50 kS/s, C_{aa} = 4.7 nF	200 kS/s, C_{aa} = 4.7 nF
2 kHz	9.2 pA_{rms}	8.7 pA_{rms}	8.6 pA_{rms}	7.9 pA_{rms}	7.5 pA_{rms}
5 kHz	14 pA_{rms}	12 pA_{rms}	12 pA_{rms}	11 pA_{rms}	10 pA_{rms}
10 kHz	19 pA_{rms}	15 pA_{rms}	16 pA_{rms}	17 pA_{rms}	13 pA_{rms}

Current Measurement Noise Floor with R_F = 200 kΩ (range = ±1.2 µA)

Bessel Filter Cutoff Frequency	Per-Channel Sampling Rate				
	50 kS/s	100 kS/s	200 kS/s	50 kS/s, C_{aa} = 4.7 nF	200 kS/s, C_{aa} = 4.7 nF
2 kHz	87 pA_{rms}	71 pA_{rms}	66 pA_{rms}	53 pA_{rms}	55 pA_{rms}
5 kHz	120 pA_{rms}	97 pA_{rms}	88 pA_{rms}	70 pA_{rms}	69 pA_{rms}
10 kHz	170 pA_{rms}	120 pA_{rms}	110 pA_{rms}	91 pA_{rms}	84 pA_{rms}

Bessel Filter MATLAB Code

```
function y = bessel_LPF(x, sample_period, fc)

% y = bessel_LPF(x, sample_period, fc)
%
% 4th-order Bessel low-pass filter
%
% y = filtered signal
% x = signal to be filtered
% sample_period = sampling period of x (in sec)
% fc = desired Bessel cutoff frequency (in Hz)
%
% Example usage:
%   Here, x is a signal sampled at 50 kS/s, and we wish to apply a
%   5 kHz Bessel filter to produce an output waveform y.
%
% >> y = bessel_LPF(x, 1/50000, 5000);
%
%   Now, if we want to downsample y by a factor of five to 10 kS/s:
%
% >> z = y(1:5:end);

y1 = lowpass_biquad(x,  sample_period, 1.6034 * fc, 0.8055);
y  = lowpass_biquad(y1, sample_period, 1.4302 * fc, 0.5219);

end


function y = lowpass_biquad(x, sample_period, fc, Q)

% Calculate five constants (a0, a1, a2, b1, and b2) to be used in
% the digital filter algorithm.  To reduce computational complexity
% (e.g., for FPGA implementations) these constants could be pre-
% calculated for fixed values of sample_period, fc, and Q.
K = tan(pi * fc * sample_period);
norm = 1 / (1 + K / Q + K * K);
a0 = K * K * norm;
a1 = 2 * a0;
a2 = a0;
b1 = 2 * (K * K - 1) * norm;
b2 = (1 - K / Q + K * K) * norm;

% Run digital biquad filter.  Each output sample at time t is a
% weighted sum of input samples from time t, t-1, and t-2, and
% output samples from time t-1 and t-2.
L = length(x);
y = x;  % y(0) = x(0); y(1) = x(1);
for t = 3:L
    y(t) = a0*x(t) + a1*x(t-1) + a2*x(t-2) - b1*y(t-1) - b2*y(t-2);
end

end
```

Switching Between Voltage Clamp and Current Clamp

The following sequence should be followed in order when switching from voltage clamp mode to current clamp mode. These steps should be executed as an uninterrupted sequence of WRITE or WRITE/CONVERT commands.

1. Set the desired **current source scale** (Registers N,10 – N,13), **clamp current magnitude** and **clamp current sign** (Register N,9).
2. Simultaneously close the **clamp current enable** switch and open the **voltage clamp connect** switch (Register N,7).
3. Adjust the magnitude of **fast transient cap compensation** (Register N,6). The optimum value for this variable is typically 0.5 pF lower in current clamp mode than in voltage clamp mode. If this value is not reduced, oscillations my result.
4. Set the **fast tran in select** bit (Register N,6) to one.

Steps 3 and 4 may be omitted if fast transient capacitance compensation is not used.

The following sequence should be followed in order when switching from current clamp mode to voltage clamp mode.

1. Set the **feedback resistance** (Register N,3) and **feedback capacitance** (Register N,4) to the desired values.
2. Set the **clamp voltage sign** and **clamp voltage magnitude** (Register N,0) to the desired levels.
3. Simultaneously open the **clamp current enable** switch and close the **voltage clamp connect** switch (Register N,7).
4. Set the **fast tran in select** bit (Register N,6) to zero.
5. Adjust the magnitude of **fast transient cap compensation** (Register N,6). The optimum value for this variable is typically 0.5 pF higher in voltage clamp mode than in current clamp mode.
6. Set the **clamp current magnitude** (Register N,9) to zero.

Steps 4 and 5 may be omitted if fast transient capacitance compensation is not used.

Zap and Buzz Functions

Traditional patch clamp amplifiers often have a “zap” function that applies brief “high” voltage pulses (1V or so) to the electrode for the purpose of breaking into a cell membrane after a gigaseal has been achieved. The wide range of the clamp voltage DAC (±1.275V with the step size set to 5 mV) allows a zap function to be implemented as a normal voltage clamp operation.

Some intracellular recording instruments also have a “buzz” function to facilitate cell penetration. A buzz function can be implemented with the CLAMP chip using the buzz switch in the fast transient capacitive compensation module to modulate the voltage driving the compensation capacitor C_C. Typically the buzz switch would alternate between V_{SS} (-1.28V) and V_{REF} (+1.28V). The value of C_C can be selected to adjust the magnitude of the AC current injected to the electrode.

Auxiliary Digital Output

All CLAMP chips have a single user-programmable digital output pin **auxout** which may be used to control an external device via SPI commands. Register 15,3 contains two control registers that configure the state of this signal: setting **digout HiZ** to zero enables the **auxout** pin; if **digout HiZ** is set to one then the **auxout** pin assumes a high-impedance state. The **digout** register controls the value of the **auxout** pin. If **digout** is set to zero then **auxout** is driven to V_{SS} (-1.28 V); if **digout** is set to one then **auxout** is driven to V_{DD} (typically +2.22 V). The **auxout** pin can supply a maximum of ±2 mA while maintaining proper voltage levels. If additional drive current is needed, the user must add external circuitry.

It is important to remember that the values of the **digout HiZ** and **digout** registers are indeterminate when the chip is first turned on, so care should be taken to ensure that any device connected to this pin does not cause trouble if the **auxout** pin assumes an unexpected value when the chip is initially powered up.

Temperature Sensor

Each CLAMP chip includes an on-chip temperature sensor that can be read using the ADC. Making temperature measurements is a multi-step process that requires sending several SPI commands and performing some simple arithmetic to process the results.

The temperature sensor is controlled by several bits in Register 15,0: **tempen**, **tempS1**, **tempS2**, and **tempS3**. If the temperature sensor is not used, these bits should be set to zero to reduce power consumption. Before performing a temperature measurement the bit **tempen** should be set to one to enable the temperature sensor module. After setting this bit, at least 200 µs should elapse before a temperature reading is made to allow time for the sensor circuitry to reach equilibrium. (All other operations may be performed on the chip during this time.)

The procedure for taking a temperature measurement involves the following steps:

1. Set **tempS1** = 1, **tempS2** = 0, **tempS3** = 0, and wait time T.

Repeat steps 2-5 four times:

2. Set **tempS2** = 1, and wait time T.
3. Set **tempS3** = 1, and wait time T.
4. Set **tempS2** = 0, and wait time T.
5. Set **tempS3** = 0, and wait time T.

6. Sample the output of the temperature sensor (MUX address 63) with the ADC.
7. Set **tempS1** = 1, and wait time T.
8. If the temperature sensor will no longer be used, set **tempS1** = 0 and **tempen** = 0.

In these steps, time T should be between 50 µs and 500 µs.

From the ADC result, the temperature is calculated as follows:

16-bit ADC: T(ºC) = (MUX_out voltage / 6.02 mV) – 273.15 = (0.01298 × result) – 273.15

18-bit ADC: T(ºC) = (MUX_out voltage / 6.02 mV) – 273.15 = (0.003244 × result) – 273.15

Note all that other chip operations may be performed during the waiting periods specified in the steps above, so temperature sensor operations may be interleaved between other SPI commands. It is recommended that no "power up/down" operations be performed while a temperature reading is in progress, as any change in overall power consumption may cause the chip temperature to change.

After a temperature reading is complete, set **tempS1** = 0, **tempS2** = 0, and **tempS3** = 0 to minimize power consumption. If another temperature reading will not be needed for some time, set **tempen** = 0.

The temperature sensor is included to track relative temperature changes that may alter certain parameters on the chip. Absolute temperature readings may vary ±3ºC from chip to chip. If accurate absolute temperature measurements are needed, each chip should be calibrated at a known temperature.

Power Dissipation

Total power dissipation of a CLAMP chip depends on how it is configured and operated. The majority of supply current is drawn from V_{DD} to V_{SS}. The V_{REF} pin pulls only 60 µA per Clamp Unit with the clamp voltage step size set to 2.5 mV and 120 µA per Clamp Unit with the voltage step size set to 5.0 mV.

Each Clamp Unit pulls approximately 2.1 mA from V_{DD} to V_{SS} with all modules powered up. If LVDS communication is enabled, the CLAMP chip pulls an additional 5.7 mA from V_{DD} to V_{SS}.

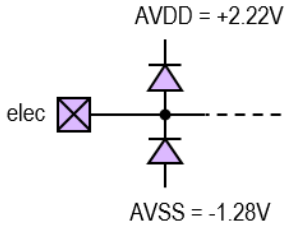
Typical CLAMP chip power dissipation and supply current values are listed in the Electrical Characteristics table. Assuming LVDS mode is enabled, a CLAMP1 chip uses approximately 27 mW of power; a CLAMP4 chip uses about 49 mW.

The external ADC consumes an additional 1 - 8 mW typically (i.e., 0.3 - 2.3 mA from the +2.22V/-1.28V supply), depending on the type of ADC used and the total sampling rate.

ESD Protection Circuitry

All CMOS integrated circuits are susceptible to damage by exposure to electrostatic discharge (ESD) from charged bodies. Electrostatic charges greater than 1000V can accumulate on the human body or test equipment and can discharge without detection. All CLAMP chips incorporate protection circuitry to guard against moderate ESD events. However, permanent damage may occur on devices subjected to high energy electrostatic discharges. It is important for users to understand the nature of the ESD protection structures used on the chips.

The figure below illustrates the on-chip diodes used for ESD protection at each electrode I/O pin. Diodes are connected to **AVSS** (-1.28V) and **AVDD** (typically +2.22V), and are used to bleed off charge quickly to prevent the voltage on internal transistors from exceeding damaging levels. The voltage level of all I/O pins should remain between V_{SS} and V_{DD} at all times to prevent the ESD diodes from becoming forward biased and passing current. Under normal operation these diodes will remain reverse biased and the leakage current through each diode will be less than 1 fA (10^{-15} A).



Additional Off-Chip Components for ESD Protection

Off-chip series resistors may be added to each electrode I/O pin to improve ESD robustness. These series resistors will add to the electrode series resistance R_P shown on page 6 and lead to increased voltage drop when current passes through the electrode. Furthermore, series resistors add thermal noise that increases the total voltage noise floor on each Clamp Unit. The rms noise added by a series resistor R is given by

$$v_{n,\mathrm{rms}} = \sqrt{4kTR \cdot \mathrm{BW}}$$

where BW is the amplifier bandwidth and kT = 4.12×10^{-21} J at 25ºC.

This noise adds to the inherent amplifier noise in a sum-of-squares manner. The following table lists series resistor values that may be used with various bandwidths and per-channel sampling rates if a 10% increase in amplifier noise (above the baseline noise floor levels listed on page 23) can be tolerated.

voltage amplifier bandwidth / sampling rate	maximum R for 10% increase in noise
2 kHz (50 kS/s)	620 kΩ
5 kHz (50 kS/s)	390 kΩ
10 kHz (50 kS/s)	330 kΩ
2 kHz (200 kS/s)	270 kΩ
5 kHz (200 kS/s)	180 kΩ
10 kHz (200 kS/s)	120 kΩ

ESD protection may be further strengthened through the use of external transient voltage suppressors manufactured by a variety of semiconductor companies (e.g., Vishay, Littelfuse, STMicroelectronics), but these parts may contribute measureable leakage currents which could affect current measurements in voltage clamp mode.

Self-Calibration Routines

Due to variability in analog device parameters (e.g., resistance, capacitance, transistor threshold voltages) across a silicon chip and from one chip to another, it is necessary to perform a self-calibration routine on each CLAMP chip to obtain high precision in both clamp levels as well as measured waveform values. Ideally the calibration routines described below should be performed every time the chip is powered up, and repeated if the chip undergoes significant temperature changes (i.e., more than 5°C). Self-calibration cannot be performed while a voltage clamp or current clamp measurement is in progress; each Clamp Unit is electrically disconnected from its electrode pin during the calibration process. Calibration will be more accurate if it is performed while the CLAMP chip is shielded in a Faraday cage to reduce 50/60 Hz noise.

After power is applied to the chip, all chip registers should be set to their default values and all Clamp Units to be used should be powered up. After registers are configured to default values, it is recommended to wait two seconds to allow the on-chip temperature to stabilize before starting calibration.

Calibration Step 1: Voltage Amplifier Calibration

The voltage amplifier, used in current clamp measurements, does not have a hardware offset trim capability. Any offset must be subtracted in software.

1. Disable fast transient compensation. (Make sure the **fast trans connect** switch (Register N,7) is open.) Make sure the **clamp current enable** switch (Register N,7) is open. Make sure the **voltage amp power** bit (Register N,8) is set. Open the **voltage clamp connect** switch (Register N,7). Set the **input select** switch to ground (Register N,8).
2. Measure the output of the voltage amplifier.
3. Store this value in software and subtract it from successive voltage amplifier measurements.
4. Restore the **voltage clamp connect** and **input select** switches to their default positions.

Calibration Step 2: Difference Amplifier Calibration, Part 1

1. Connect the **diff amp in+ select** and **diff amp in- select** switches (Register N,5) to ground.
2. Measure the output of the difference amplifier (i.e., the current sensor).
3. Adjust **diff amp offset trim** (Register N,5) and repeat Step 2 until the output of the difference amplifier is as close to zero as possible. Any residual offset must be subtracted in software.
4. Restore the **diff amp in+ select** and **diff amp in- select** switches to their default positions.

Calibration Step 3: Clamp Voltage Calibration

1. Connect the **diff amp in- select** switch (Register N,5) to ground.
2. Open the **voltage clamp connect** switch (Register N,7). Select the smallest value of the **feedback resistance** (i.e., 200 kΩ) (Register N,3). Select the largest value of **feedback capacitance** (i.e., 51.0 pF) (Register N,4).
3. Set the **clamp voltage magnitude** (Register N,0) to zero. The settings of **clamp voltage sign** and **clamp step size** (Registers N,0 and N,1) do not matter.
4. Measure the output of the difference amplifier.
5. Adjust **clamp voltage offset trim** (Register N,2) and repeat Step 4 until the output of the difference amplifier is as close to zero as possible.
6. Restore the **diff amp in- select** switch to its default position.

Calibration Step 4: Difference Amplifier Calibration, Part 2

The previous difference amplifier calibration (Part 1) was used only to facilitate clamp voltage calibration. Now the difference amplifier must be calibrated a second time to compensate for offset in both the difference amplifier and the operational amplifier in the current-to-voltage converter.

1. Open the **voltage clamp connect** switch (Register N,7). Select the smallest value of the **feedback resistance** (i.e., 200 kΩ) (Register N,3). Select the largest value of **feedback capacitance** (i.e., 51.0 pF) (Register N,4).
2. Set the **clamp voltage magnitude** (Register N,0) to zero.
3. Measure the output of the difference amplifier.
4. Adjust **diff amp offset trim** (Register N,5) and repeat Step 3 until the output of the difference amplifier is as close to zero as possible. Any residual offset must be subtracted in software.
5. Close the **voltage clamp connect** switch.

Calibration Step 5: Current-to-Voltage Converter Calibration

The current-to-voltage converter, in combination with the difference amplifier, produces a voltage proportional to the current flowing through the **voltage clamp connect** switch. The constant of proportionality is the feedback resistance (which can have one of five user-selectable values) multiplied by the gain of the difference amplifier (which is nominally set to 10). These parameters can vary from chip to chip and even across Clamp Units on the same chip, so calibration is required before accurate current measurements can be made.

This calibration should be repeated for every feedback resistance value that will be used. For each value of **feedback resistance** (Register N,3), set the **feedback capacitance** (Register N,4) to a value that yields a bandwidth $1 / (2\pi \cdot R_F C_F)$ of approximately 10 kHz.

1. Close the **voltage clamp connect** switch (Register N,7). Set the **input select** switch (Register N,8) to one of the calibration resistors (Rcal1 or Rcal2). Note that all four Clamp Units on the CLAMP4 chip share the same two calibration resistors, so only one Clamp Unit should be connected to these resistors at any time; this calibration procedure must be done sequentially for different channels on the same chip.
2. Set the **clamp step size** (Register N,1) of the clamp voltage generator to the 5 mV step size, which is slightly more accurate than the 2.5 mV step size.
3. Set **clamp voltage sign** and **clamp voltage magnitude** (Register N,0) to produce a desired clamp voltage. The voltage clamp will drive this voltage across the calibration resistor. The resulting current ($I = V_{clamp}/Rcal$) will be sensed by the current-to-voltage converter. The actual current-to-voltage "gain" may be measured using this known current.
4. Because the clamp voltage DAC has some small nonlinearities, a more accurate measurement will be obtained by measuring the current at several different clamp voltages (both positive and negative) and fitting a line to the resulting data points. When fitting data points, care should be taken to only fit data that falls within the current measurement range prescribed for each feedback resistance setting (see Register N,3 description for these ranges).
5. The user may wish to use two calibration resistors with resistances varying by a factor of 10 or 100 so that the small resistor may be used to calibrate the low feedback resistor values (i.e., 200 kΩ and 2 MΩ) while the other resistor may be used to calibrate the high feedback resistor values (i.e., 20 MΩ, 40 MΩ, and 80 MΩ).

Note on calibration resistor selection: The use of calibration resistors with values greater than 20 MΩ is not recommended unless extreme care is taken to remove residual solder flux from the circuit board after assembly and the board is kept free of oil and dirt from fingerprints and other sources of contamination. Touching a circuit board with a bare finger can easily create a conductive path of several hundred megohms. If this parasitic conductance falls in parallel with a high-valued calibration resistor, its effective resistance can change significantly. In most applications, a single calibration resistor in the range of 5-10 MΩ will suffice for accurate calibration of all feedback resistor values.

Calibration Step 6: Clamp Current Calibration

After the current-to-voltage converter has been calibrated, the clamp current generator may be calibrated by using this module to measure the output of the current source. This is achieved by setting the chip to produce a certain desired current, measuring the actual current using the current-to-voltage converter, and tuning the **current source scale** registers until the measured current matches the desired current.

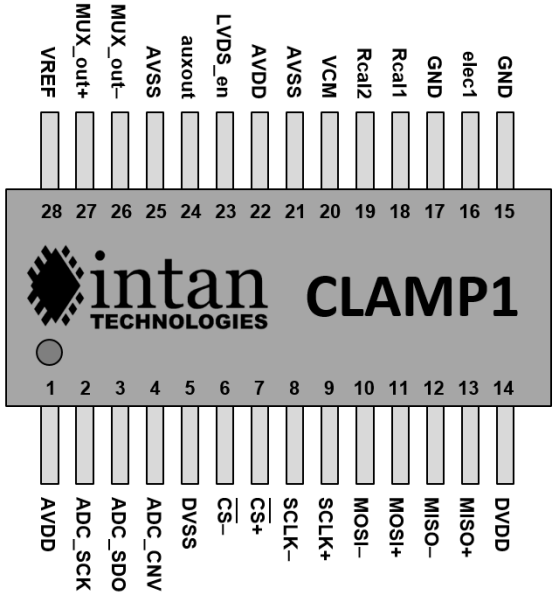
1. Set the **input select** switch (Register N,8) to open circuit. Close the **voltage clamp connect** switch (Register N,7). Set the **clamp voltage magnitude** (Register N,0) to zero. Close the **clamp current enable** switch (Register N,7).
2. Set **clamp current magnitude** (Register N,9) to its maximum value (i.e., 127).
3. Measure the resulting current using the voltage clamp circuit and adjust the **current source scale** registers (Registers N,10 – N,13) to achieve the desired current, which will be 127 times the value of the desired current step ($127 \cdot I_{step}$). Repeat for both positive and negative currents by setting **clamp current sign** (Register N,9) appropriately.

Note 1: When measuring the output of the current source with the current-to-voltage converter, try to select a value of feedback resistance that will yield an absolute output voltage ($V_{out} = 127 \cdot I_{step} \cdot R_F \cdot 10$) at the ADC between 0.3V and 1.5V. If the absolute value of voltage measured at the ADC exceeds 1.5V, use a smaller value of R_F. If the absolute voltage is below 0.3V, use a larger value of R_F.

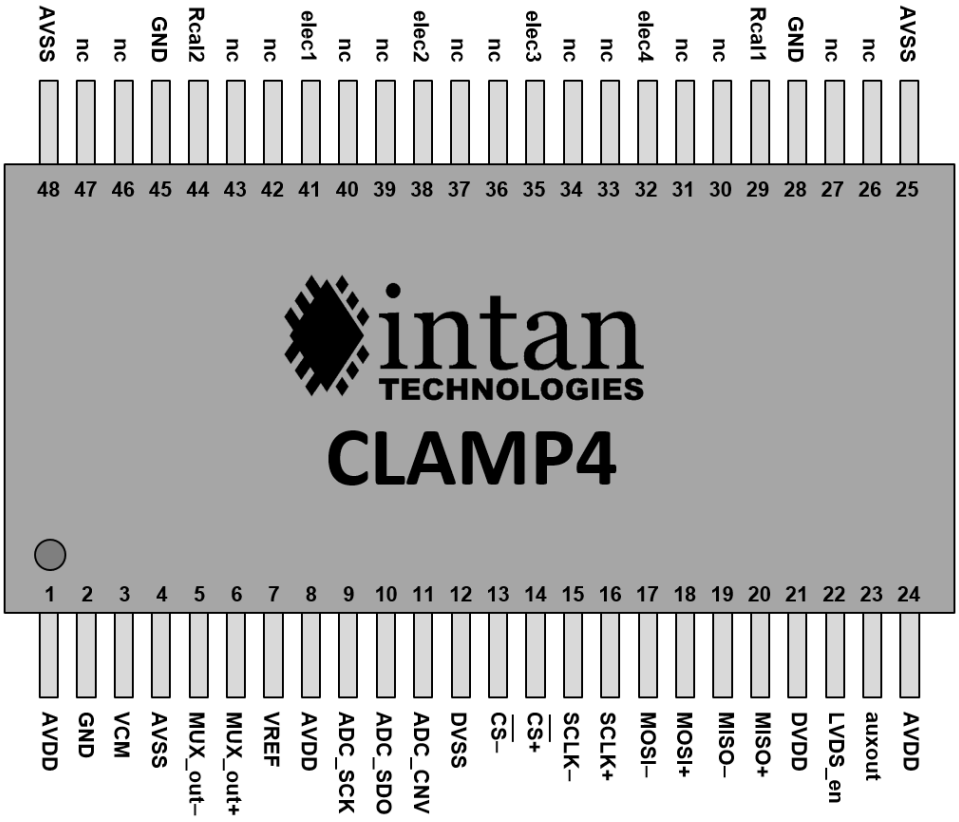
Note 2: If you are setting a relatively high value of current (e.g., 1 nA steps), you may find that the output of the current source exceeds the range of the current-to-voltage converter even when using the widest range (i.e., R_F = 200 kΩ). In this case, set the **clamp current magnitude** to 63 instead of 127 and adjust the current source scale registers to produce a measured current of $63 \cdot I_{step}$.

Package Description

CLAMP1: 28-Pin SSOP Package



CLAMP4: 48-Pin SSOP Package



nc = no connection; these pins should be left open or tied to ground.

Pin Descriptions

PIN	TYPE	FUNCTION
GND	power	System ground. All **GND** pins must be connected to the same potential. Tissue or bath should connected to this potential.
AVDD, DVDD	power	Positive power supply (+2.12 V - +2.32 V). These pins must be connected to the same potential.
AVSS, DVSS	power	Negative power supply (-1.28 V). These pins must be connected to the same potential.
VREF	power	Reference voltage (+1.28 V).
VCM	analog input	MUX output common-mode level control. This pin is normally tied to ground.
elec1, elec2, elec3, elec4	analog inputs/outputs	Voltage/current input/output for electrodes. Pins **elec2**, **elec3**, and **elec4** are not present on CLAMP1 chips.
Rcal1, Rcal2	analog inputs/outputs	Connections for optional off-chip precision resistors used for self-calibration.
LVDS_en	digital input	When **LVDS_en** is pulled high, communication with the SPI data bus is conducted using low-voltage differential signaling (LVDS). When **LVDS_en** is pulled low, SPI communication uses CMOS-level signaling with VDD/VSS voltage levels.
$\overline{\text{CS}}$+, $\overline{\text{CS}}$–	digital LVDS input pair	Active-low chip select input for SPI data bus. The falling edge of this signal is also used to trigger an ADC sample. If **LVDS_en** is pulled low, only **$\overline{\text{CS}}$+** is used as a CMOS-level input. If **LVDS_en** is pulled high, both pins are used as an LVDS input pair.
SCLK+, SCLK–	digital LVDS input pair	Serial clock input for SPI data bus. The base value of the clock is zero (CPOL = 0). If **LVDS_en** is pulled low, only **SCLK+** is used as a CMOS-level input. If **LVDS_en** is pulled high, both pins are used as an LVDS input pair.
MOSI+, MOSI–	digital LVDS input pair	Serial data input ("Master Out, Slave In") for SPI data bus. The CLAMP chip always acts as slave in an SPI data link. This line is sampled on the rising edge of SCLK. If **LVDS_en** is pulled low, only **MOSI+** is used as a CMOS-level input. If **LVDS_en** is pulled high, both pins are used as an LVDS input pair.
MISO+, MISO–	digital LVDS output pair	Serial data output ("Master In, Slave Out") for SPI data bus. The CLAMP chip always acts as slave in an SPI data link. The value of this line changes in response to a falling edge on SCLK. If **LVDS_en** is pulled low, only **MISO+** is used as a CMOS-level output. If **LVDS_en** is pulled high, both pins are used as an LVDS output pair.
MUX_out+, MUX_out–	analog output pair	Differential analog multiplexer (MUX) output. These lines should be connected to the differential input of the external ADC. On the CLAMP1 chip, an anti-alias filter capacitor should be tied across these pins.
ADC_CNV, ADC_SCK	digital outputs	Conversion and serial clock control lines for external ADC.
ADC_SDO	digital input	Serial data input from external ADC.
auxout	digital output	This pin is an auxiliary CMOS digital output that is controlled by setting registers on the chip. If not used, this pin should be left unconnected. This pin should never be tied to a power bus, as the operation of this pin is undefined at power-up.

Electrical Characteristics

T_A = 25ºC, V_{DD} = +2.22V, V_{SS} = -1.28V, V_{REF} = +1.28V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNITS	COMMENTS
V_{DD}	Positive Supply Voltage		+2.12 – +2.32	V	Recommended nominal supply voltage is 2.22 V.
V_{SS}	Negative Supply Voltage		-1.28	V	±2% recommended.
V_{REF}	Reference Voltage		+1.28	V	±2% recommended.
$V_{clamp\text{-}range}$	Voltage Clamp Range	step size = 2.5 mV step size = 5.0 mV	±637.5 ±1.275	mV V	Voltage clamp range is set by V_{REF} and V_{SS}.
$I_{clamp\text{-}range}$	Current Clamp Range	step size = 5 pA step size = 50 pA step size = 500 pA step size = 1 nA	±635 ±6.35 ±63.5 ±127	pA nA nA nA	
$V_{meas\text{-}range}$	Voltage Measurement Range		±300	µV	Referred to electrode.
v_{ni}	Voltage Measurement Noise Floor (to 10 kHz)	50 kS/s 50 kS/s, C_{aa} = 4.7 nF 200 kS/s, C_{aa} = 4.7 nF	54 15 12	μV_{rms}	Typical. See below for more details.
$I_{meas\text{-}range}$	Current Measurement Range		±1.2	µA	Referred to electrode.
i_{ni}	Current Measurement Noise Floor (to 5 kHz)	<u>range = ±6.0 nA</u> 50 kS/s 50 kS/s, C_{aa} = 4.7 nF 200 kS/s, C_{aa} = 4.7 nF <u>range = ±12 nA</u> 50 kS/s 50 kS/s, C_{aa} = 4.7 nF 200 kS/s, C_{aa} = 4.7 nF <u>range = ±120 nA</u> 50 kS/s 50 kS/s, C_{aa} = 4.7 nF 200 kS/s, C_{aa} = 4.7 nF <u>range = ±1.2 µA</u> 50 kS/s 50 kS/s, C_{aa} = 4.7 nF 200 kS/s, C_{aa} = 4.7 nF	 3.0 2.6 2.1 3.0 3.0 2.7 14 11 10 120 70 69	 pA_{rms} pA_{rms} pA_{rms} pA_{rms} pA_{rms} pA_{rms} pA_{rms} pA_{rms} pA_{rms} pA_{rms} pA_{rms} pA_{rms}	Typical. Range is set by selection of feedback resistor R_F in current-to-voltage converter. See previous pages for more details.
$C_{P\text{-}comp}$	Fast Transient Capacitive Compensation Range	step size = 0.05 pF step size = 0.07 pF step size = 0.08 pF step size = 0.10 pF	0 – 10 0 – 14 0 – 16 0 – 20	pF pF pF pF	Set in Register N,8.

Electrical Characteristics

T_A = 25ºC, V_{DD} = +2.22V, V_{SS} = -1.28V, V_{REF} = +1.28V unless otherwise noted.

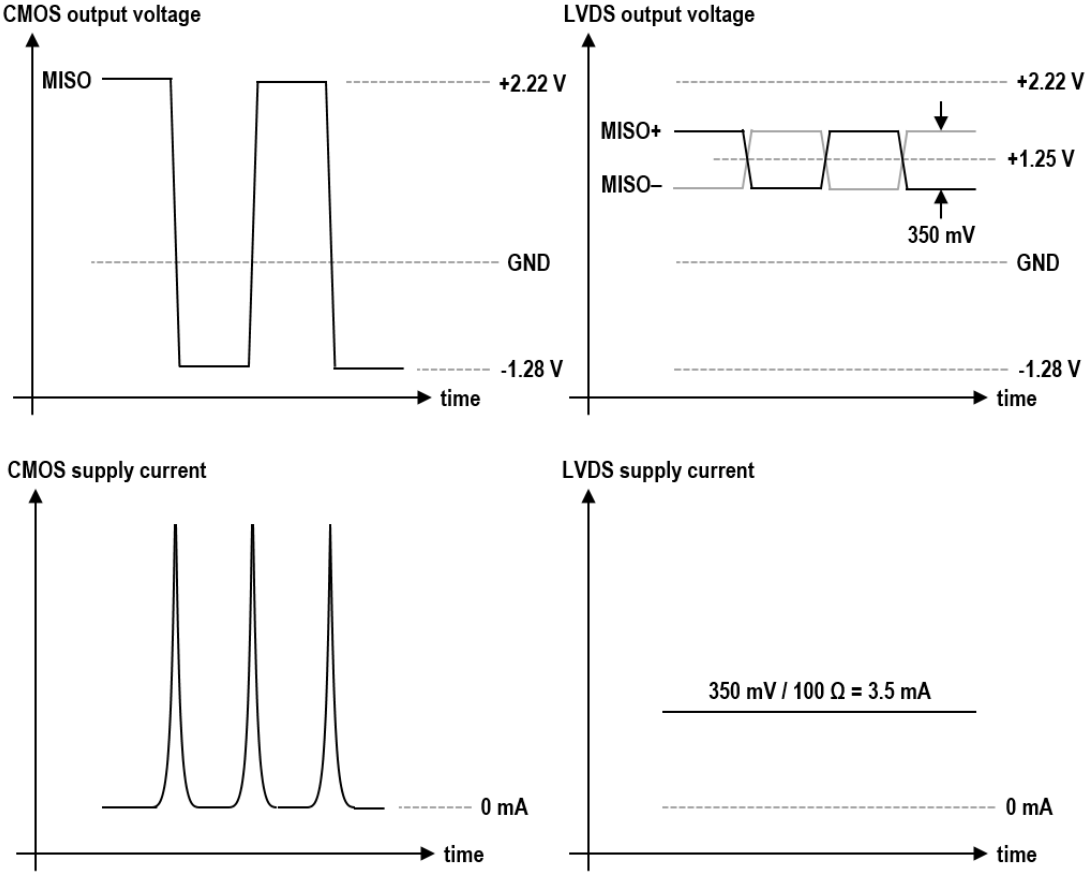
SYMBOL	PARAMETER	CONDITIONS	VALUE	UNITS	COMMENTS
$Z_{diginCMOS}$	CMOS Digital Input Impedance	LVDS_en = 0	5	pF	
$Z_{diginLVDS}$	LVDS Digital Input Impedance	LVDS_en = 1	150	kΩ	LVDS inputs are weakly pulled to V_{DD} if unconnected. User must add 100 Ω termination.
V_{inLO}	CMOS Digital "Low" Input Voltage	For all non-LVDS digital inputs to chip	-1.7 – -0.6	V	Nominal "low" input voltage is V_{SS} (-1.28 V).
V_{inHI}	CMOS Digital "High" Input Voltage	For all non-LVDS digital inputs to chip	+1.32 – +2.32	V	+2.5V, +3.3V, or +5V signals should not be applied to chip.
$V_{inLVDS-CM}$	LVDS Input Common-Mode Voltage		1.0 – 1.5	V	Suggested common-mode level is 1.25 V.
$V_{inLVDS-D}$	LVDS Input Differential Voltage		±250 – ±500	mV	Suggested differential voltage is ±350 mV.
$V_{outLVDS-CM}$	LVDS Output Common-Mode Voltage		1.25	V	Typical
$V_{outLVDS-D}$	LVDS Output Differential Voltage	With 100 Ω termination	±350	mV	Typical
I_{DD}	Positive Supply Current	LVDS_en = 0			Typical
		CLAMP1	2.3	mA	
		CLAMP4	9.0	mA	
		LVDS_en = 1			
		CLAMP1	8.0	mA	
		CLAMP4	14.7	mA	
I_{SS}	Negative Supply Current	LVDS_en = 0			Typical
		CLAMP1	2.3	mA	
		CLAMP4	9.4	mA	
		LVDS_en = 1			
		CLAMP1	8.1	mA	
		CLAMP4	15.0	mA	
I_{REF}	Reference Current	CLAMP1			Typical
		step size = 2.5 mV	0.04	mA	
		step size = 5.0 mV	0.08	mA	
		CLAMP4			
		step size = 2.5 mV	0.15	mA	
		step size = 5.0 mV	0.30	mA	
P_S	Total Power Dissipation	LVDS_en = 0			Typical
		CLAMP1	8.1	mW	
		CLAMP4	32	mW	
		LVDS_en = 1			
		CLAMP1	28	mW	
		CLAMP4	52	mW	

Electrical Characteristics

T_A = 25ºC, V_{DD} = +2.22V, V_{SS} = -1.28V, V_{REF} = +1.28V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNITS	COMMENTS
S_{chip}	Size of Packaged Chip	CLAMP1 CLAMP4	9.9 × 6.0 15.9 × 10.3	mm^2 mm^2	28-pin plastic SSOP package 48-pin plastic SSOP package
m_{chip}	Mass of Packaged Chip	CLAMP1 CLAMP4	140 600	mg mg	
S_{die}	Size of Bare Die	CLAMP1 CLAMP4	2.0 × 3.6 3.8 × 3.7	mm^2 mm^2	Bare silicon die (0.20 mm thick)
m_{die}	Mass of Bare Die	CLAMP1 CLAMP4	4 7	mg mg	

Digital Signaling Modes



The CLAMP chips communicate over a standard digital Serial Peripheral Interface (SPI) bus. The bus protocol and data structures used are described in later sections. The voltage levels used to send digital signals over this bus can assume one of two forms: CMOS signaling or low-voltage differential signaling (LVDS). The above figure illustrates the differences between a digital value (e.g., MISO) transmitted using these two signaling methods.

CMOS Signaling

CMOS signaling (upper left) transmits a digital zero or one by switching the voltage on a single output wire between V_{SS} (-1.28 V) and V_{DD} (typically +2.22 V). **It is important to note that the CMOS signaling used by the CLAMP chips does not use standard voltage levels. Digital zero is conveyed by -1.28 V and digital one is conveyed by +2.22 V.**

The current drawn from the power supply (lower left) is nearly zero until the output switches state; at this point, a burst of current is pulled from the power supply to charge or discharge the capacitance of the output wire. These bursts of supply current introduce high frequency noise to the on-chip power supply; this noise can adversely affect noise levels. For typical data streams containing similar numbers of ones and zeros, the dynamic power dissipation of a CMOS output driving a wire with capacitance C_{wire} at R bits/s is

$$P = \frac{1}{2} C_{\text{wire}} (V_{\text{DD}} - V_{\text{SS}})^2 R.$$

(The actual power dissipation will be slightly higher than this due to secondary effects like the momentary short-circuit current that leaks through CMOS circuits every time they switch state.)

If we operate a CLAMP chip at a sampling rate of 400 kS/s, the data rate R is 400 kHz × 32 bits = 12.8 Mbit/s. Typical coaxial cables have a capacitance of 100 pF/m. The power required to transmit 12.8 Mbit/s over a 2.0 m cable is approximately 14 mW.

Transmitting high-frequency data reliably over long wires is challenging due to the presence of reflections that occur when a propagating signal reaches the high-impedance input of a digital receiver. These reflections interfere with the transmitted signal and corrupt the data stream. The characteristic impedance Z_0 of a cable is given by

$$Z_0 = \sqrt{L/C}$$

where L is the cable inductance per unit length and C is the cable capacitance per unit length. For most common cable geometries (e.g., coaxial, twisted pair, ribbon), Z_0 falls in the range of 50 – 200 Ω. To eliminate reflections, the cable must be terminated with a parallel resistance equal to Z_0.

CMOS digital outputs lack the current sourcing capability to drive the high DC currents necessary to support CMOS-level signals (i.e., 3.3V) across such small resistances, so proper cable termination cannot be used in these cases. A series resistor with a value of Z_0 placed near a CMOS digital output can prevent multiple reflections from the high-impedance input at the far end of a cable by absorbing the first reflection, but this is an imperfect solution that fails with high data rates or long cables.

LVDS Signaling

LVDS signaling (upper right, previous page) uses a pair of wires (e.g., **MISO+** and **MISO–**) to transmit each digital signal; the wires are terminated with a 100 Ω resistor tied between them near the LVDS receiver. The average voltage on the wire pair is held roughly at +1.25V, and a 3.5 mA current is forced through the wires in one direction or the other, creating a ±350 mV differential voltage across the terminating resistor to signal a digital one or zero.

LVDS signaling offers several advantages over CMOS signaling. First, the use of terminated wires drastically reduces reflections, maintaining high signal integrity on long wires and at high data rates. Second, the use of small differential voltages greatly reduces crosstalk to other nearby wires in a cable bundle, especially if twisted pairs are used. Electromagnetic interference and emissions are also minimized using LVDS signaling. Finally, the current drawn from the power supply of the LVDS transmitter is nearly constant (lower right, previous page). This constant current draw does not introduce noise to the on-chip power supply. Thus, LVDS signaling is far better suited for low-noise operation on a chip containing both analog and digital components.

The minimum power dissipation of an LVDS transmitter is given by $(V_{DD} – V_{SS})\cdot(3.5\text{ mA}) = 12.3\text{ mW}$ using a 3.5V power supply (i.e., V_{DD} = +2.22 V and V_{SS} = -1.28 V). At low frequencies and short wire lengths, CMOS signaling can operate at far lower power levels. However, as the calculations in the previous section demonstrate, LVDS can operate at lower power levels when data rates are high and wires are long.

Cables several meters in length can be used with LVDS signaling as long as the geometry of the cable is fairly consistent along its length. Twisted pairs are particularly good structures for LVDS signaling, and many standard cables contain multiple twisted pairs (e.g., USB, HDMI). The DC series resistance of the cable typically has no effect on the performance of the system as long as it is much less than the terminating resistance of 100 Ω. Signals propagate along standard cables at approximately two-thirds the speed of light, or 20 cm/ns, so a five-meter cable will introduce a round-trip delay of around 50 ns. As long as the SPI controller accounts for these delays, long cables may be used to communicate with a CLAMP chip reliably.

The LVDS inputs and outputs on the CLAMP chips use industry-standard LVDS signal levels. Many commercially available FPGAs and microcontrollers have built-in LVDS I/O pins, and can be interfaced directly with the CLAMP. If a controller lacks LVDS I/O, a wide variety of commercially available LVDS-to-standard-CMOS driver and receiver interface chips may be used to translate signal levels (e.g., TI SN65LVDS, SN65LVDT, DS90LV, and DS90C lines; Fairchild FIN10xx line).

Selecting Signaling Modes on CLAMP Chips

If the **LVDS_en** pin on a CLAMP chip is tied to DVSS, the SPI bus operates with CMOS signals, using a single wire for each digital signal. The digital input pins on the CLAMP interpret any voltage below -0.6 V as logic "low" and any voltage above +1.1 V as logic "high", so the chip can be interfaced with standard 2.5 V, 3.0 V, or 3.3 V signals, as long as these signals are referenced to a -1.28 V, not ground. **Digital inputs to the CLAMP should not go more than 0.4V below DVSS, and should never exceed +2.32 V.** Digital outputs from the CLAMP chip are driven to V_{SS} (-1.28V) for logic "low" and to V_{DD} (+2.22 V) for logic "high".

If the **LVDS_en** pin is tied to V_{DD}, the SPI bus operates in LVDS mode, where every signal in the SPI bus is represented by a differential voltage across a pair of wires (e.g., **SCLK+** and **SCLK–**). The LVDS inputs on CLAMP chips expect a common-mode voltage near +1.25 V and differential signals near ±350 mV, but are fairly tolerant of moderate variations in these values. The LVDS inputs do not include on-chip termination, so a 100 Ω resistor should be placed between each LVDS input signal pair near the chip. Connection diagrams on the following pages provide examples of termination schemes.

Enabling LVDS mode on a CLAMP chip increases current consumption by approximately 5.7 mA. This includes the 3.5 mA of current driven through the MISO output as well as current to power the three on-chip LVDS receivers for $\overline{CS}$, SCLK, and MOSI. (Commercial LVDS interface chips typically consume over 17 mA to perform the same functions as the CLAMP chip LVDS I/O system.)

Increased Noise Levels with CMOS Signaling

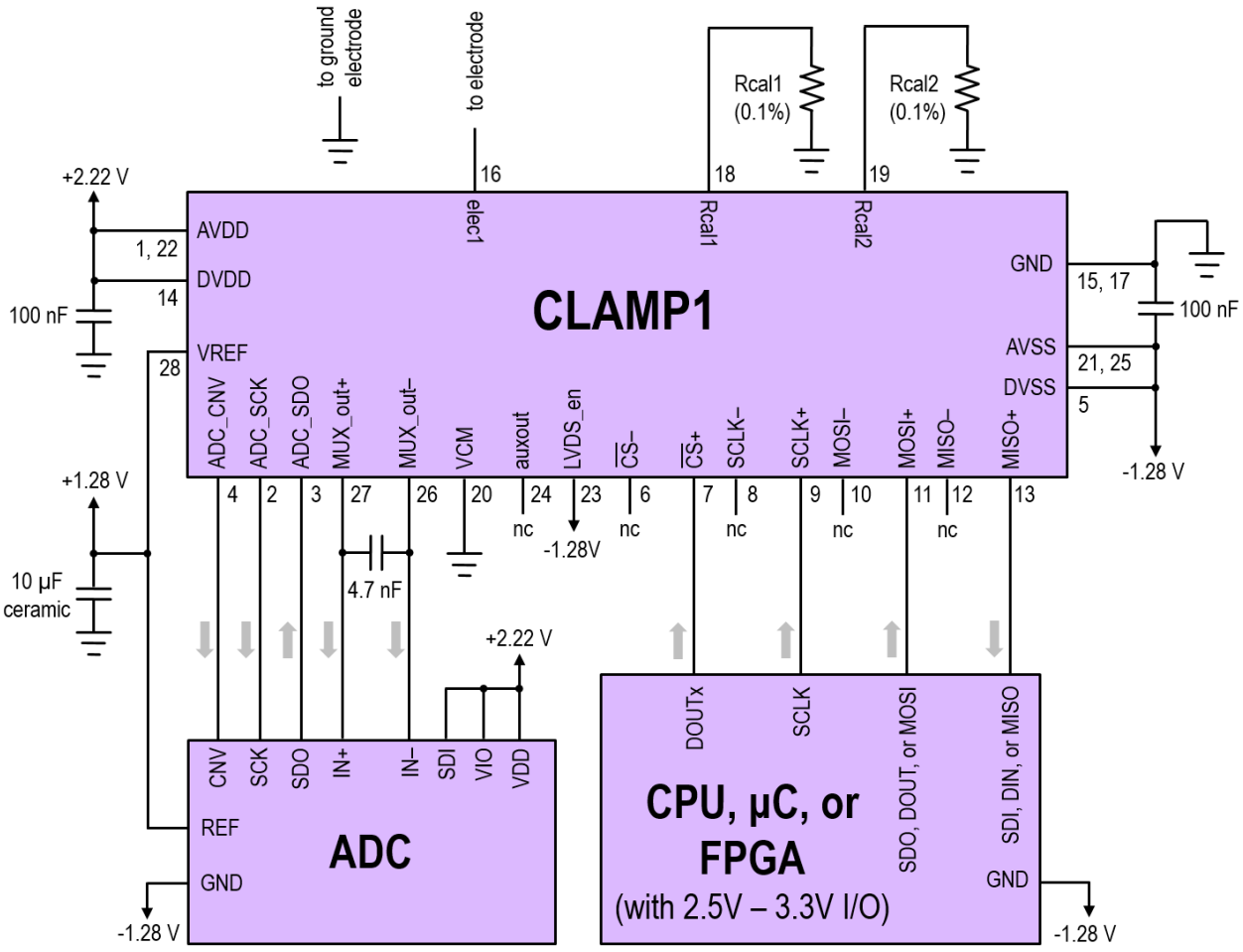
If CMOS signaling is used, the noise levels on the CLAMP chips will rise above their nominal values. Using long, high-capacitance wires will likely increase the amplifier noise level further.

Typical CLAMP1 Connection Diagram

CMOS SPI INTERFACE (LVDS_en = 0)

The diagram below shows a typical circuit schematic for a CLAMP1 chip interfaced to a controller that is located in close proximity and uses a CMOS four-wire SPI interface.

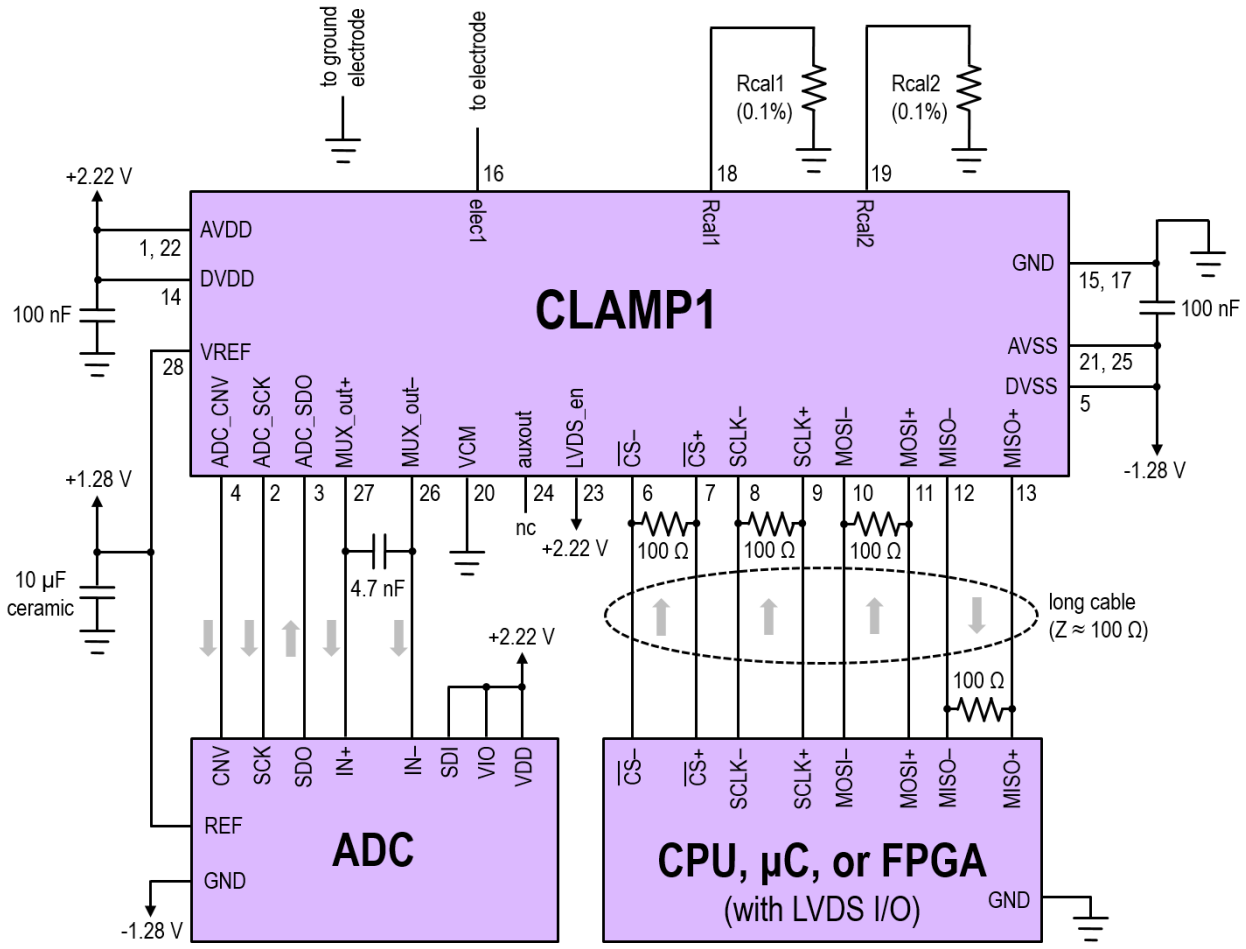
Note that the ADC ground and the digital controller ground are connected to -1.28V.



LVDS SPI INTERFACE (LVDS_en = 1)

The diagram below shows a typical circuit schematic for a CLAMP1 chip interfaced to a controller over a long cable, using an SPI interface with low-voltage differential signaling and 100 Ω termination resistors.

Note that the ADC ground is connected to -1.28V



Anti-Aliasing Filter Capacitor

The noise floor of the CLAMP1 chips can be lowered significantly by adding an external 4.7 nF capacitor across the **MUX_out+** and **MUX_out–** pins, as shown in the schematics above. This capacitor limits the bandwidth of the CLAMP1 multiplexer output and attenuates high-frequency noise that exceeds the Nyquist frequency (i.e., half the sampling frequency) of the ADC. Noise above this frequency is aliased back into the pass band, increasing the noise floor significantly, particularly in current clamp mode.

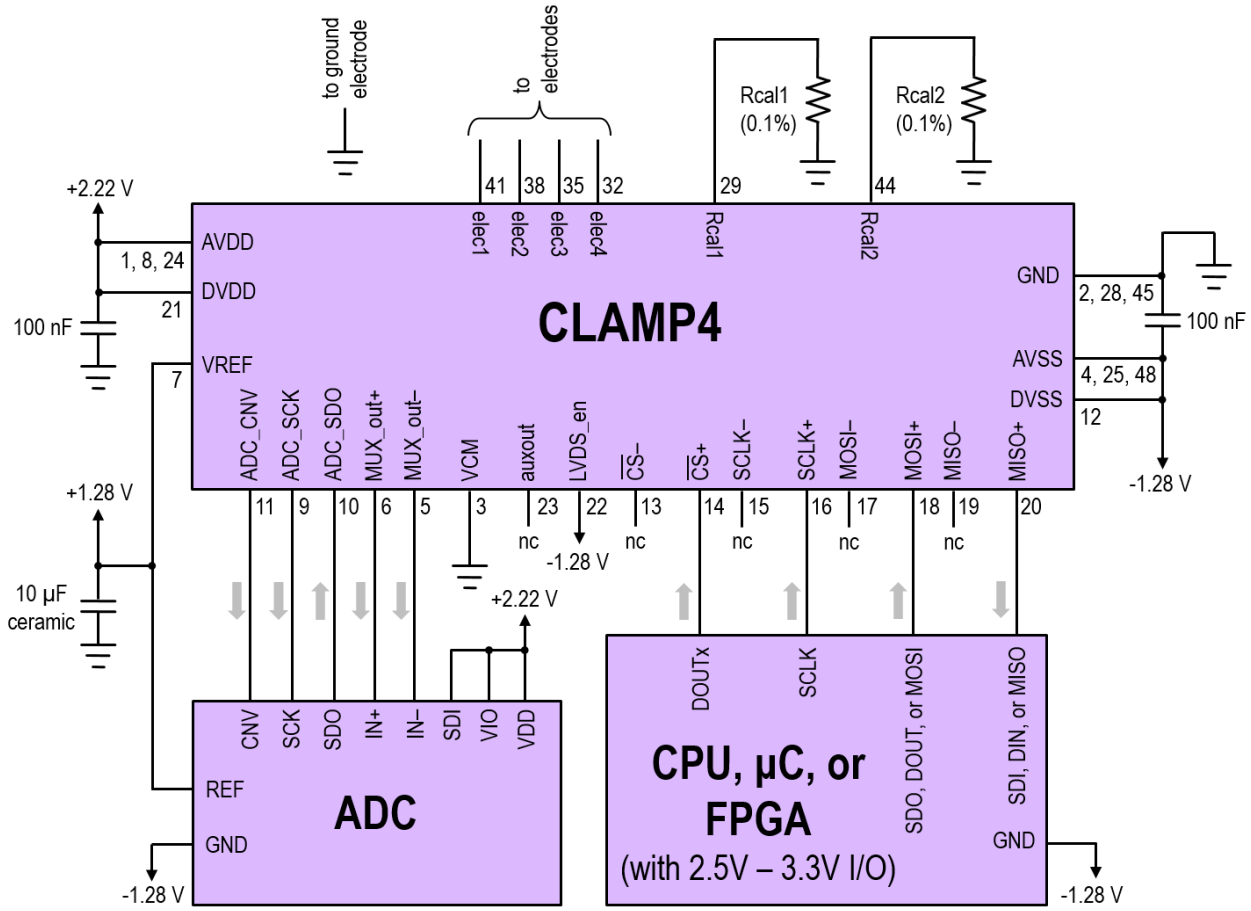
This anti-aliasing capacitor can only be used with the CLAMP1 chip, where the multiplexer dwells on one channel. In normal CLAMP4 operation that multiplexer scans rapidly between all four channels, and any anti-aliasing capacitor would interfere with this multi-channel sharing of the ADC.

Typical CLAMP4 Connection Diagram

CMOS SPI INTERFACE (LVDS_en = 0)

The diagram below shows a typical circuit schematic for a CLAMP4 chip interfaced to a controller that is located in close proximity and uses a CMOS four-wire SPI interface.

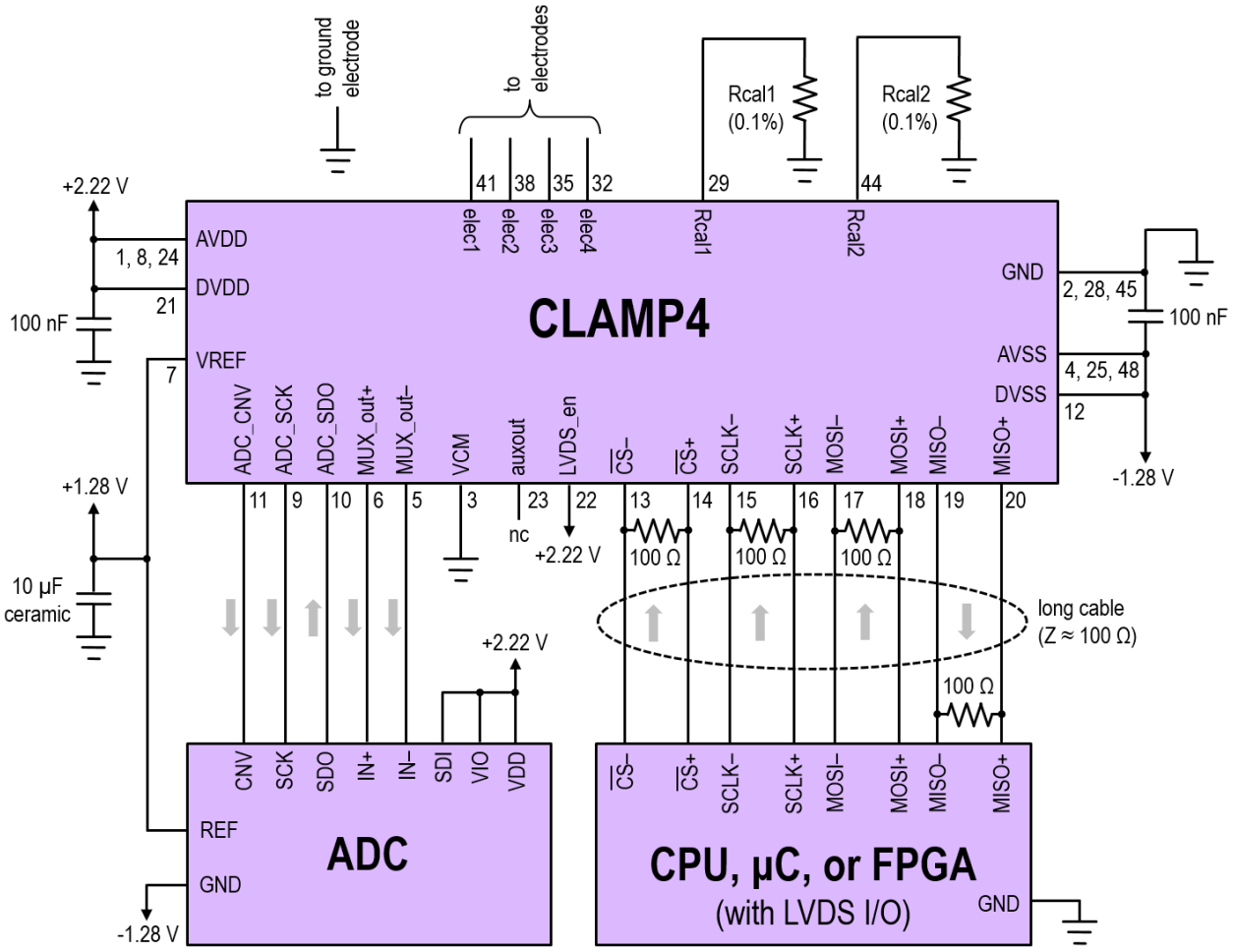
Note that the ADC ground and the digital controller ground are connected to -1.28V.



LVDS SPI INTERFACE (LVDS_en = 1)

The diagram below shows a typical circuit schematic for a CLAMP4 chip interfaced to a controller over a long cable, using an SPI interface with low-voltage differential signaling and 100 Ω termination resistors.

Note that the ADC ground is connected to -1.28V



ADC Selection

The following ADCs may be used with CLAMP chips:

Manufacturer	Part Designation	Resolution	Total Sampling Rate
Analog Devices	AD7687	16 bit	200 kS/s
Analog Devices	AD7691	18 bit	180 kS/s
Texas Instruments	ADS8865	16 bit	400 kS/s
Texas Instruments	ADS8885	18 bit	400 kS/s

The sampling rate cited is valid for an ADC power supply voltage of 3.5 V (i.e., ADC VDD connected to the +2.22V supply and ADC GND connected to the -1.28V supply). All ADCs listed here have same pinout and are available in small 10-lead MSOP (mini small outline) or LFCSP (lead frame chip scale) packages from many third-party vendors (e.g., Digi-Key, Mouser, Newark).

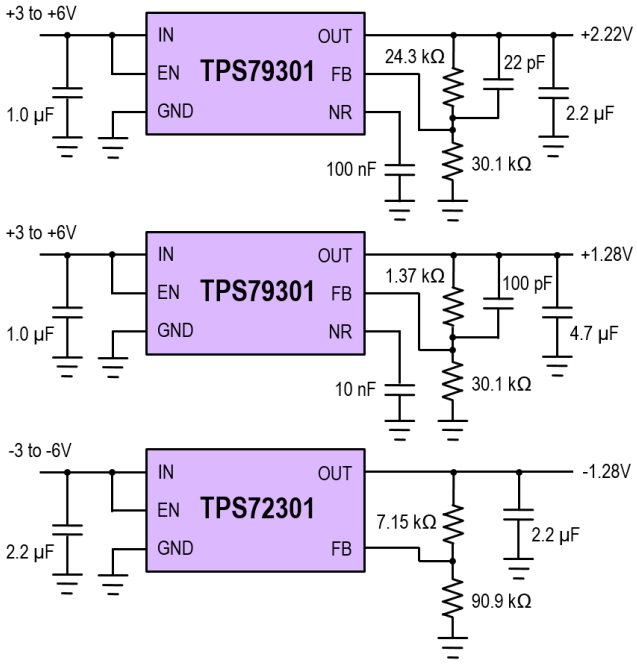
The **18 bit ADC** variable in Register 15,3 should be set to one if an 18-bit ADC is used or zero if a 16-bit ADC is used.

Recommended Support Circuitry

The CLAMP chip requires three voltage supplies: a positive supply V_{DD} which must lie between +2.12V and +2.32V (with a recommended value of +2.22V), a negative supply V_{SS} which should have a precise level of -1.28V ± 2%, and a reference voltage V_{REF} which should have a precise level of +1.28V ± 2%. The external ADC should be powered from the V_{DD} and V_{SS} supplies (not from ground), as shown on the previous two pages, with V_{REF} used as the ADC reference voltage.

Many semiconductor companies provide small, inexpensive low-dropout (LDO) adjustable voltage regulators whose output voltage can be set using two external resistors. Precision (1% or better) resistors should be used to ensure accurate voltage levels. The use of linear voltage regulators is essential; switching voltage regulators generate high levels of noise in the kHz range that can adversely affect the sensitivity and accuracy of the CLAMP chip.

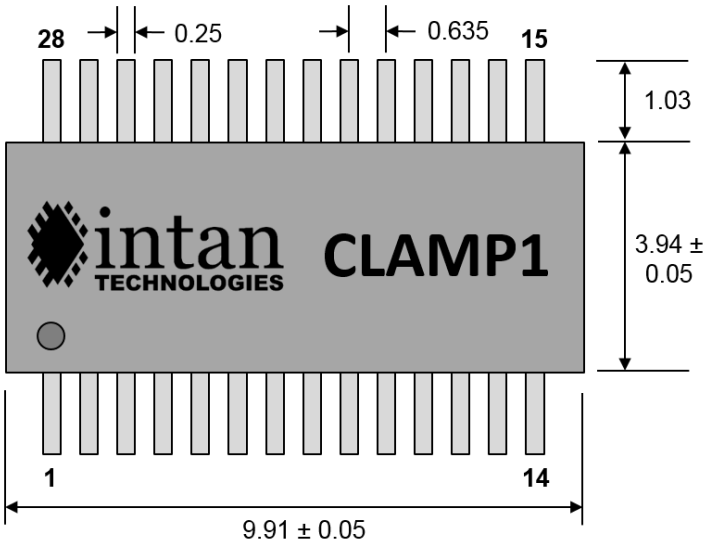
The following schematic shows an example circuit that generates these voltage supplies from a ±3V to ±6V supply using the TPS79301 adjustable linear positive regulator and TPS72301 adjustable linear negative regulator from Texas Instruments. Whichever voltage regulators are used, the datasheets of the regulators should be studied carefully to guide in the optimal selection of external resistor and capacitors. All capacitors should be ceramic capacitors with voltage ratings of at least 16V. (While each capacitor will only be exposed to a few volts, small surface-mount device (SMD) capacitors are known to dramatically decrease in capacitance as the voltage across the device approaches the maximum rated voltage. It is best to use a capacitor with a voltage rating several times higher than the expected voltage.) Voltage regulators should be placed reasonably near the CLAMP chip and its external ADC, with additional bypass capacitors placed near these chips as shown on the previous two pages.



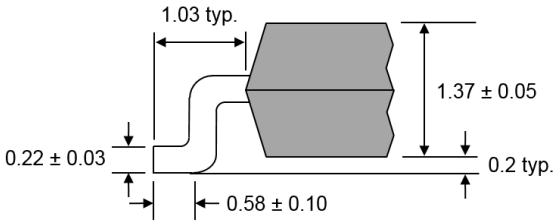
CLAMP1 Package Dimensions

All dimensions are in millimeters.

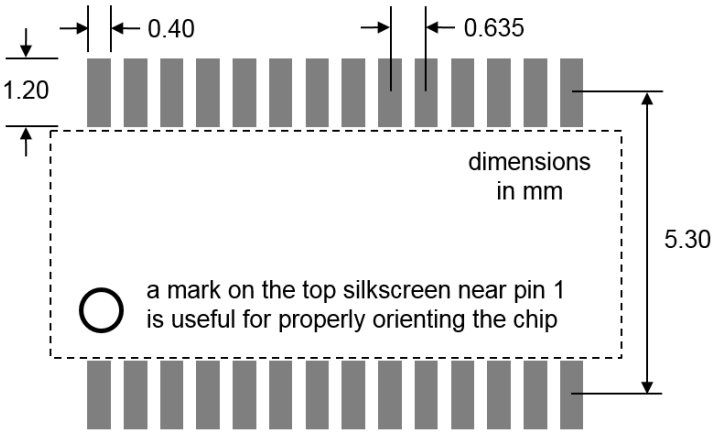
28-Pin SSOP Package: Top View



28-Pin SSOP Package: Side View



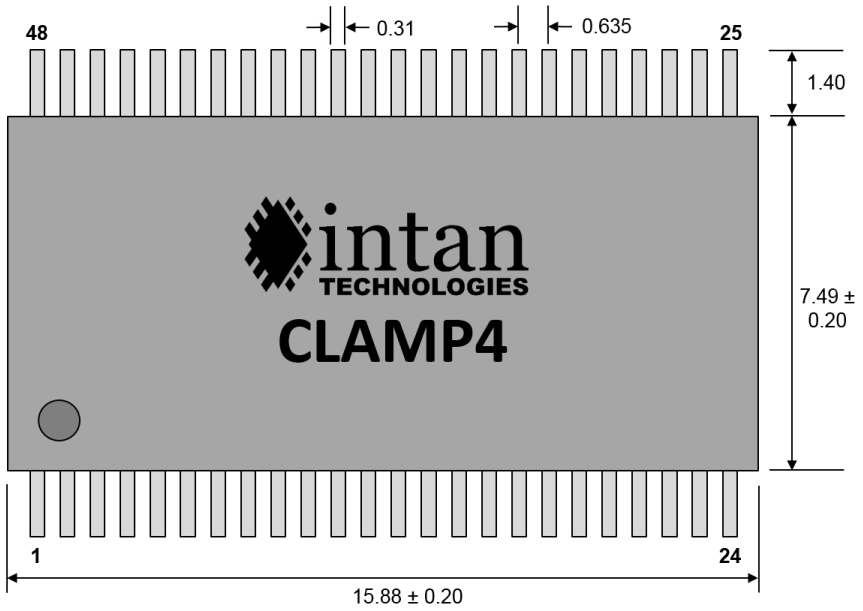
CLAMP1 Printed Circuit Board Layout



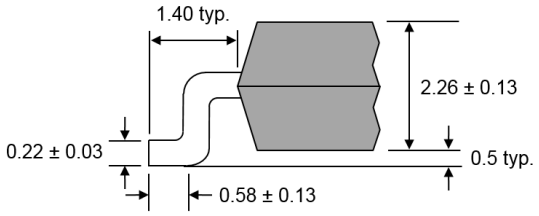
CLAMP4 Package Dimensions

All dimensions are in millimeters.

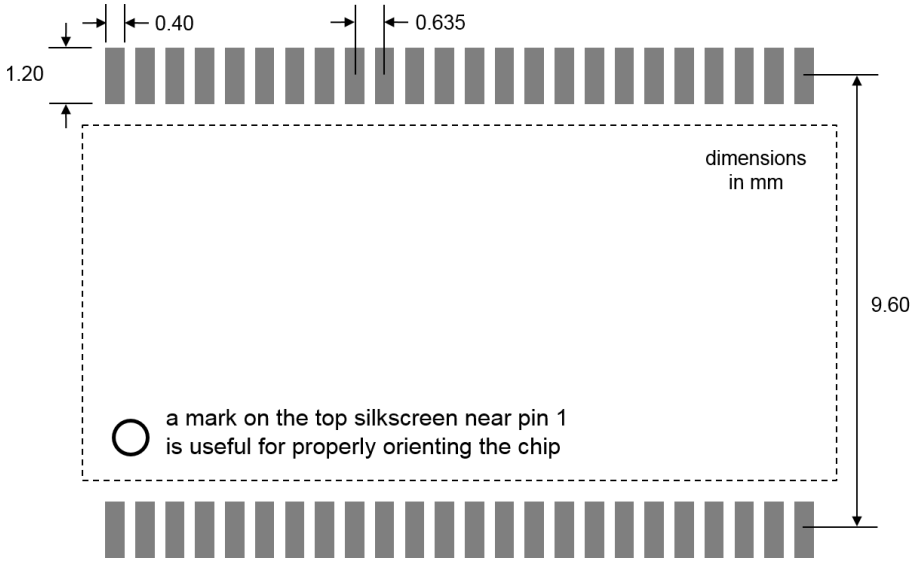
48-Pin SSOP Package: Top View



48-Pin SSOP Package: Side View



CLAMP4 Printed Circuit Board Layout

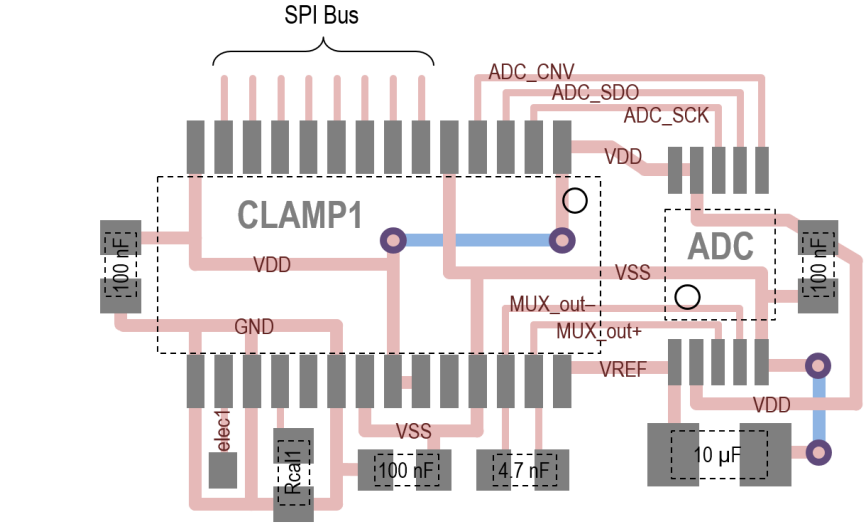


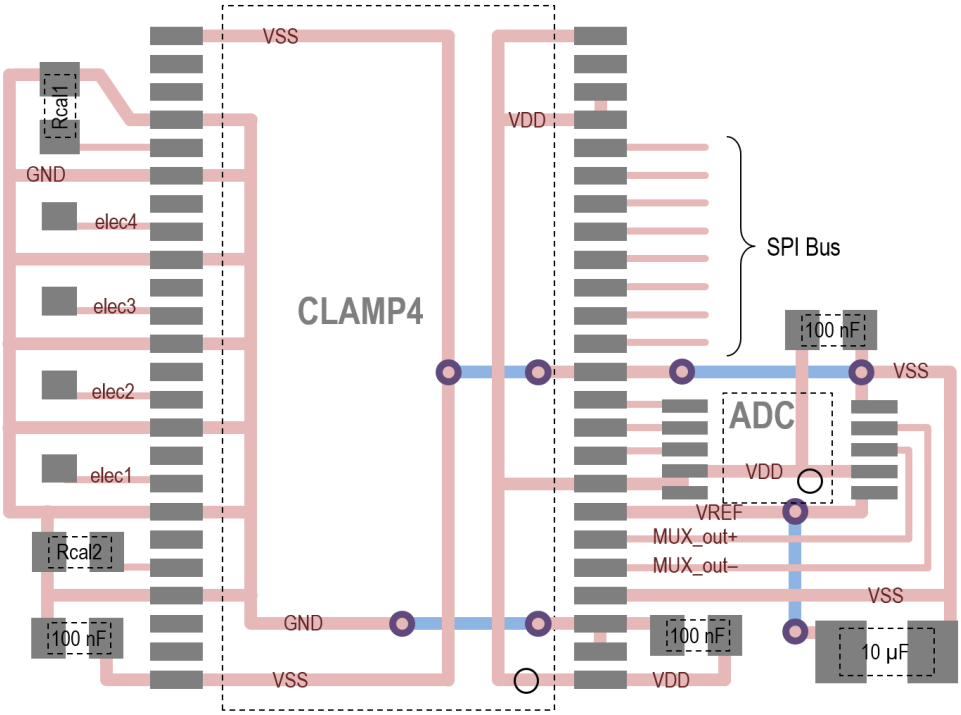
Sample Printed Circuit Board Layout

The I/O pins of the CLAMP chips are oriented to facilitate positioning the external ADC nearby to reduce the opportunity for interference or noise pickup. The diagrams below show sample printed circuit board (PCB) layouts for the CLAMP1 and CLAMP4 chips with the external ADC (in MSOP package) and associated bypass capacitors. These layouts can be improved further by placing some components (e.g., the 10 µF capacitor) on the bottom of the PCB to reduce trace lengths.

Note that ground traces encircle completely the electrode pins and Rcal pins to provide lateral shielding and to block possible surface currents. If currents in the low picoamp range will be measured, it is recommended to lift each electrode pin off the PCB after board assembly and solder a wire directly from the raised pin to the electrode connector to eliminate any possible path for leakage conductance on the PCB surface due to residual solder flux or oil from handling.

A ground plane (not shown) should always be used underneath the CLAMP chip and ADC, but the ground plane can be eliminated directly underneath the electrode pins to reduce parasitic capacitance (i.e., contributions to C_P) on these critical nodes. The datasheet of the ADC should also be consulted for PCB layout recommendations and best practices.





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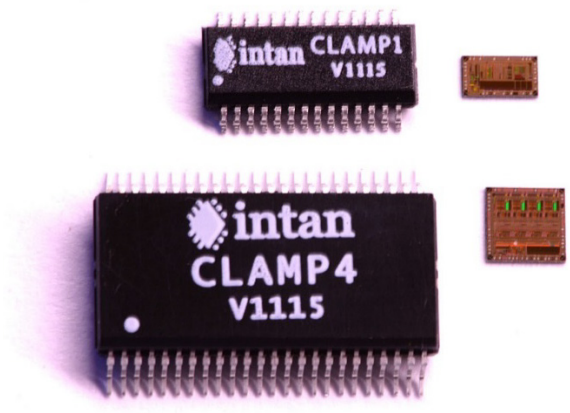

Contact Information

This datasheet is meant to acquaint engineers and scientists with the general characteristics of the CLAMP voltage/current clamp amplifier chips developed at Intan Technologies. We value feedback from potential end users. We can discuss your specific needs and suggest a custom integrated solution tailored to your applications.

For more information, contact Intan Technologies at:

intan TECHNOLOGIES, LLC

www.intantech.com
info@intantech.com