

## Overview

Niagara 32265 Dual Port Gigabit Ethernet Server Adapter is built on Intel's 82576 Gigabit technology & Interface Masters' sterling design and customer service.

Niagara 32265 is designed with a built-in programmable bypass circuit to provide maximum uptime for the network. The bypass circuit takes the Niagara 32265 ports offline in case of either power or software failure. The bypass circuit works in absence of power.

Niagara 32265 Dual Port Copper Gigabit Ethernet NIC is designed to integrate with PCI Express compatible servers and high-end appliances providing high speed networking and bypass/failover capabilities for any mission-critical application.



## Features

- Intel 82576EB Dual MAC & PHY ethernet controller
- Peak bandwidth 2.5 Gb/s in each direction per PCI Express lane
- 4 Gigabit per second of traffic when fully utilized
- PCI-E x4 (Gen 2.0) compatible
- Two RJ45 Connectors
- Passive Bypass which is essential during power loss or software failure
- Link Fault Detection (LFD) support
- Programmable "Fail-Closed" or "Fail-Open" while in the power-off state
- Programmable independent mode to function as a dual port gigabit copper card
- Integrated PHY for full and half-duplex 10/100/1000 Base-T Support
- TCP/UDP/IP checksum offload and TCP segmentation
- IEEE 802.1q, 802.3ab, 802.3u, 802.3x compliant
- Layer 2, 3 and 4 Advanced packet filtering capabilities (IPv4, IPv6)
- Efficient form factor – 5.2 inches in length and 2.64 inches in height

- Low Power Consumption (3.7W maximum power)
- Full RoHS compliance
- FCC Class A and CE certification

## Component Specifications

The Intel 82576 provides support for:

- PCI Express 2.0 (2.5GT/s)
- Low Power 2.4W
- Protocols: TCP, UDP & SCTP
- Queues per port: (16) Tx & (16) Rx Queues
- Enhanced Virtualization Support
  - » VMDq2 & PCI SIG IOV
- Intel® I/OAT Acceleration v3.0
  - » VM Direct Assignment (VT-d)
- Data Center Ethernet
  - » Traffic Classes (802.1q): 2
  - » Flow Interrupt Priority (802.3ar)
  - » Priority Grouping (802.1P)
- End-to-End Congestion Mgmt (802.1 PAR)
- IEEE 1588 Support
  - » Manageability interfaces
    - ⇒ RMII, SMBus, PXE, iSCSI Boot
- Layer 2 & 3 Security: IPSec & LinkSec

## Environmental

<b>Operating Humidity</b>	0%–90%, non-condensing
<b>Operating Temperature</b>	0°C – 50°C (32°F - 122°F)
<b>Storage Temperature</b>	-20°C – 65°C (-4°F – 149°F)

## Dimensions

	mm	inches
<b>Length</b>	132.08	5.2
<b>Height</b>	67.056	2.64

## Ordering Part Numbers

Part Number	Description
Niagara 32265	Dual Port Copper Gigabit NIC with Bypass

## Product Line

- External Bypass Systems/Switches 1Gb and 10Gb
- External 1GE and 10GE Aggregation TAP system
- Special Server Adaptors/NIC cards supporting
  - » Multi Port NIC cards - Copper, Fiber MM and Fiber SM
  - » 10/100, Gigabit and 10 Gigabit - Supporting Fiber SX, LX, SR and LR
  - » NIC cards with Bypass and Security
  - » PCI-Express, PCI-X, PMC and PC104 Plus
- Gigabit and 10GE Embedded Switches

## About Interface Masters Technologies, Inc.

[Interface Masters Technologies](#) is a leading vendor in the network monitoring and visibility market including Bypass, TAP, switches and smart NICs products, based in the heart of the Silicon Valley.

Interface Masters' expertise lies in Gigabit, 10GbE and 40GbE networking solutions that integrate with monitoring, inline networking, IPS, UTM, Load Balancing, WAN acceleration, and other mission-critical IT and security appliances. Flagship product lines include PacketMaster® Network Packet Broker, specialized 10GE internal server adapter cards, switches, 10Gb and 40Gb external intelligent Network TAP and Bypass and failover systems.

Company Headquarters are located in San Jose, CA with satellite offices in Hong Kong and Europe.



## Contact Interface Masters

150 East Brokaw Rd, San Jose, CA 95112  
Phone: 408-441-9341 x122  
Fax: 815-364-0888  
Email: [sales@interfacemasters.com](mailto:sales@interfacemasters.com)  
Web: [www.interfacemasters.com](http://www.interfacemasters.com)

# Interface Masters

TECHNOLOGIES

*Innovative Network Solutions*