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INTERLAKEN ALLIANCE PUBLISHES IMPLEMENTATION RECOMMENDATIONS

Industry Group Agrees on Guidelines for Interoperability between High Performance Networking Components

Silicon Valley, Calif., Nov 5, 2007 — The Interlaken Alliance, a group of companies who are collaborating on creating component interoperability recommendations, today released interoperability guidelines for components implementing Interlaken interfaces. Interlaken, an open specification for high-speed chip-to-chip packet transfers using the latest serial technology, enables component manufacturers to scale their devices to 100 Gbps. These implementation recommendations help networking equipment builders by enabling a wide range of interoperable silicon components.

The released guidelines document specifies the logical configurations to use for packet transfers at throughputs of 10Gbps, 20Gbps, 40Gbps and 100Gbps and addresses the needs of many component types including network processors, traffic managers, switch fabrics, framers and Ethernet controllers.

For more information and to download the interoperability recommendations go to www.interlakenalliance.com

“Altera is enabling the deployment of serial chip-chip interconnect technology in next generation data center and telecom infrastructure equipment by offering FPGAs and structured ASICs that leverage leading edge process technology with robust SerDes solutions,” said David Greenfield, senior director of product marketing for high-end FPGAs at Altera Corporation. “Altera is pleased to support Interlaken compliant high speed chip-chip interconnect IP and silicon solutions that support 100 Gbps bandwidth today.”

“Because of its higher bandwidth capabilities, we have designed the Interlaken interface into several of our data center products and are very pleased with the results,” said Tom Edsall, Senior Vice President and Chief Technology Officer, Data Center, Switching and Security Technology Group, Cisco. “As a co-developer of the Interlaken interface, Cisco supports its adoption by the industry as a standard interface.”

“We have seen strong industry support for Interlaken since its launch and are pleased with the depth of Interlaken eco-system,” said Fred Olsson, product line manager, Cortina Systems, leading supplier of intelligent communication solutions. “The Interlaken Alliance demonstrates how the industry is willing to work together to create compatible components that benefit all the users of Interlaken technology.”

“We see a growing opportunity for the Interlaken interconnect, bridging the gap between high performance networking components,” said Guy Koren, CTO, EZchip Technologies, provider of high-speed network processors. “EZchip will feature Interlaken in its NP-4 100-Gigabit network processor to provide customers with powerful and future-proof interoperable solutions.”

"Advanced services continue to drive high-performance networking interfaces. In anticipation of these networking requirements, Freescale expects to enable systems that incorporate Interlaken-based networking," said Jeff Timbs, marketing director for Freescale Semiconductor's Networking Systems Division. "We look forward to collaborating with Alliance members as they build awareness and interoperability for the standard."

"PMC-Sierra is pleased to support the Interlaken Alliance ecosystem," said Jonathan Loewen, PMC-Sierra’s vice president, research and development. "The definition of these key implementation recommendations is enabling seamless silicon interoperability across Interlaken-compliant interfaces."

“As a key innovator in the development of high performance multi-core and multi-threaded MIPS-based processors, RMI strives to incorporate technologies that meet and/or exceed the performance requirements of our customers,” said Mark Litvack, Director of Business Development, RMI. “Since scalability to 40Gbps and beyond is critical to the success of any future proofed network, Interlaken technology will enable a wide range of interoperable silicon components to seamlessly interconnect to our next generation XLR Processor.”

“We increasingly see Interlaken being adopted as the chip to chip interconnect of choice among most leading networking equipment vendors", said Farhad Shafai, Vice President of R&D at Sarance Technologies. "Our Interlaken IP Cores for ASICs and FPGAs offer data rates ranging from 10 to 150 Gbps, and enable our customers a low-risk and proven path for integrating this new technology into their products."

“Our customers are looking for a standards based protocol to replace SPI4.2 in their next generation networking components,” said Matt Weber, Senior Hardware Engineer at

SLE, a provider of ASIC design services and IP. “Interlaken fills that need perfectly with a solution that simultaneously provides both interoperability and scalability.”

"Xelerated has confidence in Interlaken appearing as the preferred interconnect technology for communications devices, enabling the success of our forthcoming products by virtue of its performance, scalability and flexibility. Xelerated’s roadmap includes products using 10, 20, 40 and 100Gbit/s Interlaken interfaces, enabling us to strengthen our position as the Performance Leader in Network Processing," said Thomas Eklund VP of Business Development and Marketing at Xelerated.

“Interlaken is well poised in the industry as the emerging successor to SPI4 for speeds at and above 10G, enabling a wide range of interoperable silicon components in the communications space. Leveraging the maximum interconnect performance delivered by Interlaken, communication designers benefit from the immediately available FPGA core from Sarance, hardware-proven on high performance 65-nm Xilinx Virtex-5 LXT FPGAs in production today,” said Amit Dhir, director of Infrastructure Vertical Markets at Xilinx.