PCB Assembly Guidelines for Intersil Wafer Level Chip Scale Package Devices

Introduction

There is an industry-wide trend towards using the smallest package possible for a given pin count. This is driven primarily by the handheld products market where the trend towards thinner, lighter, and low electrical parasitic packages is extremely important. The Wafer Level Chip Scale Package (WLCSP) offers the smallest footprint per pin count at a given pitch. Intersil's WLCSP allows direct connections between silicon IC and printed circuit board (PCB) through solder balls by directly connecting solder balls on the silicon die to corresponding metal pads on the PCB. Figure 1 displays a picture of an Intersil WLCSP part.

Some salient features and advantages of Intersil's WLCSP are as follows:

- Saves board real-estate by providing smallest footprint per I/O
- Ball pitch of 0.5mm or 0.4mm allows assembly with standard SMT equipment
- No underfill is required (See “Frequently Asked Questions” on page 5.)
- Completely lead-free and RoHS compliant
- MSL1 moisture sensitivity at +260°C per JEDEC J-STD-020
- Better electrical parasitics due to elimination of wires and leads
- Shipped in tape and reel per EIA 481-1

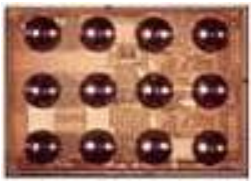

FIGURE 1. INTERSIL WLCSP

The purpose of this technical brief is to outline the basic guidelines to use the Intersil WLCSP package to ensure consistent PCB assembly necessary to achieve high yield and reliability.

Figure 2 shows a cross section of Intersil's WLCSP. Figure 3 shows Intersil WLCSP mounted on PCB.

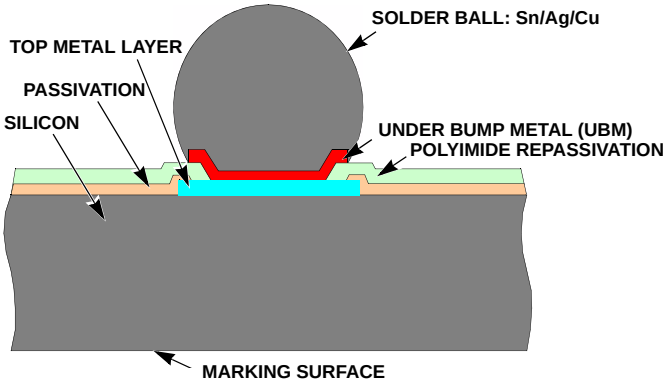

FIGURE 2. CROSS SECTION OF INTERSIL’S WLCSP (BALL ON PAD VERSION)

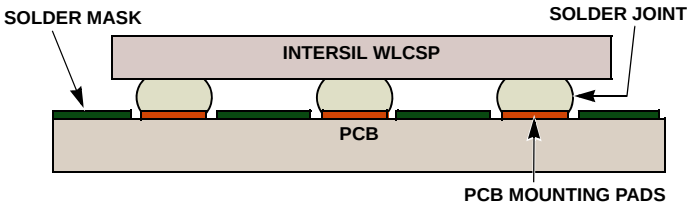

FIGURE 3. INTERSIL’S WLCSP MOUNTED ON PCB

Intersil's WLCSP Package Data

Table 1 lists Intersil's WLCSP bump count options.

TABLE 1. PACKAGE OFFERINGS

BUMP COUNT	ARRAY TYPE
4	2x2
6	2x3
8	3x3
9	3x3
10	3x4
16	4x4
20	4x5
25	5x5
30	5x6
36	6x6
42	6x7
49	7x7
56	7x8
64	8x8

TABLE 1. PACKAGE OFFERINGS (Continued)

BUMP COUNT	ARRAY TYPE
72	8x9
81	9x9
90	9x10
100	10x10
110	10x11
121	11x11

Key Considerations for WLCSP Application on PCB

- PCB mounting pads need to be controlled in terms of shapes and sizes, since they control the final dimensions of the solder joint between board and package.
- Solder paste deposit used to attach the Intersil WLCSP devices to the board which subsequently becomes part of the solder joint, must be defined and controlled.
- Solder reflow process that forms the final solder joint should comply with standard JEDEC reflow profiles and solder paste manufacturing recommendations.
- Small size of the devices and solder balls require automatic pick-and-place equipment and handling.
- Subsequent paragraphs provide more details on these items.
- WLCSP products (like other surface mount products) should not be subjected to wave solder on the PCB side that has the part mounted to it.

Printed Circuit Board (PCB) Design Parameters

Key Considerations

- Table 2 lists recommended PCB mounting pad and solder paste printing stencil parameters.
- Non-Solder Mask Defined (NSMD) or Metal Pad Defined pad construction is preferred over Solder Mask Defined (SMD) construction.
- Symmetric placement of exit traces recommended (in case of NSMD) to avoid component rotation during reflow due to surface tension of molten solder.
- Via-in-pad structures may be used for higher bump count devices when escape routing is not adequate between pads.
- For dog-bone type via connections, vias connected to the PCB mounting pads using traces should have a minimum length of 10 mils (0.254mm) for the connecting trace and should not exceed 2/3 of the pad diameter for the via diameter. (See Figure 4.)

TABLE 2. PCB MOUNTING PAD AND STENCIL PARAMETERS

DESCRIPTION	0.4mm AND 0.5mm PITCH
Mounting Pad Shape	Round
Mounting Pad Material	Copper
Pad Finish	OSP or Ni-Au (Au <0.5micron to avoid solder joint embrittlement)
Nominal PCB Pad Diameter	280µm for 0.5mm pitch and 240µm for 0.4mm pitch (+0/-25µm)
Pad thickness	<1 oz. (30µm)
Clearance between Mounting Pad and Solder Mask (in NSMD)	1 mil optimum (Figure 6) (25µm)
Stencil Fabrication	Laser cut stainless steel followed by electropolish; chemical etch method not recommended
Stencil Thickness	0.100mm to 0.125mm
Stencil Apertures	5° tapered, trapezoidal square 0.25mmx0.25mm (±0.025mm)

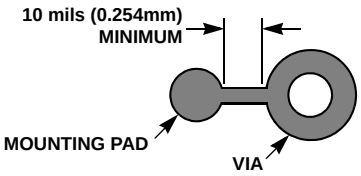

FIGURE 4. MOUNTING PAD TO VIA

Intersil WLCSP mounting pads that are directly connected to a ground plane or power plane are to be connected with a maximum of two traces of 10 mils (0.254mm) minimum length. The two traces should be at least 90° apart. (See Figure 5.)

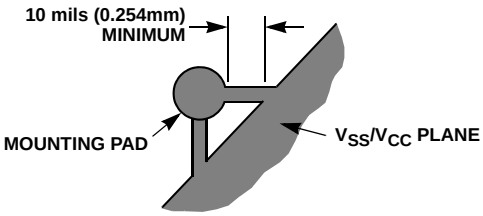

FIGURE 5. MOUNTING PAD TO V_{SS}/V_{CC} PLANE

PCB Solder Mask Opening

The PCB solder mask opening shall be larger than the PCB mounting pad (NSMD) by 1 mil (0.0254mm) per side as shown in Figure 6.

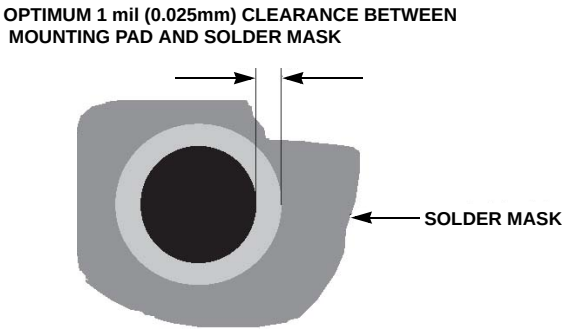

FIGURE 6. SOLDER MASK TO MOUNTING PAD CLEARANCE FOR NSMD PAD

Artwork Critical Dimension Check

During the data conversion from design software to PCB fabrication artwork the critical dimensions may be changed by rounding-off errors in the software. The critical dimensions need to be verified on the artwork before PCB manufacturing.

1. Mounting pad to mounting pad pitch
2. Mounting pad diameter
3. Solder mask opening
4. Alignment of solder mask opening with mounting pad

Intersil WLCSP Mounting Guideline

Typical Assembly Procedures

The assembly procedure for Intersil WLCSP packages is compatible with industry standard surface mount procedures, as exemplified in IPC-CM-770 and IPC-A-610 class 2 standards. Modern practice usually includes a controlled environment with a temperature of +22°C ±3°C and a relative humidity of 50% ±10%. ESD protection should be used in all process steps.

Typical Assembly Flow for Surface Mount of Intersil WLCSP

Figure 7 outlines important considerations for using Intersil WLCSP packages within the typical process flow.

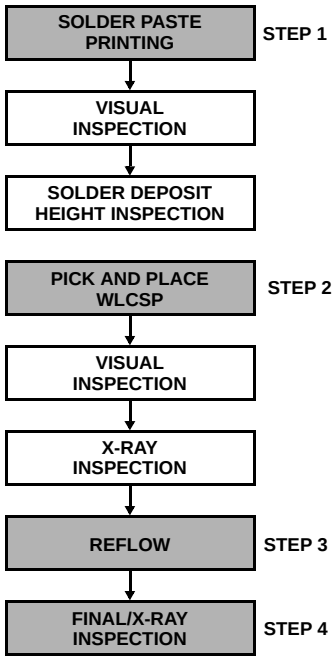

FIGURE 7. ASSEMBLY PROCESS FLOW

Step 1: Stencil for Solder Paste Printing

Solder paste printing is performed using a stencil using a standard stencil printer. The squeegee speed and pressure should be adjusted per solder paste manufacturer's recommendation. The PCB should be supported during the printing process to prevent bending of the PCB.

Use of type 3 (25 micron to 45 micron particle size range) or finer solder paste is recommended.

The solder paste height should be measured as needed to confirm stencil thickness and tolerance of ±0.5 mil (±0.012mm) per Figures 8A and 8B.

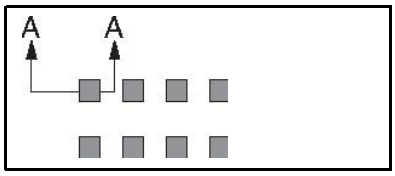

FIGURE 8A. SOLDER PASTER PATTERN - TOP VIEW

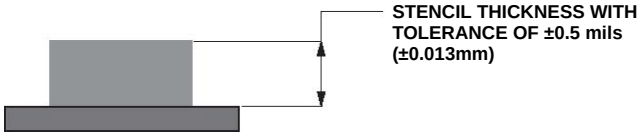

FIGURE 8B. CROSS-SECTION (AA FROM Figure 8A) OF SOLDER PASTE DEPOSIT

The PCB should be transferred to the pick-and-place machine within the time limit specified by the solder paste manufacturer after solder paste printing.

Step 2: Pick-and-Place

- Place the Intersil WLCSP on PCB according to the parts list and the assembly drawing using a pick and place machine with optical alignment.
- Verify Intersil WLCSP alignment using package orientation pin 1 marker.
- It is not recommended to use chipshooters without adequate adjustments to minimize vibrations and placer errors.
- Ensure minimal force is used for pick-and-place of the Intersil WLCSP to avoid physical damage. Z-height control method is preferred over force control.
- Maximum Z axis force on the WLCSP should be 10N.
- It is recommended that bumps be dipped into solder paste on PCB to greater than 20% of paste block height.
- Side view of Intersil WLCSP placement on PCB is shown in Figure 9.

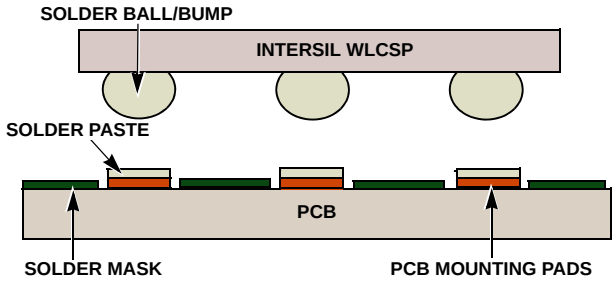

FIGURE 9. INTERSIL WLCSP PLACEMENT ON MOUNTING PAD WITH SOLDER PASTE - SIDE VIEW

Step 3: Reflow and Cleaning

Intersil WLCSP's are compatible with industry standard reflow and cleaning processes and are qualified per J-STD-020. Actual board assembly profiles should be developed based on specific process needs and board designs and should not exceed the parameters provided in the aforementioned standard.

Step 4: Final/X-Ray Inspection

Verify assembly quality using available inspection techniques such as transmission X-ray inspection. The side view of the final configuration is shown in Figure 10. There should be no shorts, no solder bridging between solder bumps and no loose solder balls under or around the WLCSP device.

NOTE: Intersil WLCSP parts do not require underfill, and are qualified without the use of it. Use of underfill in application, if desired by the end-user, should involve careful selection of the material so as to avoid problems caused by a mismatched material choice.

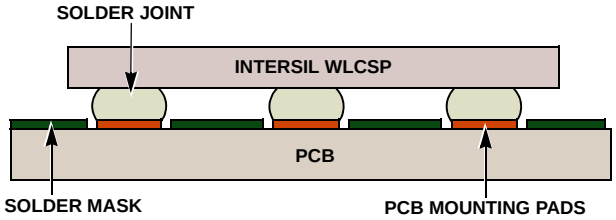

FIGURE 10. INTERSIL WLCSP MOUNTED TO A PCB BOARD

Board-Level Reliability Data

Intersil WLCSP tests and passing criteria are shown in Table 3.

TABLE 3. BOARD LEVEL RELIABILITY DATA FOR INTERSIL'S WLCSP

RELIABILITY TEST	RESULT
HAST	Passed +130°C/85% RH for 96 hrs
TC	Passed 500 cycles of -40°C to +125°C
THB	Passed +85°C/85% RH for 1000 hrs
HTOL	Passed 1000 hrs at +125°C
HTS	Passed 1000 hrs at +150°C

Thermal Characteristics

Intersil WLCSP thermal impedance data is listed in Table 4.

TABLE 4. THERMAL IMPEDANCE DATA IN NATURAL CONVECTION (STILL AIR) PER JESD 51-7 AND JESD 51-9

BUMP COUNT	DIE SIZE X (mm)	DIE SIZE Y (mm)	PITCH (mm)	JEDEC PCB TYPE	T_{JA} (°C/W)	Psi-JB (°C/W)
8	3	3	0.5	2S2P + vias	74.2	33.4
16	1.65	1.65	0.4	2S2P + vias	59.6	-
36	5	5	0.5	2S2P + vias	39.9	15.2

Rework

Rework procedures are identical to BGA.

Rework profile should duplicate original reflow profile used in assembly.

Rework system should include localized convection heating, bottom side heating and a pick-and-place device. System should also provide thermal profile capability.

Frequently Asked Questions

Question: Does WLCSP package require use of underfill upon board mount?
Answer: No. Intersil WLCSP packages are qualified to be used without any underfill. However, customers may use it based on their preference while taking precaution to ensure properties of the underfill, for example Tg and CTE, do not negatively impact reliability of the WLCSP.

Question: Will the WLCSP package get damaged during board mount?
Answer: WLCSP is basically silicon die with solder bumps which can be damaged if mishandled or subjected to excessive mechanical force. Board mounting performed per Intersil's SMT guideline will ensure such issues do not occur. Manually removing and reattaching a WLCSP will pose very high risk of damaging the package

Question: Is there a marking or traceability information on the WLCSP package?
Answer: Yes. The unbumped side of the package is laser marked with pin 1 identification, product code and manufacturing batch traceability information.

Question: Does the WLCSP package have backside coating?
Answer: Backside coating is offered selectively for certain products or package size. Contact intersil.com/support for more details.