Thermal Characterization of Packaged Semiconductor Devices

Abstract

With the continuing industry trends towards smaller, faster and higher power devices, thermal management is becoming increasingly important. After all, higher device performance can come at a price (higher temperatures and lower reliability) if thermal considerations aren't carefully weighed.

Not only are devices trending smaller but the boards they mount onto are also shrinking. Placing the units closer and closer together on smaller boards helps lower overall system size and cost and improves electrical performance. These benefits are important; but from a thermal standpoint, raising power while reducing size is a bad combination. It's this increase in “power density” that's been driving the heightened industry focus on thermal management.

To assist board and system level designers in this effort, Intersil provides standardized thermal resistance data, most commonly Theta-$_{JA}$, on our product datasheets. This tech brief should assist in understanding and using these thermal resistances or “theta's”. It also discusses several thermal characterization parameters called “psi's” that are coming into more widespread use.

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The Concept of Thermal Resistance

A common method of characterizing a packaged device's thermal performance is with “thermal resistance”, denoted by the Greek letter “theta” or θ. For a semiconductor device, thermal resistance indicates the steady state temperature rise of the die junction above a given reference for each watt of power (heat) dissipated at the die surface. Its units are °C/W.

The most common examples are Theta-$_{JA}$ (junction-to-ambient), Theta-$_{JC}$ (junction-to-case), and Theta-$_{JB}$ (junction-to-board). Knowing the reference, (i.e., ambient, case, or board) temperature, the power, and the relevant theta value, the junction temperature can be calculated. Theta-$_{JA}$ is commonly used with natural and forced convection air-cooled systems using components mounted on epoxy-glass PCBs. Theta-$_{JC}$ is useful when the package has a high conductivity case mounted directly to a PCB or heatsink. And theta-$_{JB}$ applies when the board temperature adjacent to the package is known.

In addition to these theta thermal resistances, the psi-$_{JB}$ (junction-to-board) and psi-$_{JT}$ (junction-to-top) thermal characterization parameters can be useful. For a device powered up on an application board, these psi's provide a correlation between junction temperature and the board temperature or “top of package” temperature.

The term “psi” is used to distinguish these from “theta” thermal resistances since not all heat is actually flowing between the points of temperature measurement with the psi's. They're not true thermal resistances for this reason.

Common Terminology

- T_J = Die junction temperature, °C
- T_C = Package case temperature, °C
- T_B = Board temperature adjacent to package, °C
- T_T = Top of package temperature at center, °C
- T_A = Ambient air temperature, °C
- θ_{JA} (Theta-$_{JA}$) = Thermal resistance junction-to-ambient, °C/W
- θ_{JC} (Theta-$_{JC}$) = Thermal resistance junction-to-case, °C/W
- θ_{JB} (Theta-$_{JB}$) = Thermal resistance junction-to-board, °C/W
- Ψ_{JB} (Psi-$_{JB}$) = Junction-to-board characterization parameter, °C/W
- Ψ_{JT} (Psi-$_{JT}$) = Junction-to-top (of package) characterization parameter, °C/W
- P = Power dissipated by device, Watts

Thermal Test Standardization

The main purpose of standard datasheet thermal ratings is to compare the relative performance of packaged devices against each other. These comparisons are more accurate and meaningful when the tests are performed using standardized procedures.

Intersil generally follows the following industry standards:

- JEDEC EIA/JESD 51-X Series Standards

They're available at www.jedec.org under the “Standards and Documents” area. These define thermal test board designs as well as general thermal test procedures. This tech brief will summarize key details.

The 3 Basic Thermal Test Board Types

Because of the influence of the Printed Circuit Board (PCB) on results, tight control of the test board design is needed. This helps ensure that differences in published thermal ratings from various suppliers are due to the component or package design, and not test board variability.

When directly comparing theta-$_{JA}$'s for different products, be sure to compare data for the same board type. The 3 basic board types have different heat spreading capability and will result in different theta-$_{JA}$ values, even for the exact same device. On each product datasheet, Intersil generally provides thermal data based on the board type(s) that are likely to be used in the application.

The 3 basic test board types are:

1. **“Low Effective” Thermal Conductivity Board (1S0P)**

- Top surface traces only.
- Called 1S or 1S0P for “1 Signal, 0 Plane” layers.
- Similar to previous “SEMI” 1S0P boards.
- Applicable JEDEC board specs:
  - JESD51-3: Most surface mount packages.
  - JESD51-9: Area array (e.g., BGA, WLCSP).
  - JESD51-10: Through-hole perimeter leaded (e.g., DIP, SIP).
  - JESD51-11: Through-hole area array (e.g., PGA).

2. **“High Effective” Thermal Conductivity Board (1S2P)**

- Top surface traces + 2 buried planes.
- Called 1S2P for “1 Signal, 2 Plane” layers.
- Also called 2S2P because of a 2nd nonrelevant bottom edge signal trace layer for wiring.
- Adding 2 planes lowers theta-$_{JA}$ roughly 20-40+% vs 1S0P (reduction varies widely by package size and style).
- Applicable JEDEC board specs:
  - JESD51-7: Most surface mount packages.
  - JESD51-9: Area array (e.g., BGA, WLCSP).
  - JESD51-10: Through-hole perimeter leaded (e.g., DIP, SIP).
  - JESD51-11: Through-hole area array (e.g., PGA).

3. **“High Effective” Thermal Conductivity Board with “Direct Attach” Features (1S2P+Vias)**

- Top surface traces + 2 buried planes + thermal vias.
- Called 1S2P+Vias or 1S2P-DA board type.

- Applies to WLCSPs with GND/thermal balls and to plastic packages with exposed metal pads (e-pads), thermal balls, etc.
- Applies to ceramic/metal packages when the base (whether ceramic or metal finish) is adhered to the PCB (no air gap).
- Thermal vias are added into the PCB below the package to connect to the upper buried plane.
- Adding vias lowers theta-$_{JA}$ vs 1S2P type (percentage varies but generally significant).
- Applicable JEDEC board specs:
  - JESD51-5 add-on to JESD51-7: Most surface mount packages.
  - JESD51-9: Area array (e.g., BGA, WLCSP).

Industry Standards for Thermal Test Boards

JEDEC uses a number of standards to define the test board designs that apply to the various package styles:

- **JESD51-3:** "Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages"
- **JESD51-7:** "High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages"
- **JESD51-5:** "Extension of Thermal Test Board Standards for Packages with Direct Thermal Attachment Mechanisms"
- **JESD51-9:** "Test Boards for Area Array Surface Mount Package Thermal Measurements"
- **JESD51-10:** "Test Boards for Through-hole Perimeter Leaded Package Thermal Measurements"
- **JESD51-11: "**Test Boards for Through-hole Area Array Leaded Package Thermal Measurements"

Studying these standards isn't necessary to simply compare datasheet theta-$_{JA}$'s for different devices. But understanding more of the test board design details should help a system level designer estimate the device thermal performance on their actual application board.

This is accomplished by comparing such details as board size, metal coverage, buried planes, thermal vias, etc. This can help determine whether a device will be hotter or cooler on the application board vs the standard test board. Note that these test boards contain only 1 self-heated unit, so theta-$_{JA}$'s based on them don't include mutual heating from any other devices.

The typical features listed below apply to most test boards. A more extensive summary by each JEDEC test board standard is found in "Appendix A" on page 11.

Typical Test Board Features

- Board Material: FR-4 epoxy-glass
- Finished copper metal layer thickness
  - Surface traces: 2 ounce ±20%
  - Buried planes: 1 ounce +0/-20%
- Board thickness: ~1.6mm (63mils)
- Board and buried plane size for most leaded and leadless surface mount packages

PACKAGE LENGTH (L)	BOARD SIZE	PLANE SIZE (IF PRESENT)
L ≤27mm	3 x 4.5"	2.92 x 2.92"
27 < L ≤48mm	4 x 4.5"	3.92 x 3.92"

- Board and buried planes size for BGA, WLCSP, DIP, SIP and PGA packages.

PACKAGE LENGTH (L)	BOARD SIZE	PLANE SIZE (IF PRESENT)
L ≤ 40mm	4 x 4.5"	3.92 x 3.92"
40 < L ≤ 65mm	5 x 5.5"	4.92 x 4.92"
65 < L ≤ 90mm	6 x 6.5"	5.92 x 5.92"

- See "Appendix A" on page 11 for extensive summary.
- See JEDEC specs for all details.
- Figures 1 and 2 show a typical test board from Top and Side Views.

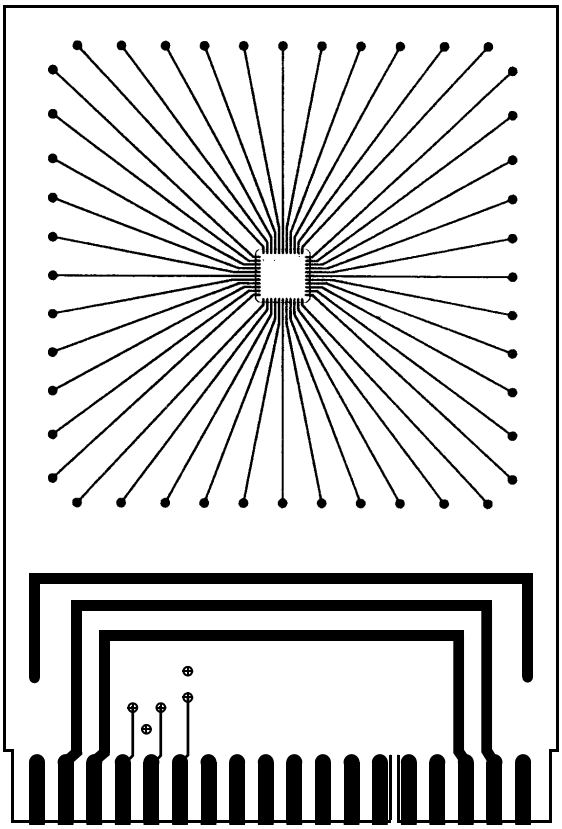

FIGURE 1. TOP VIEW - TYPICAL TEST BOARD

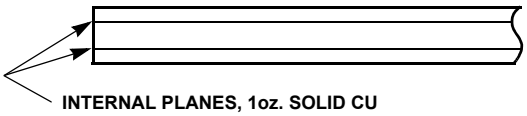

FIGURE 2. SIDE VIEW (~5X) - HIGH EFFECTIVE CONDUCTIVITY (1S2P) TEST BOARD

Industry Standards for Thermal Test Procedures

Intersil calculates Theta and Psi values using temperature and power data from a lab test or equivalent computer simulation. Testing procedures generally follow the JEDEC EIA/JESD 51-X series. The applicable standards grouped by type are:

General Methodology

- **JESD51:** "Methodology for the Thermal Measurement of Component Packages (Single Semiconductor Device)"
- **JESD51-1:** "Integrated Circuits Thermal Measurement Method-electrical Test Method (Single Semiconductor Device)"
- **JESD51-13: "**Glossary of Thermal Measurement Terms and Conditions"
- **JEP140:** "Beaded Thermocouple Temperature Measurement of Semiconductor Packages"

Natural Convection

(Applies to Theta-$_{JA}$, psi-$_{JT}$, psi-$_{JB}$)

- **JESD51-2A:** "Integrated Circuits Thermal Test Method Environmental Conditions - Natural Convection (Still Air)"

These "still air" tests are run in a 1 cubic foot box to prevent stray air currents. The JEDEC compliant board is mounted horizontally, with the device on the top side.

Forced Convection

(Applies to Theta-$_{JA}$, psi-$_{JT}$, psi-$_{JB}$)

- **JESD51-6:** Integrated Circuits Thermal Test Method Environmental Conditions - Forced Convection (Moving Air)

Airflow tests are run in a wind tunnel with a single device mounted on a JEDEC compliant board. The board is mounted vertically and parallel to the airflow, which cools both sides of the board. Common airflow speeds are 100 to 600 Linear Feet per Minute (LFM). For reference, a commonly used speed of 200 LFM equals about 1 meter/second or 2.3 miles/hour, equivalent to a light breeze.

Junction-to-case

(Applies to Theta-$_{JC}$)

- **SEMI G30-88: "**Junction-to-case Thermal Resistance Measurements of Ceramic Packages"
- **Mil-Std 883 Method 1012.1:** Thermal Characteristics

The objective of the theta-$_{JC}$ test is to force almost all of the heat flow through either the package top or bottom surface (i.e., the "case"). This is achieved by mounting that surface onto a temperature-controlled heatsink.

Junction-to-board

(Applies to Theta-$_{JB}$)

- **JESD51-8:** "Integrated Circuits Thermal Test Method Environmental Conditions - Junction-to-board"

Defines a ring style cold plate used with a standard 1S2P or 1S2P+Vias test board. The cold plate is clamped onto both sides of the board at least 5mm from the package. Almost all heat is forced to flow from the package into the plane of the board so that accurate "junction-to-board" thermal resistance can be measured.

General Test Procedures

Lab Testing of Standard Packages on JEDEC Standard Boards

This type of data is based on results from an industry-standard Thermal Analyzer designed for this purpose.

T_J is determined using the semiconductor junction characteristic of a declining forward voltage drop with increasing temperature. Before each test, a sample unit is calibrated over the necessary temperature range while immersed in a heated mineral oil bath. The resulting calibration curve is used along with voltage readings to continuously monitor T_J during the test.

Other temperatures (i.e., T_A, T_B, T_T, T_C) are monitored using small thermocouples. Once the device has reached steady-state equilibrium, temperatures applicable to the test are recorded. The analyzer controls device power dissipation (P), which is used along with the temperature data to calculate the theta and/or psi values. Generally 3 or more units are tested and the results averaged.

Lab Testing of Unique Packages Such as Modules on Product Evaluation Boards

Lab equipment specific to the product type involved may be used to take relevant device temperature and/or power data. Device internal (T_J) temperature data may be monitored through built-in device sensing methods, or embedded small thermocouples. In addition to the above, other temperatures are generally monitored using small thermocouples. Once the device has reached steady-state equilibrium, the device power dissipation (P) and temperatures applicable to the test are recorded and thermal metrics are calculated from the data.

Product datasheet Theta-$_{JA}$ or related metrics based on such work make reference to the product evaluation board used for thermal testing, rather than to a JEDEC standard thermal test board.

Finite Element Analysis (FEA) or Computational Fluid Dynamics (CFD) Modeling

For a computer simulation, a detailed 3D-Solid model is constructed of the packaged device mounted as appropriate for the test involved. Intersil uses industry standard advanced thermal modeling software for these simulations.

With power applied to the die surface, the model is solved. The results provide full temperature contours across the package and board or heatsink. Temperatures at specific locations are extracted and used in relevant theta or psi calculations, just as if they had been obtained from lab testing.

The 5 Main Thermal Metrics

TABLE 1. QUICK SUMMARY

THERMAL METRIC	SYMBOL	DEFINITION FORMULA	GENERAL USAGE FORMULA	TYPE	MAIN PURPOSE
Theta-$_{JA}$	θ_{JA}	$\theta_{JA} = (T_J - T_A) / P$	$T_J = T_A + (\theta_{JA} * P)$	Thermal Resistance	Used to rank package performance.
Theta-$_{JC}$	θ_{JC}	$\theta_{JC} = (T_J - T_C) / P$	$T_J = T_C + (\theta_{JC} * P)$	Thermal Resistance	Used to rank package performance.
Theta-$_{JB}$	θ_{JB}	$\theta_{JB} = (T_J - T_B) / P$	$T_J = T_B + (\theta_{JB} * P)$	Thermal Resistance	Used to rank package performance and estimate T_J of devices on application PCBs.
Psi-$_{JB}$	Ψ_{JB}	$\Psi_{JB} = (T_J - T_B) / P$	$T_J = T_B + (\Psi_{JB} * P)$	Characterization Parameter	Used to estimate T_J of devices on application PCBs.
Psi-$_{JT}$	Ψ_{JT}	$\Psi_{JT} = (T_J - T_T) / P$	$T_J = T_T + (\Psi_{JT} * P)$	Characterization Parameter	Used to estimate T_J of devices on application PCBs.

Theta-$_{JA}$

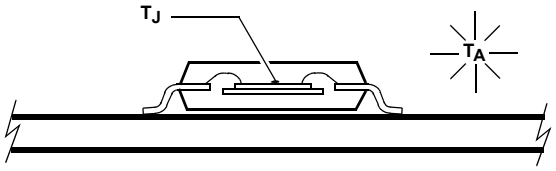

FIGURE 3. THETA-$_{JA}$ MEASUREMENT POINTS

DEFINITION: $\Theta_{JA} = (T_J - T_A) / P$

Where:

θ_{JA} = Thermal resistance junction-to-ambient, °C/W

T_J = Die junction temperature, °C

T_A = Ambient air temperature, °C

P = Power dissipated by device, watts

Example: To determine theta-$_{JA}$, the lab test or model data needed is T_J, T_A, and P. If T_J = 80°C, T_A = 25°C, and P = 1.0W, then:

θ_{JA} = (80°C - 25°C) / 1.0W = 55°C/W.

USAGE FORMULA:

With θ_{JA}, T_A and P known, then:

$T_J = T_A + (\theta_{JA} * P)$

Example: If theta-$_{JA}$ = 55°C/W and the application board has similar construction as the thermal test board, then a 1st order approximation of T_J in the system can be made. Assuming T_A = +35°C in the system, and steady state power of the device is P = 0.6W, then:

T_J = 35°C + (55°C/W * 0.6W) = 68°C

KEY POINTS FOR Θ_{JA}:

- Indicates ease of heat flow through the total of all paths between die junction and ambient air.
- Datasheet θ_{JA}'s are intended mainly for performance comparison of one packaged device against another.
- Lower values indicate better performance.
- Since θ_{JA} is highly dependent on board design, standardized test boards are used.
- Datasheet θ_{JA}'s should be used only for 1st order approximation of performance (i.e., T_J rise above T_A) in an application-specific environment.

APPLYING DATASHEET Θ_{JA} TO APPLICATION PCBs

It's safe to assume that a device that performs better in a standardized test will also perform better in an actual system of similar design. This helps in making component or package design choices, but when extending a vendor's standardized datasheet values to the end application, it's important to keep in mind that they're based on specific test conditions. It falls to the board/system designer to understand how the thermal test environment/board compare to the system under design. The various sections of this tech brief help by describing key details of thermal test boards and procedures.

It should not be assumed that a datasheet theta-$_{JA}$ value (for a single device on an standard test board) would predict the temperature rise of the device on a final application board. Performance will be affected by variations in board surface metal coverage, number of buried planes, heat-spreading area around each component, other surrounding “hot” devices, etc. The main differences between test and application boards should be understood before using datasheet theta$_{JA}$'s to estimate T_J of devices on application boards.

Theta-$_{JC}$

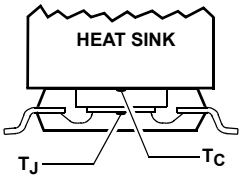

FIGURE 4A. CONDUCTIVE PACKAGE TOP (HEAT SINK ON TOP)-

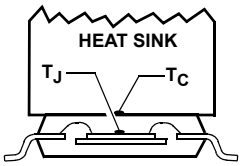

FIGURE 4B. NON-ENHANCED PACKAGE TOP (HEAT SINK ON TOP)

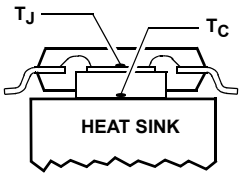

FIGURE 4C. CONDUCTIVE PACKAGE BOTTOM (HEAT SINK OR ENHANCED PCB ON BOTTOM)

FIGURE 4. THETA-$_{JC}$ MEASUREMENT POINTS FOR 3 MOUNTING EXAMPLES

DEFINITION: $\Theta_{JC} = (T_J - T_C / P$

Where:

θ_{JC} = Thermal resistance junction-to-case, °C/W

T_J = Die junction temperature, °C

T_C = Package case temperature, °C

P = Power dissipated by device, watts

USAGE FORMULA:

With θ_{JC}, T_C and P known, then:

$T_J = T_C + (\theta_{JC} * P)$

KEY POINTS FOR Θ_{JC}:

- Indicates ease of heat flow between die junction and either package top or bottom.
- Measured with package top or bottom surface mounted to a heatsink. If not obvious, the surface used should be reported.
- Datasheet θ_{JC} values are intended for:
  - Performance comparison of one packaged device against another (lower values indicate better performance).
  - Calculation of T_J rise above T_C.
  - Calculating a larger overall thermal resistance of which θ_{JC} as a part.
- Generally relevant to:
  - Plastic packages with top or bottom mounted to an external heatsink.
  - Plastic packages with bottom e-pad soldered to a thermally enhanced PCB.
  - Ceramic and metal cased packages with a surface mounted to an external heatsink or thermally enhanced PCB.
- Dependent mainly on thickness, area, and conductivity of device materials in the θ_{JC} heat flow path.

OTHER APPLICABLE FORMULA'S:

For packages with a surface adhered or soldered to an epoxy-glass PCB, the total θ_{JA} is:

$\theta_{JA} = \theta_{JC} + \theta_{CA}$

Note the θ_{CA} term is the case-to-ambient resistance, which is controlled by the PCB design.

For packages with a surface adhered or soldered to a heatsink, the total θ_{JA} through this path is:

$\theta_{JA} = \theta_{JC} + \theta_{CS} + \theta_{SA}$

Note the θ_{CS} (case-to-sink) term is controlled by the thermal grease or mounting pad between the package and heatsink. The θ_{SA} (sink-to-ambient) term is obtained from the heatsink manufacturer's datasheet.

Theta-$_{JB}$

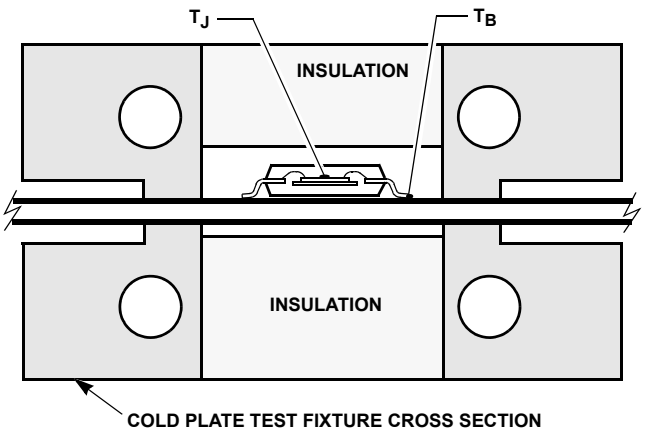

FIGURE 5. THETA-$_{JB}$ MEASUREMENT POINTS

DEFINITION: $\Theta_{JB} = (T_J - T_B / P$

Where:

θ_{JB} = Thermal resistance junction-to-board, °C/W

T_J = Die junction temperature, °C

T_B = Board temperature adjacent to package, °C

P = Power dissipated by device, watts

USAGE FORMULA

With θ_{JB}, T_B and P known, then:

$T_J = T_B + (\theta_{JB} * P)$

KEY POINTS FOR Θ_{JB}:

- Datasheet θ_{JB} values are intended for:
  - Performance comparison of one packaged device against another.
  - Calculation of T_J rise above Tb for devices on application PCBs.
  - Calculating a larger overall thermal resistance of which θ_{JB} is a part.
- Uses ring style cold plate to drive vast majority of heat into test board.
- Since θ_{JB} is dependent on test board design, it's standardized on the style with 2 buried planes (1S2P or 1S2P+vias as applicable).
- Similar to Ψ_{JB}, but θ_{JB} will have a larger value (see Ψ_{JB} notes below).

ANOTHER APPLICABLE FORMULA:

With the package mounted on an epoxy-glass PCB, the total thermal resistance is:

$\theta_{JA} = \theta_{JB} + \theta_{BA}$

Note the θ_{BA} term is the board-to-ambient resistance, which is controlled by the PCB design.

Psi-$_{JB}$

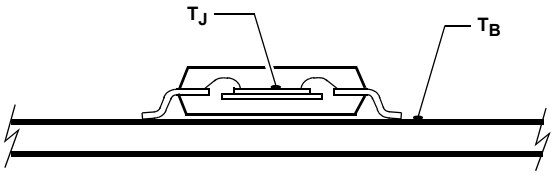

FIGURE 6. PSI-$_{JB}$ MEASUREMENT POINTS

DEFINITION: $\Psi_{JB} = (T_J - T_B) / P$

Where:

Ψ_{JB} (Psi-$_{JB}$) = Junction-to-board characterization parameter, °C/W

T_J = Die junction temperature, °C

T_B = Board temperature adjacent to package, °C

P = Power dissipated by device, watts

USAGE

Knowing Ψ_{JB}, to obtain T_J of a device powered-up on an application PCB:

1) Measure the board temperature near the edge of the package, on a copper trace at the center of one side.

2) Determine the power dissipated by the device.

3) Calculate: $T_J = T_B + (\Psi_{JB} * P)$

KEY POINTS FOR Ψ_{JB}

- A characterization parameter, not a “true” thermal resistance.
- Intended for calculation of T_J rise above T_B for devices on application PCB's.
- Optional test in JESD51-6 θ_{JA} standard.
- Generally measured using 1S2P or 1S2P+vias board.
- Measured using setup same as for a theta-$_{JA}$ test.
- Similar to θ_{JB}, but Ψ_{JB} will have a slightly smaller value.

Ψ_{JB} VS Θ_{JB}

The Greek letter “psi” is used to distinguish Ψ_{JB} from θ_{JB} since not all heat is actually flowing between the points of temperature measurement (i.e., junction and board) like with θ_{JB}. This is because the setup of the Ψ_{JB} test does not force all heat flow into the board like the θ_{JB} ring style cold plate. Ψ_{JB} is not a “true” thermal resistance for this reason.

With Ψ_{JB} testing a certain amount of device heat can dissipate from the package top and sides; therefore ΨJB will always have a smaller value than θ_{JB}. It turns out however, that for most common small to medium sized packages, the two values will be similar - generally within 15%. Thus, Ψ_{JB} is sometimes reported in lieu of θ_{JB}.

BOARD TEMPERATURE MEASUREMENT

When measuring T_B in an application, care should be taken to prevent accidental cooling of the thermocouple bead. We recommend use of a small ~40 gauge (3.15mil diameter) thermocouple soldered to the board trace. Cover the bead with a thermally conductive epoxy and route the wires along the board surface. This is important towards preventing "too cool" T_B measurements, which would lead to the calculated T_J also being too cool.

IR spot tools are not recommended for the T_B measurement. Even those with smaller spot (measurement area) diameters still typically have a ~100mil+ spot. This is much larger than the copper trace to be measured. If the IR tool emissivity is factory-fixed, it's generally ~0.95 which is accurate for epoxy-glass surfaces alone. But bare copper or copper covered with thin solder mask can have much lower emissivity. These issues make accurate measurement of the copper trace temperature difficult using IR spot tools.

Psi-$_{JT}$

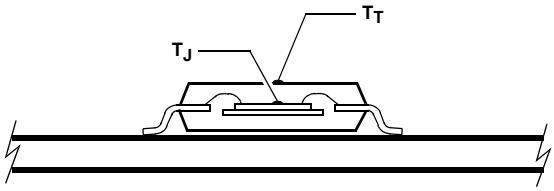

FIGURE 7. PSI-$_{JT}$ MEASUREMENT POINTS

DEFINITION: $\Psi_{JT} = (T_J - T_T) / P$

Where:

Ψ_{JT} (Psi-$_{JT}$) = Junction-to-top (of package) characterization parameter, °C/W

T_J = Die junction temperature, °C

T_T = Top of package temperature at center, °C

P = Power dissipated by device, watts

USAGE

Knowing Ψ_{JT}, to obtain T_J of a device powered-up on the application PCB:

1) Measure the top-of-package temperature at the center.

2) Determine the power dissipated by the device.

3) Calculate: $T_J = T_T + (\Psi_{JT} * P)$

KEY POINTS FOR Ψ_{JT}

- A characterization parameter, not a "true" thermal resistance.
- Intended for calculation of T_J rise above T_T for devices on application PCBs.
- Optional test in JESD51-2A and JESD51-6 θ_{JA} standards.
- For plastic packages, depends mainly on thickness and thermal conductivity of plastic mold compound above die, and die size (Ψ_{JT} increases as die size decreases-mainly affects smaller devices).
- Rises with increasing airflow, the speed of which is reported with Ψ_{JT} if not measured under natural convection.

Ψ_{JT} vs Θ_{JC}

It's worth noting that Ψ_{JT} is not the same as θ_{JC}, which only applies when the package surface is mounted onto a heatsink. The test methods and resulting values are quite different. In fact, if Ψ_{JT} and θ_{JC} (at the top surface) are measured on the same package, Ψ_{JT} will generally be much smaller than θ_{JC}. The Greek letter "psi" is used to help clearly distinguish Ψ_{JT} from the θ_{JC} thermal resistance.

TYPICAL PLASTIC PACKAGE Ψ_{JT} VALUES

Under natural convection, Ψ_{JT} for a plastic package is generally a relatively low value. This means that T_J is usually just a little hotter than the top of the package, T_T. The die is physically separated from the top surface by only a thin region of plastic mold compound. So unless the top is forcibly cooled by significant airflow there will be very little delta-T between them.

The natural convection Ψ_{JT} value is often less than 1 °C/W for thin packages. For packages that are progressively thicker and/or have smaller body, die, or die paddle size, the value increases into the roughly 2 - 10+ °C/W range. These relatively low values suggest that knowing Ψ_{JT} accurately is often not essential. T_T measurements are often so low that using any reasonable Ψ_{JT} value in the temperature rise calculations results in T_J estimates within temperature limits.

TOP OF PACKAGE TEMPERATURE MEASUREMENT

When measuring T_T in an application, care should be taken to prevent accidental cooling of the package surface during the act of measuring it. This is especially important with a plastic package due to the low thermal conductivity of the surface.

We recommend use of a small ~40 gauge (3.15mil diameter) thermocouple. The bead and thermocouple wires should touch the top of the package and be covered with a minimal amount of thermally conductive epoxy. The wires should be routed closely along the package and board surfaces to help prevent cooling of the bead due to heat loss into the leads. This is important towards preventing "too cool" T_T measurements, which would lead to the calculated T_J also being too cool.

An IR spot method should be utilized only when using a tool with a small enough spot area to acquire the true top center "hot spot". Note the emissivity of plastic mold compound is ~0.95, which fortunately matches the common factory-fixed value found in some IR tools.

Many so-called "small spot size" tools still have a measurement area of ~100+ mils at "zero" distance of the tool from the surface. This spot area is too big for many smaller packages and likely would result in cooler readings than the small thermocouple method. The accuracy depends on the IR spot size in relation to the size of the device being measured.

For a thin package with a die size larger than ~125 mils square for example, the temperature will be relatively uniform across a ~100 mil IR spot. A reasonably accurate top center reading

should be obtained. But for packages that are thicker or have smaller die sizes, the temperature distribution within the IR spot area may be very nonuniform. Cooler temperature bands surrounding the true hot spot will be averaged into the readout. In such cases, it's prudent to add at least a few degrees to the IR readout to better estimate the true top center temperature. If in doubt about the IR spot size or measurement accuracy, revert to the small thermocouple method.

Additional PCB Design Considerations

Spread the Heat Around... and Down

To help understand the influence of the PCB on thermal performance, it's interesting to compare the “effective” thermal conductivity (“k”) for the composite PCB after adding buried copper planes. These “effective” values are based on the parallel resistance formula for the “x” and “y” direction, and series formula for “z”. The calculations use the thickness and conductivity of the FR-4 and the copper planes.

TABLE 2. COPPER PLANE EFFECTS

NUMBER OF BURIED 1oz Cu PLANES	PCB EFFECTIVE THERMAL CONDUCTIVITY, W/m-K	
	x AND y	z
NONE (FR-4 ONLY)	0.87	0.310
ONE PLANE (1P)	9.4	0.317
TWO PLANES (2P)	18	0.324

The in-plane (x and y) value rises from 0.87 W/m-K for “FR-4 only” all the way up to 18 W/m-K with 2 planes. This ~2000% increase in the effective in-plane “k” value generally results in a ~20-40+% reduction in datasheet Theta-$_{JA}$ values.

Even as the in-plane “k” is increased 20x, the through-plane (z) value is nearly unchanged. Realizing this negligible z-direction effect is important when designing with a package with a bottom exposed metal pad.

For these e-pad packages, there’s another PCB design option that takes better advantage of the high conductivity path through the bottom. This involves dropping thermal vias down beneath the e-pad to one or more of the buried planes to help overcome FR-4’s poor thermal conductivity.

The closer thermal coupling of the device to the buried planes results in more efficient heat spreading and more uniform temperature distribution across the PCB. The larger effective cooling area around the device also allows its heat to be more efficiently dissipated off the board surfaces by convection and radiation. The overall cooling effect can be significant, especially in newer smaller exposed-pad packages where not much heat spreading can occur in the package itself.

Think “Thermal”, not “Electrical”

Thermal and electrical systems have analogies that many engineers draw upon, but there’s an important difference that might make you want to think about thermal a little differently.

The ratio of high versus low conductivity items in the thermal world is typically on the order of hundred’s-to-one, while in the electrical world it’s trillion’s-to-one or more. Because of this, an engineer’s thermal “gut feel” may not be quite right when it’s based mainly on electrical engineering experiences.

Heat doesn’t tend to flow down metal traces from points “A” to “B” with little loss like electrical current. Rather, the heat flows much more easily into surrounding materials or the air. All this “leakage” of heat is generally nothing to complain about since we’re usually trying to increase it even more, but it does add a good bit of complexity to the task of predicting how much heat is flowing where.

To nail down the required accuracy, simulation tools such as 3D FEA (Finite Element Analysis) and CFD (Computational Fluid Dynamics) are used by the industry to help take all the variables into account.

Appendix A

JESD51-X

Thermal Test Board Design Summary (See JEDEC Specs for Full Details)

JESD51-3

Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages

- Covers 1S0P boards.
- For leaded and leadless surface mount packages.
- Not for through-hole or BGA or WLCSP.
- Top surface copper traces only:
  - Fanout: to at least 25mm from package.
  - Width: 0.254mm (10 mils) ±10%
  - Thickness: 2oz (0.070mm ±20%), typically 1oz clad + 1oz plated.
- Board thickness: 1.57mm (62 mils).
- Board size:

PACKAGE LENGTH (L)	BOARD SIZE
Less than 27mm	3 x 4.5"
27 to 48mm	4 x 4.5"

JESD51-7

High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages

- Covers 1S2P boards.
- For leaded and leadless surface mount packages.
- Not for through-hole or BGA or WLCSP.
- Top surface trace layout: same as for 51-3.
- Adds 2 buried planes for “high effective” *x*-*y* conductivity.
  - 1oz thick (0.035mm +0/-20%) each.
- Z-direction conductivity of PCB still poor.
- Board thickness: 1.60mm (63 mils).
- Board and buried planes sizes:

PACKAGE LENGTH (L)	BOARD SIZE	PLANE SIZE
L ≤ 27mm	3 x 4.5"	2.92 x 2.92"
27 < L ≤48mm	4 x 4.5"	3.92 x 3.92"

JESD51-5

Extension of Thermal Test Board Standards for Packages with Direct Thermal Attachment Mechanisms

- Covers “1S2P+Vias” boards.
- For plastic leaded and leadless surface mount packages with an exposed metal pad on the package underside.
- For Ceramic/Metal packages when the base, whether ceramic or metal finish, is adhered or soldered to the PCB (no air gap).
- Not for through-hole or BGA or WLCSP.
- Defines PCB attach pad (thermal land) geometry to match package’s mounting surface.
- Defines thermal vias (added to 1S2P) to make 1S2P+Vias board.
  - 1.2 x 1.2mm array under attach pad.
  - 0.3mm diameter.
  - 0.025mm min Cu in via barrel.
  - Vias contact upper buried plane only.

JESD51-9

Test Boards for Area Array Surface Mount Package Thermal Measurements

- Covers all 3 board types:
  - 1S0P, 1S2P, 1S2P+vias
- For area array packages (e.g., BGA, WLCSP) only.
- Top surface traces:
  - Fanout at least 25mm from package.
  - Trace thickness and width:

BALL PITCH	TRACE Tkn	TRACE WIDTH
>0.5mm	70µm (2oz) ± 20%	36 to 44% of ball pitch
0.5mm or Less	50µm (1.5oz) ± 20%	45 to 55% of ball pitch

- 2 Buried Planes (1S2P and 1S2P+Vias only):
  - 1 oz thick (0.035mm +0/-20%) each
- Board thickness: 1.60mm (63 mils).
- Board and buried planes sizes:

PACKAGE LENGTH (L)	BOARD SIZE	PLANE SIZE (ONLY 1S2P AND 1S2P + Vias)
L ≤ 40mm	4 x 4.5"	3.92 x 3.92"
40 < L ≤ 65mm	5 x 5.5"	4.92 x 4.92"
65 < L ≤ 90mm	6 x 6.5”	5.92 x 5.92”

- Thermal vias (1S2P + Vias board only):
  - Only for packages with thermal balls.
  - Via diameter: Varies by ball pitch.
  - 0.018mm min Cu in via barrel.
  - Vias contact upper buried plane only.

JESD51-10

Test Boards for Through-hole Perimeter Leaded Package Thermal Measurements

- Covers 1S0P and 1S2P board types.
- For through-hole perimeter leaded packages (e.g., DIP, SIP) only.
- Top surface copper traces:
  - Fanout: to at least 25mm from package.
  - Width: 0.25mm ±10%
  - Thickness: 2oz (0.070mm ±20%), typically 1oz clad + 1oz plated.
- 2 Buried planes (for 1S2P board only):
  - 1oz thick (0.035mm +0/-20%) each
  - Isolation gaps in both buried planes for pin through-holes.
  - Thermal pins directly attached to die pad are to be connected to top buried plane.
- Board thickness: 1.60mm (63 mils).
- Board and buried planes sizes:

PACKAGE LENGTH (L)	BOARD SIZE	PLANE SIZE (ONLY 1S2P AND 1S2P + Vias)
L ≤ 40mm	4 x 4.5"	3.92 x 3.92"
40 < L ≤ 65mm	5 x 5.5"	4.92 x 4.92"
65 < L ≤ 90mm	6 x 6.5”	5.92 x 5.92”

JESD51-11

Test Boards for Through-hole Area Array Leaded Package Thermal Measurements

- Covers 1S0P and 1S2P board types.
- For through-hole area array leaded packages (e.g., PGA) only.
- Top surface copper traces:
  - Fanout: to at least 25mm from package.
  - Width: 36 to 44% of pin pitch.
  - Thickness: 2oz (0.070mm ±20%), typically 1oz clad + 1oz plated.
- 2 Buried planes (for 1S2P board only):
  - 1oz thick (0.035mm +0/-20%) each.
  - Isolation gaps in both buried planes for pin through-holes.
- Board Thickness: 1.60mm (63 mils).
- Board and buried planes sizes:

PACKAGE LENGTH (L)	BOARD SIZE	PLANE SIZE (1S2P ONLY)
L ≤ 40mm	4 x 4.5"	3.92 x 3.92"
40 < L ≤ 65mm	5 x 5.5"	4.92 x 4.92"
65 < L ≤ 90mm	6 x 6.5”	5.92 x 5.92”