QML

QUALITY MANAGEMENT

PLAN

SECTION 1.0 INTRODUCTION

1.1 SCOPE

This document is the Intersil "Quality Management (QM) Plan" which is required for the QML program as defined in MIL-PRF-38535. The contents describe the operating systems and procedures used by Intersil Corporation to meet all the requirements of the QML program. Intersil Corporation has manufacturing operations in Palm Bay, Florida

Intersil Corporation is a fully certified manufacturer for Product Assurance Levels Q, V, and T.

Class T

1. Class “T” is designed for specific applications. Intersil does not claim Class T is the same as Class Q.
2. Intersil Reliability information is available on the Intersil web site. http://rel.intersil.com
3. Intersil Class T RAD Hard application devices are fully tested and guaranteed to the total dose specified in the SMD drawing.
4. CLASS T TECHNOLOGIES

DIE TECHNOLOGY
HFSTDB
AVLSI-R
RH-SIGATE
P6

1.2 AUTHORIZATION AND MAINTENANCE

The QML Plan will be maintained under configuration control. The specification may be reviewed or distributed to external customers. QML documents manually distributed externally will not be placed under change control. External customers may access the current revision of the manual via the Intersil web site http://www.intersil.com/en/support/qualandreliability.html Revisions can be initiated by Intersil employees with approval by the Intersil Technical Review Board (TRB).

The Intersil QML Coordinator is responsible for insuring that the QM Plan is implemented and maintained to current MIL-PRF-38535 requirements.

1.3 RAD HARD PRODUCT DEVELOPMENT AND INTRODUCTION

Product design for radiation specific applications is active at this time. Product introductions of radiation hardened product will be based on characterization and formal release through DLA.
As Intersil introduces newly developed radiation hardened products, all necessary actions will be taken to certify the design tools, devices models and fabrication processes. Appendix C of MIL-PRF-38535 will be used as a guideline for further certification.

1.4 CONTENT

The QM Plan is documented in 4 sections and 2 appendixes

1. Introduction
2. QML General (Non Technology Specific)
3. QML Technology Specific
4. Quality Systems Reference
6. Appendix A RAD Hard Assurance
7. Appendix B Ship Ahead of Qualification

The format used for this plan is based on the QM plan outline in MIL-PRF-38535.

Reference is made throughout the plan to the Quality Manual for the Palm Bay operations.

Sections 2 & 4 are written general in nature. Reference is made in each of these sections to Intersil internal specifications which provide details for the operations.

TABLE OF CONTENTS

INTERSIL QUALITY MANAGEMENT PLAN

SECTION 2.X QML GENERAL (NON-TECHNOLOGY SPECIFIC)

GENERAL

Section 2.X of this manual is written to describe the general (non-technology specific) systems/requirements of the Intersil QM Plan. These systems/requirements establish the "Quality System" which is used for all product types, regardless of technology type.

SECTION 2.1 INDEX OF CERTIFIED BASELINE DOCUMENTS

GENERAL

The Intersil documentation system includes an index of specifications used in the QML program.

CONTENTS OF INDEX

The Document Control index of specifications includes; specification number, specification title and the latest revision of the specifications.

INDEX AVAILABILITY

A listing of all specification series critical to the QML program is available on-line in Intersil's document control system (Intrepid).

The indexes containing specifications used to make-up the QML program will be available at the time of validation and thus will be considered the certified baseline. The complete database for the QML program resides on Intersil's electronic systems.

SECTION 2.2. CONVERSION OF CUSTOMER REQUIREMENTS

GENERAL

Conversion of customer requirements to Intersil processes specifications utilizes the contract review system and order entry procedures. These procedures are used by Marketing and the Customer Engineering department to review the Customer Control Drawings (SCD), Statement of Work (SOW) and Purchase Orders (P.O.) and translate the customer's requirements into Intersil internal processing procedures. These review systems are supported by Design Engineering, Product Engineering, Manufacturing Operations, Quality Assurance, Finance and Legal/Contracts, as applicable.

PROCEDURES

1. INITIAL DOCUMENT REVIEW -
   The primary sources of customer requirements are the SCD, SOW, and P.O.. The Marketing Manager (MM) will initiate a Drawing Review Request (DRR) for a customer SCD or SOW. The DRR will be sent to the Customer Engineer. The SCD and SOW is compared to standard flows and, where necessary, exceptions are noted. These exceptions are negotiated between the MM/or Sale Representative and customer until acceptance is mutually achieved. Confirmations of customer acceptance to the modification are included in the permanent record file.
2. PO REVIEW AND ORDER ENTRY -
   The customer generated P.O. is entered into a P.O. database. For standard flow product, the PO is sent to order entry. For custom flow product, the PO is reviewed by Customer Engineering, Engineering and Manufacturing. All discrepancies are resolved and the PO is prepared for order entry.

3. CONTRACT REVIEW
   The contract review system ensures:
   a. The contract has been reviewed
   b. There is a method to verify that all requirements are met.
   c. There are provisions for processing contract changes
   d. There is a method to prepare internal specifications which reflect customer requirements.

QUALITY SUPPORT DOCUMENTS

240114	Customer Documentation Review and Specification Generation
999053	Intrepid System
999032	Ship Ahead of Qual Instructions and Non-Std Product Option Descriptions (R/S Specs)
999003	Contract Review Procedures for Marketing and Sales
999017	Part Number and Structure Definitions

SECTION 2.2.1 DEVICE SPECIFICATION REQUIREMENTS

GENERAL

Device specifications are written for all products to reflect the requirements of MIL-PRF-38535. These device specifications are either controlled by Defense Logistics Agency Land and Maritime (DLA) or are part of the Intersil internal document control program.

DEVICE SPECIFICATION REQUIREMENTS

Both the specifications controlled by DLA and those controlled internally by Intersil contain the following information.

a. Scope
b. Applicable Documents
c. Requirements
d. Quality Assurance Provisions
e. Packaging
f. Special Requirements

Intersil works with DLA to format information to comply with DLA SMD standard formatting requirements.

QUALITY SUPPORT DOCUMENTS

54XXXX	B Specifications
55XXXX	K Specifications
87XXXX	R Specifications

SECTION 2.2.2 CONTROLLED DESIGN PROCEDURES AND TOOLS

GENERAL

The Intersil Chip Design methodology draws on proven and integrated tools that permit a designer to migrate a design concept from an objective specification or functional description to functional circuits. The Intersil Cadence Design System provides a basis for the design tools. The tools support simulation, performance analysis, physical layout, layout verification, and testability.

CONTROLLED DESIGN PROCEDURES AND TOOLS

The New Product Development Process (NPDP) program is designed to optimize the PTM (Product to Market) cycle times and improve the success rate of new product developments. The formalized NPDP procedure series provides guidelines and a methodology for product development, product planning, product definition, and market introduction. The NPDP procedure includes formal reviews at strategic points within the development cycle to ensure consistency in all areas of circuit development. Appropriate documentation is retained as Quality records. The Intersil Design System is a world class design system which contains tool sets for Analog, Mixed Signal, Power, RF Communication, and Digital designs. Intersil Design System uses the defined core set of tools for front-end design, layout, and physical design verification. In addition to the core design tools, the Intersil Design Systems are tightly integrated with high performance Intersil tools and populated with advanced Intersil processes/libraries.

QUALITY SUPPORT DOCUMENTS

54XXXX	B Specifications
87XXXX	R Specifications
55XXXX	K Specifications
NPDP-XXXX	New Product Development Procedures

SECTION 2.2.3 PHOTOMASK SUBCONTRACTED

GENERAL

Photomasks are used in the Wafer Fab forming operations to transfer the patterns of the various levels of the IC design onto a photoresist coated wafer. All photomasks will be purchased through an approved subcontractor.

QUALITY SUPPORT DOCUMENTS

All Mask Fabrication procedures are documented in specification controlled by the supplier. All mask are ordered in conformance with requirements specified in purchase specification 210825-XXXX.

SECTION 2.2.4 WAFER FABRICATION AND ASSEMBLY CAPABILITIES BASELINE

GENERAL

Records and information related to wafer fabrication and assembly capabilities covered by the Intersil QML program are in the Intrepid System.

SYSTEM

Each device type assigned to the QML program will be so designated in Intrepid. Attached to each of these device types are the die and package technology used. Wafer process and package capabilities are listed below.

WAFER FAB CAPABILITIES

Reference section 3.3 for a list of QML Process Technologies.

ASSEMBLY CAPABILITIES

HERMETIC

PACKAGE TYPES	LEAD FINISHES	DIE ATTACH MATERIAL
CERDIP SIDE BRAZE DIP METAL CANS FLATPACKS CERQUADS LCC PGA To-257 SMD .5	SOLDER (SnPb) (63/37% TIN/LEAD) GOLD (>99.7%)	SILVER GLASS 67-73% Ag EUTECTIC GOLD (>99.7%) SILVER POLYMER (79.5-80.5 Ag) SILVER EPOXY (79% Ag) SOLDER (95% Pb/5% Sn)

SECTION 2.2.5 WAFER FABRICATION, ASSEMBLY & TEST FLOWS

GENERAL

Each product fabricated at Intersil is produced in accordance with a series of "traveler/flow" specifications. The traveler/flow describes the sequence of processes and references the appropriate unit process specification which describes how each process is to be executed. "Traveler/flows" are written for material fabrication, wafer fabrication, assembly, test, and post test processing. Wafer process and wafer level testing are defined in Section 2.2.9 Screening.

MASK, WAFER FABRICATION, ASSEMBLY & TEST FLOWS

All operations on the process flows used to fabricate, assemble, test, and monitor product will have appropriate work instructions. These work instructions will include, where appropriate, samples, drawings, and detailed operational instructions to ensure quality levels are maintained.

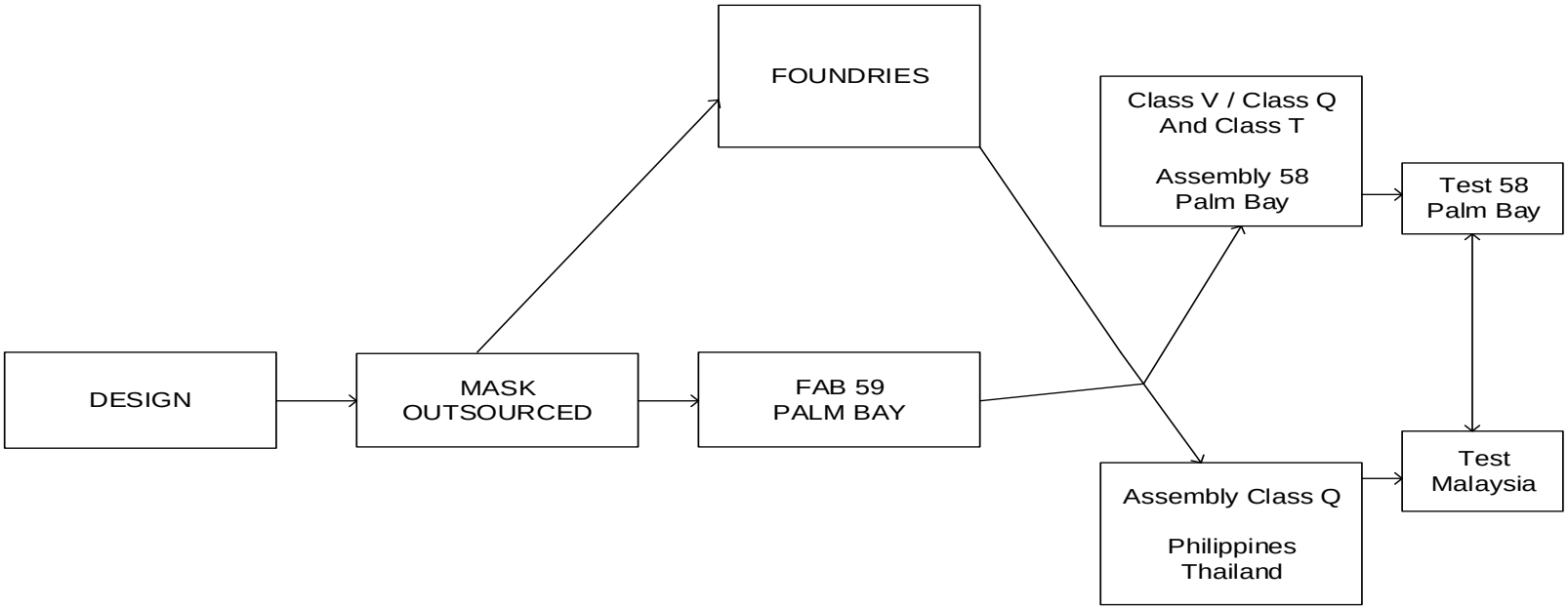
Through specified procedures, all designated support personnel, team members, and management are responsible for, and have the authority to, update work instructions to insure process and test procedures conform to expected practices and optimum quality systems. All applicable personnel are jointly responsible for ensuring the current work instructions are available.

Software control is the responsibility of the department who manages, administers, and/or uses the software. Procedures used to govern critical software are documented in internal process specifications.

QUALITY SUPPORT DOCUMENTS

All QML Product with corresponding flows/travelers are controlled by the electronic database "Intrepid".
Generic flows for Design, Wafer Fabrication, Assembly, and Test are as follows:

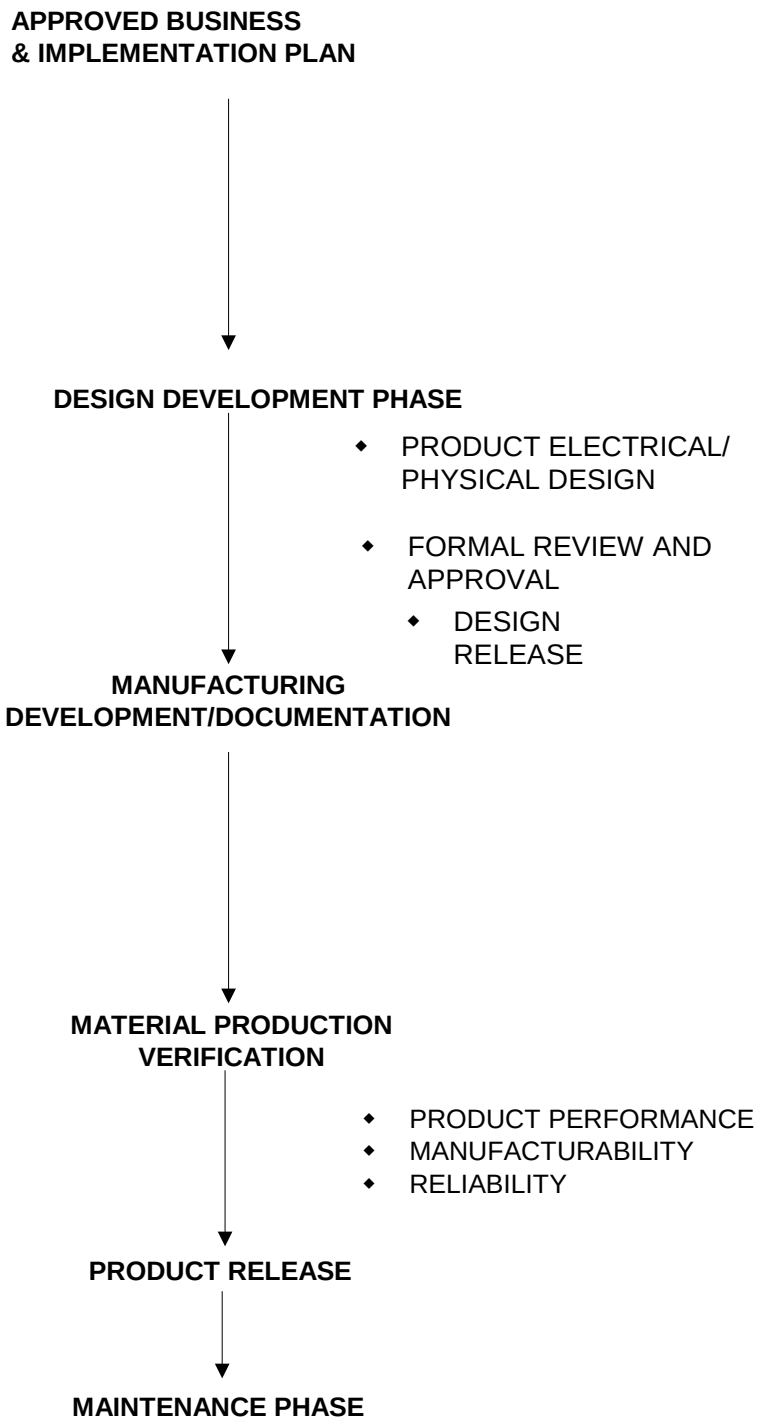
PRODUCT FLOW

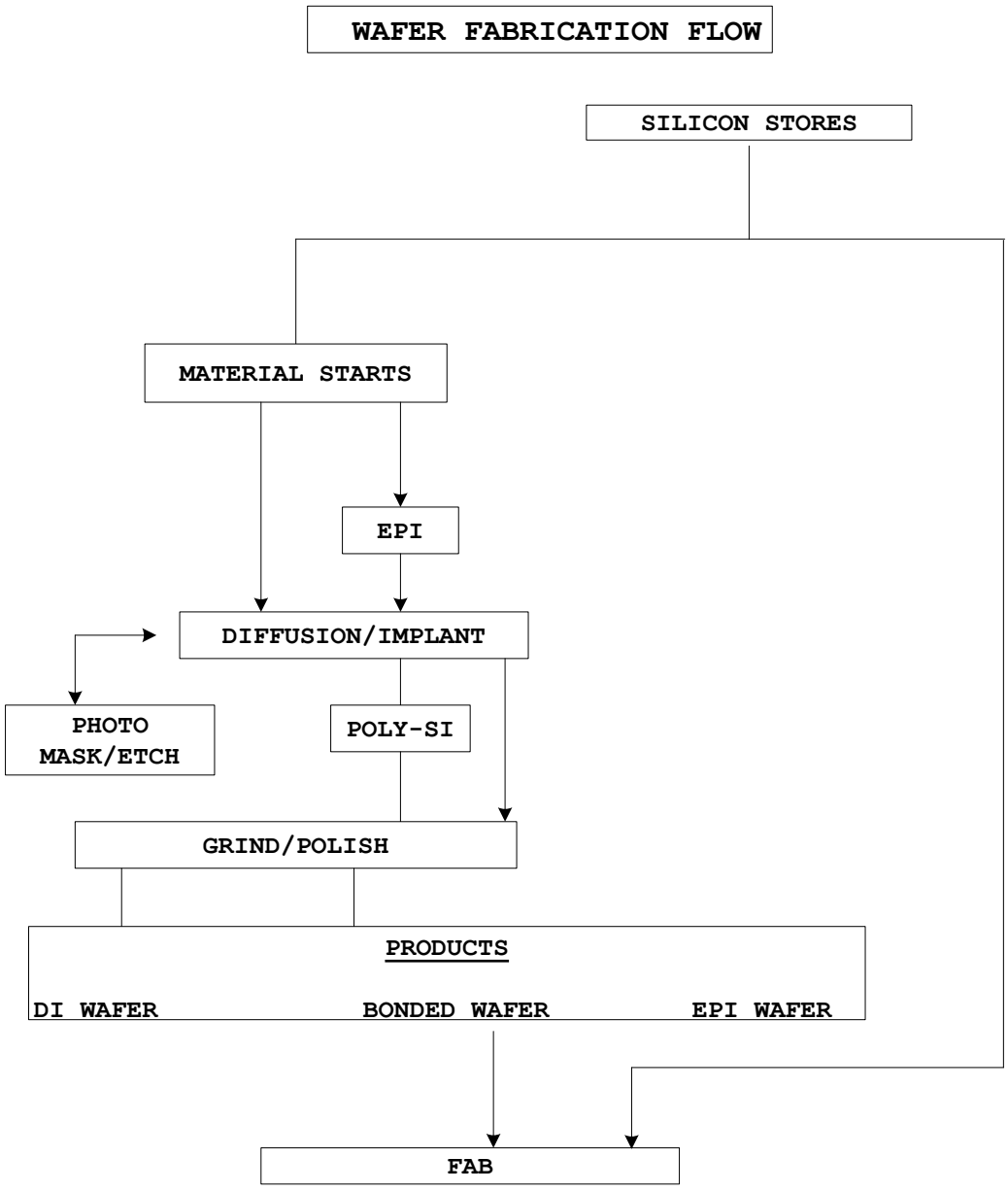


Subcontractors

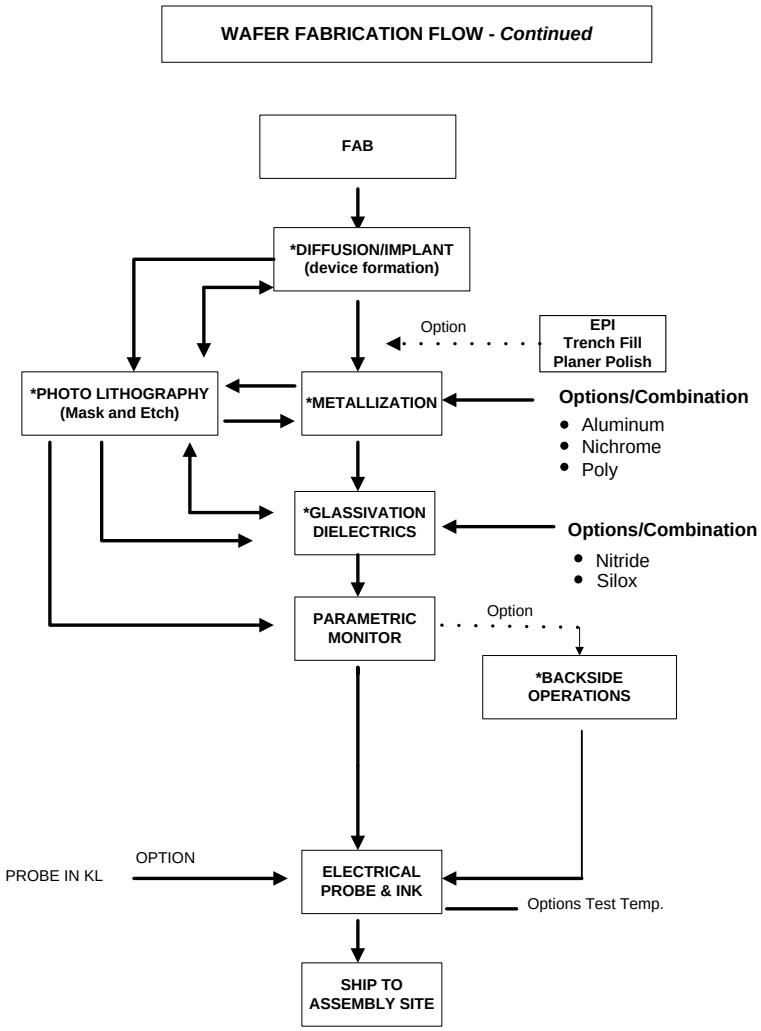
- UMC is an Intersil approved subcontractor for Mask Generation and Wafer Fab Operations.
- Global (IBM) is an Intersil approved subcontractor for Mask Generation and Wafer Fab Operations.
- TowerJazz is an Intersil approved subcontractor for Mask Generation and Wafer Fab Operations.
- Amkor Philippines is Intersil approved for subcontractor services for Class Q assembly.
- Millennium Microchip Technology (MMT) is Intersil approved for subcontractor services for Class Q assembly.
- Carsem Malaysia is Intersil approved for subcontractor services for Class Q test operation.
- Bridgepoint (Criteria Labs), Texas wafer level 100% testing (probe) Class Q and V.

BASIC DESIGN FLOW





CONTINUED



Technologies/Products are defined by a specific flow (traveler). A unit process contained in the flow is evaluated by specific measurements such as:

* Diffusion/Implant	* Deposited Films	* Photo Resist	* Grind/Polish
- Junction Depth	-Film Thickness	- Critical Dimension	- Thickness
- Sheet Resistivity	- Refractive Index	- Resist Thickness	
- Oxide Thickness	- Film Composition	- Etch Rates	
- Implant Dose Calibration	- Resistivity		

NOTE: Changes to process evaluations are approved per 999004.

WAFER SAW AND DIE SORT CLASS Q,V, AND T

Optional and if required are controled via specific flows/travelers defined by the current best practice

RECEIVE DIE/WAFERS AND PAPERWORK

↓

DIE/WAFER STORES

↓

ATTACH WAFER SAW/DIE INSPECT TRAVELER

↓

DIE SEPARATION (Saw)

↓

DIE PEEL

- 100% SAW through ON TAPE- SILICON, SOS

↓

DIE SORT/CLEAN

- MANUAL/AUTO, DIE PICK
- RAD HARD SAMPLES PCKED AS REQUIRED
- (TOTAL DOSE RADIATION TESTING LEVEL IS AS SPECIFIED IN THE SMD DRAWING)
- SEM SAMPLES AS REQUIRED

↓

DIE INSPECTION (HIGH POWER)

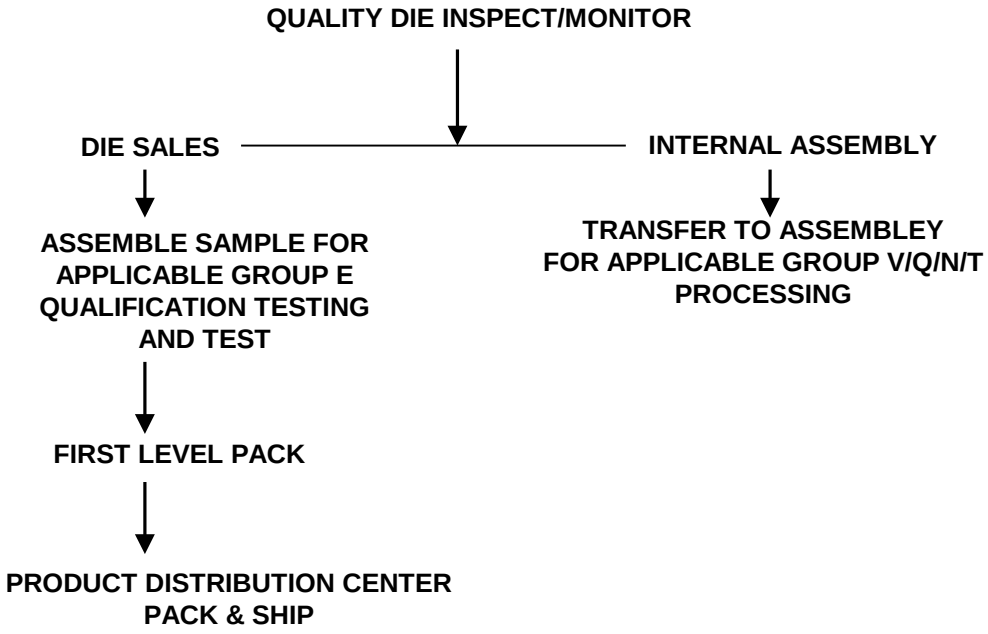
- CLASS V CONDITION "A"
- CLASS Q CONDITION 'B'
- CLASS Q CONDITION 'B' ALTERNATE
- SOS STANDARD PRODUCT MODIFIED COND. A
- SOS STANDARD PRODUCT MODIFIED B COND . B
- CLASS T MODIFIED CONDITION B
- DETAILS OF CLASS T VISUAL INSPECTION ARE IN 233750 AND ARE AVAILABLE IN INTREPID

↓

QUALITY DIE INSPECT/ MONITOR

WAFER SAW AND DIE SORT CLASS Q,V, AND T continued

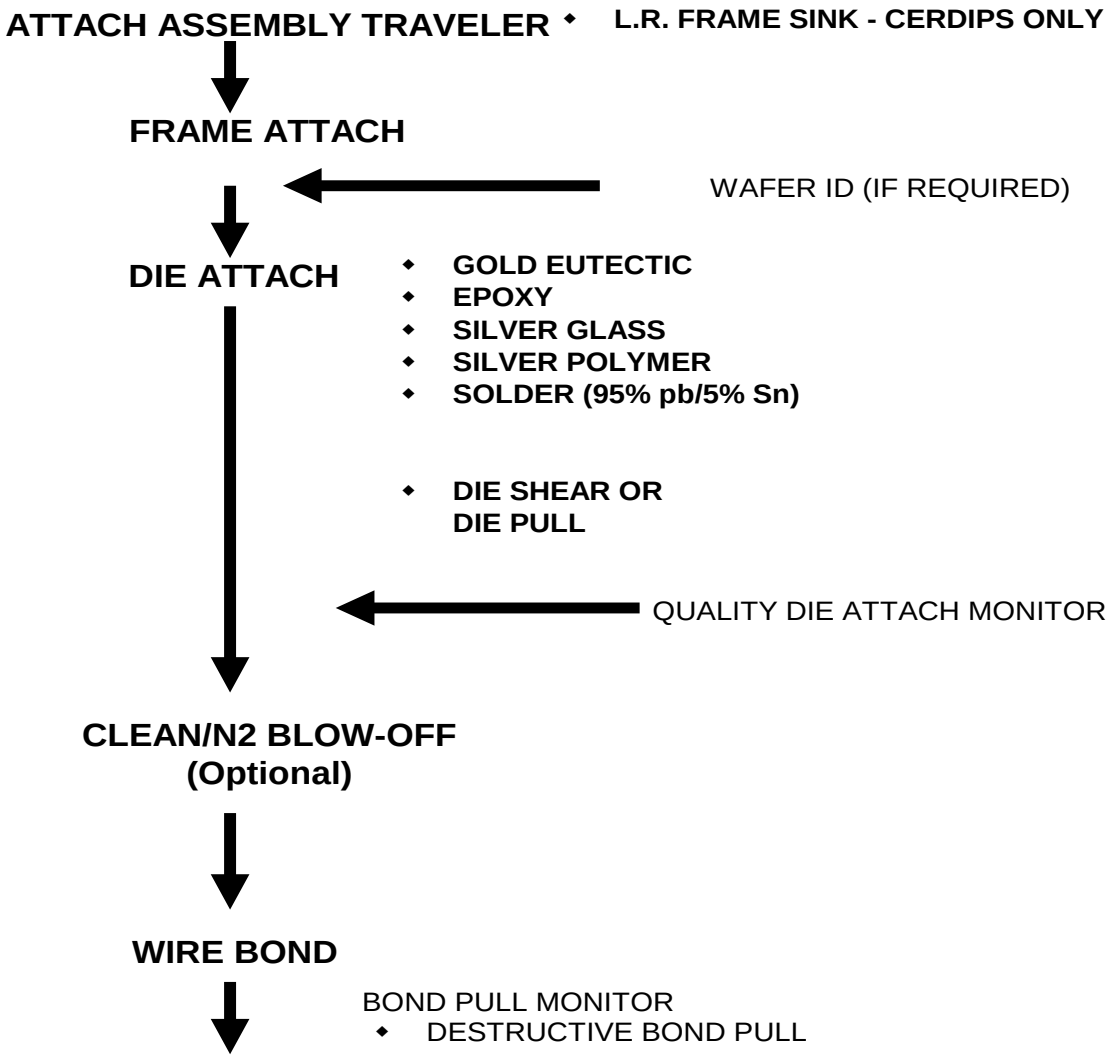
Optional and if required are controled via specific flows/travelers defined by the current best practice



ASSEMBLY FLOW HERMETIC
Class Q and V

Options and if applicable are controled via specific flows/travelers defined by the current best practice

* Mil-STD-750 Test methods are used for all RAD Hard Power IC Product processed from die attach through seal operations & centrifuge. The process is a Mil-PRF.19500 DSCC certifed process for Power Products.



ASSEMBLY FLOW HERMETIC
Class Q and V
CONTINUED

NON-DESTRUCT BOND PULL
(IF REQUIRED)

- 100% WIRES PULLED - CLASS "V" OR WHEN SPECIFIED
- NOT APPLICABLE FOR CLASS "V" RAD HARD POWER IC

↓

HYDROGEN FIRE
(SOLDER SEAL ONLY)

↓

CLEAN/N2 BLOW-OFF
(OPTIONAL)

↓

PRESEAL INSPECTION
(HIGH AND LOW POWER)

- CLASS "V"/COND "A"
- CLASS "Q"/COND "B"
- CLASS "Q" ALTERNATE
- SOS STD. PRODUCT MODIFIED "A
- SOS STD. PRODUCT MODIFIED "B"
- CLASS "V" RAD HARD POWER IC Mil-STD-750

↓

QUALITY PRESEAL MONITOR
(HIGH AND LOW POWER)

- PER APPLICABLE VISUAL INSPECTION CLASS

CONTINUED -

ASSEMBLY FLOW HERMETIC CLASS Q AND V (CONTINUED)

SEAL

- FURNACE GLASS SEAL - CERDIPS
- FURNACE SOLDER SEAL - GOLD/TIN COMBO LIDS
- RESISTANCE WELD - NICKEL LIDS METAL CANS
- SEAM WELD - NICKEL/GOLD LIDS

↓

TEMPERATURE CYCLE

↓

CENTRIFUGE

↓

PIND TEST (IF REQUIRED)

- ALL CLASS "V" OR CUSTOMER REQUIREMENTS

↓

Sequence of events below may vary

↓

FINE LEAK TEST

↓

GROSS LEAK

↓

FRAME REMOVAL (IF REQUIRED)

- MANUAL TRIMMING

↓

TUBE AND CARIER LOAD

- VISUAL INSPECTION -SAMPLE

↓

QUALITY MONITOR (OPTIONAL)

- EXTERNAL VISUAL SAMPLE AND DATA REVIEW

↓

SHIP TO TEST

CONTINUED

ASSEMBLY FLOW HERMETIC CLASS Q AND V (CONTINUED)

(RETURNED TO ASSEMBLY FROM TEST)

LEAD FINISH (IF REQUIRED)

- SOLDER * CERDIPS, SIDEBRAZE DIPS, METAL CANS, LCC
- GOLD- SIDEBRAZE DIPS, FLATPACKS, LCC, PGA, METAL CANS
- MAY BE PERFORMED AFTER BURN-IN AND ELECTRICAL TEST

↓

QUALITY MONITOR (OPTIONAL)

- EXTERNAL VISUAL AND DATA REVIEW

↓

RESHIP TO TEST

ASSEMBLY FLOW HERMETIC CLASS T

Optional and if applicable are controlled via specific flows/travelers defined by current best practice. Monitors are to the same criteria as manufacturing operations
Class T RAD Hard Power IC products will follow the Class S/Q Flow for the die attach through package seal operations

ATTACH ASSEMBLY TRAVELER

↓

DIE ATTACH

- GOLD EUTECTIC
- SILVER POLYMER
- SILVER GLASS

↓

← **QUALITY DIE ATTACH MONITOR**

- DIE SHEAR
  OR
- DIE PULL

↓

CLEAN/N2 BLOW-OFF (OPTIONAL)

↓

WIRE BOND

BOND PULL MONITOR

- DESTRUCTIVE BOND PULL

↓

CONTINUED

ASSEMBLY FLOW HERMETIC CLASS T *(CONTINUED)*

CLEAN/N2 BLOW-OFF (OPTIONAL)

↓

PRESEAL INSPECTION (HIGH AND LOW POWER)

↓

- CLASS T VISUAL PER 233750 (MODIFIED CONDITION B OF TEST METHOD 2010)
- NOTE: INSPECTION DETAILS WILL BE MADE AVAILABLE UPON REQUEST

QUALITY PRESEAL MONITOR (HIGH AND LOW POWER)

↓

SOLDER SEAL

↓

- FURNACE SOLDER SEAL GOLD/TIN COMBO LID

ASSEMBLY HERMETIC FLOW CLASS T (CONTINUED)

NOTE: Sequence of events below may vary

FINE LEAK SAMPLE TEST

↓

FRAME REMOVAL (IF REQUIRED)

↓

- MANUAL TRIMMING

TUBE/CARRIER LOAD

↓

QUALITY MONITOR (OPTIONAL)

↓

SHIP TO TEST

TEST OPERATIONS FLOW
CLASS Q and V

- OPTIONS. "If Applicable" are controlled via specific flows/travelers defined by special customer requirements or current best commercial practices.

LOT FORM

↓

100% ELECTRIC TEST (OPTIONAL)
see Notes 1 and 2

↓

BURN-IN (IF APPLICABLE)

- BURN-IN CONDITIONS eg STATIC OR DYNAMIC, ARE DEFINED IN THE APPLICABLE DETAIL DRAWING, AND INCLUDED IN THE PART SPECIFIC FLOW
  See Note 3

↓

- POST BURN-IN ELECTRICAL (See Notes 1 and 2)
- APPLY APPLICABLE PDA
- OPTIONAL ELECTRICAL TEST MONITOR/ ALTERNATE GROUP "A" AS DEFINED BY PRODUCT SPECIFIC TRAVELER

↓

SOLDER DIP (IF APPLICABLE)

- VISUAL
- SOLDERABILITY MONITOR

TEST OPERATIONS FLOW
CLASS Q and V
CONTINUED

BRAND

- FLOW DEPENDENT - BRAND MAY
- BE COMPLETED PRIOR TO BURN-IN.

↓

FINAL ELECTRICAL TEST PER APPLICABLE DEVICE SPECIFICATION

- SEE NOTE 1 AND 2
- ELECTRIC TEST MONITOR
- (ALTERNATE GROUP "A" if applicable)

↓

QUALITY (TCI) TESTING (AS APPLICABLE)

- HERMETIC - APPLICABLE GROUPS B, C, D, AND E TESTING
- REFERENCE Section 2.10 /2.2.10

- PLASTICS --MATRIX MONITOR,
- REFERENCE Section 2.10 /2.2.10

↓

VISUAL/MECHANICAL

↓

FINAL ACCEPTANCE

↓

PACK AND SHIP

NOTES

NOTE 1: **100% of the product will receive a minimum of one electrical test insertion per the manufacturing flow.**

NOTE 2 **Typical test temperatures are:**

MINIMUM	MAXIMUM	GRADE
- 0° C	+ 70° C	Commercial
- 40° C	+ 85° C	Industrial
- 55° C	+ 125°C	Military

NOTE 3 **Typical burn-in, when specified, is 160 hours at 125° C for Class Q and 240 hours at 125°C for Class V. Standard time/temperature regression tables in the product flow shall be used when applicable.**

TEST OPERATION FLOW
CLASS T

- OPTIONS. "If Applicable" are controlled via specific flows/travelers defined by current best practices.

LOT FORM

↓

100% ELECTRIC TEST (Optional Flow Dependent)

↓

BURN-IN

- BURN-IN CONDITIONS e.g. STATIC OR DYNAMIC, ARE DEFINED IN THE INTERSIL PART SPECIFIC APPLICABLE DETAIL DRAWING,160 HOURS, AT 125°C OR 120 HOURS AT 135
- PART SPECIFIC FLOW OPTIONAL POST BURN-IN ELECTRICAL (Room/low/high)

↓

BRAND

- FLOW DEPENDENT --BRAND MAY BE COMPLETED PRIOR TO BURN-IN

↓

VISUAL MECHANICAL (SAMPLE)

↓

FINAL ACCEPTANCE

↓

QUALITY TESTING (AS APPLICABLE)

- APPLICABLE GROUPS B,C.D AND E TESTING REFERENCE SECTION 2.2.10

↓

PACK AND SHIP

- MAY INCLUDE SILVER EPOXY DIE ATTACH INVENTORY

SECTION 2.2.6 QML LISTING COVERAGE

GENERAL

Intersil maintains an electronic database which lists all QML part types and their corresponding die technologies and package/assembly technologies.

QML LISTING COVERAGE SYSTEM

Intersil maintains a listing of all QML part types and their corresponding die technologies and package/assembly technologies in the Intersil "Oracle (COBRA)" and "Intrepid" database systems.

QUALITY SUPPORT DOCUMENTS

999017 Product Number and Structure Definitions

SECTION 2.2.7 PM/TCV/SEC PROGRAM

GENERAL

At Intersil a Process Monitor (PM) and a Technology Characterization Vehicle (TCV) are designed for each die technology.

A PM is used to obtain key electrical and physical data on product as it is being fabricated for the purpose of process control, scrap/continue processing decisions and a database for design model verification.

The TCV is used to characterize a technology's susceptibility to wear-out reliability failure mechanisms such as Electromigration, TDDB, etc.

Standard Evaluation Circuits (SEC)s may be an actual device selected for TCI (Technology Conformance Testing) testing or a special design qualification circuit. The SEC may be used as a surrogate for the purposes of TCI testing and as a vehicle for various yield improvement projects or RAD hard evaluations.

Intersil typically conforms to the microcircuit grouping for test coverage and does not utilize the allowed SEC program.
Reference paragraph 3.3 for a list of PM’s and TCV’s by technology

PROCESS MONITORS PROGRAM

Process Monitors are designed for measuring the wafer level electrical parameters and are on every wafer manufactured. The PM's are part of the Wafer Acceptance Testing consistent with Intersil standards for high quality and reliability. This electrical data is used for feedback to the Wafer Fab, provides pass/fail data relative to the wafers continuing processing, and provides a database for design to verify device models. Structures are also available for assessment of radiation effects, monitoring of oxide charge trapping, and other tests.

TECHNOLOGY CHARACTERIZATION VEHICLE PROGRAM

The TCV contains the structures necessary to fully characterize each process technology for each of the following "wear-out" mechanisms:

A. Electromigration
B. Hot carrier aging
C. Time dependent dielectric break down
D. Ohmic contact degradation

The designs of the TCV structures are to worst case design ground rules. Each TCV is fully processed through glassivation. The structures can exist in a fully independent mask set or as part of the PM or SEC. During the initial Reliability qualification of each new technology, the TCV structures are stressed to failure and statistically characterized. Once in production, the "wear-out" mechanisms are monitored on each run via the use of a critical node list. In addition design ground rules are modified, if necessary, to provide guard bands for guaranteeing sufficient life times.

STANDARD EVALUATION CIRCUIT PROGRAM

The SEC for each technology is either a product or a specially designed circuit. The SEC is used as a surrogate to demonstrate process reliability for the technology via TCI (Technology Conformance Inspection) testing. SEC's are selected from standard products or are specially designed on the basis of worst case design rules and level of complexity. For RHA environment, the SEC utilizes all relevant radiation hardness assurance design rules.

QUALITY SUPPORT DOCUMENTS

230415-QML Reliability Qualification Specification – QML

SECTION 2.2.8 INCOMING INSPECTION & VENDOR CONTROL PROCEDURES

GENERAL

Engineering, Purchasing, Manufacturing and Quality Assurance have established a system to insure that purchased materials conform to specified requirements.

INCOMING INSPECTION & VENDOR CONTROL SYSTEM

Reference the sections regarding "Purchasing & Receiving Inspection" of Intersil's Quality Manual.

QUALITY SUPPORT DOCUMENTS

Reference the sections regarding "Purchasing & Receiving Inspection" of Intersil's Quality Manual.

SECTION 2.2.9 SCREENING

GENERAL

All QML integrated circuits shall be subjected to and pass the screening tests as specified in the Screening Tables that follow. (Reference Class Q, Figure 2.2.9 A Class T Figure 2.2.9B, Figure 2.2.9C Class V)

A screening test may be eliminated or modified by the TRB when reliability data justifies the change. The qualifying activity will be notified of such changes. Approval from the qualifying activity is required for Class V product. (Reference Appendix B Para B.3.1 of MIL-PRF-38535)

MICROCIRCUIT SCREENING

Screening is performed in accordance with the wafer fab, assembly and test travelers. These travelers reference process specifications required to perform the appropriate screening tests.

QUALITY SUPPORT DOCUMENTS

233XXX	Quality Procedures
240111-XXX	QCI Test Inspection Procedures - Palm Bay

Screening Tables

Class Q Figure 2.2.9A	
Screen	**MIL-STD-883 test method**
1. Wafer acceptance	Sample PM electrical
2. Internal visual	2010 SOS/SCD Compliant Grandfathered material
3. Temperature cycling	1010
4. Constant acceleration	2001
5. Serialization	In accordance with device procurement specification
6. RAD Inspection	1019 RAD Level as specified in SMD
7. Interim (pre burn-in) electrical parameters	In accordance with device procurement specification
8. Burn-in test	1015
9. Interim (post burn-in) electrical parameters	In accordance with device procurement specification
10 Percent Defective Allowable (PDA) calculation	All lots or as required by device procurement specification
11. Seal a. Fine b. Gross	1014
12. External visual	2009

Class T Figure 2.2.9B	
Screen	**MIL-STD-883 test method or TRB/DLA approved alternate test method**
1. Wafer Lot Acceptance	PM electrical, SEM inspections, thickness and CV measurements are per the standard Class Q monitor program.
2. Internal Visual	2010 Condition B modified per 233750 (Intersil internal specification available upon request)
3 RAD Inspection	1019 RAD level as specified in the SMD
4. Interim Pre Burn-in Electrical Parameters	In accordance with device procurement specification
5. Burn-in	1015
6. Final Electrical Test	In accordance with device procurement specification
7 Seal (Sample)	1014 For devices assembled in solder seal packages the fine and gross leak seal test will be performed after the seal operation. The test will not be performed after the lead shearing/clipping or between the final electrical testing and external visual inspection operation. Time restrictions between die mount and seal do not apply
8. External Visual	2009

Class V Figure 2.2.9 C	
Screen	**MIL-STD-883 test method or TRB/DLA approved alternate test method**
1. Wafer Lot Acceptance	**5007 Plus PM Electrical samples** ***DLA approved acceptance criteria.** **Note 1 & 2. For SEM step coverage** **Note 3 & 4 for CV Test optimization.** **Note 5 SEM re-inspection of previously SEM qualified material.** **Note 6 for SEM Inspection Certification Requirements** **Note 7 SEM Sampling for product in die form** **Note 8 Alternate SEM for UHF2CMOS, P6 and UHF2 BI-CMOS Technologies**
2. Nondestructive Bond Pull	**2023 or Approved Alternate** **(Not applicable for RAD Hard power IC)**
3. Internal Visual	**2010 SOS/SCD Compliant Grandfathered material** **Reference Section 3.3 for Special AV/SI criteria**
4. Temp Cycle	**1010**
5. Constant Acceleration	**2001**
6. PIND	**2020**
7. Serialization	**In accordance with device procurement specifications (DLA approved lot formation allows 6 weeks Seal Window)**
8. Radiographic Inspection	**2012**
9. Interim Pre Burn-in Electrical Parameters	**In accordance with device procurement specification**
10. Burn-in	**1015**
11. Interim (Post Burn-in) Electrical Parameters	**In accordance with device procurement specification**
12. Reverse Bias Burn-in	**1015**
13. Interim (Post Burn-in) Electrical Parameters	**In accordance with device procurement specification**
14. PDA Calculation	**All lots or as required by device procurement specification**
15. Final Electrical Test	**In accordance with device procurement specification**
16. Fine & Gross	**1014 For devices assembled in solder seal packages at the Palm Bay Facility the fine and gross leak seal test will be performed after the centrifuge operation. The test will not be performed after the lead shearing/clipping or between the final electrical testing and external visual inspection operation.** **As of Seal Date code "0815", all Class "V", "S" and Condition "A" product sealed on or after 6th April 2008 in Palm Bay, will receive a 100% Gross Leak Test**
17. Seal	**Time restrictions between die mount and seal do not apply**
18. External Visual	**2009**
19 RAD Inspection	**1019 RAD level as specified in the SMD**

NOTE 1: Product that does not meet step coverage requirements per MIL-STD-883, Method 2018 will be evaluated for minimum metal thickness requirements using the following criteria:

1) **Current density of 2E5 A/CM2**
2) **Electro migration rules for the applicable technology**
3) **A minimum thickness of 2000 angstroms for mechanical integrity**

The thickest metal requirement calculated to meet the appropriate metal thickness will be used as the acceptance criteria for step coverage.

NOTE 2: Reference Section 3.3 for Special AVSLI acceptance criteria for moly.

NOTE 3: CV metal wafer lot for Test Method 5007 may be:

For CV acceptance using high vacuum, load lock metallization systems, all product processed through metal deposition under a continuous vacuum will be considered a wafer lot for CV testing and wafer lot acceptance

NOTE 4: CV monitor for gate oxide for Test Method 5007 may be:

The gate oxide for Class S devices will be monitored to the most stringent condition defined in test Method 5007 at the frequency specified in the internal Intersil process specification.

NOTE 5: The following sample plan will be used to reinspect and document step coverage results for product inventory previously SEM qualified to the full sample and test requirements in affect at the time of the original SEM.

Product in Wafer Form

Two random wafers will be selected and inspected per the requirements in the Intersil QM Plan 999015.

Product in Die Form

_ A total of 8 die from each wafer lot will be randomly selected and inspected per the requirements in the Intersil QM Plan 999015.

NOTE 6: Class V SEM Inspection Certification will be performed initially and for reinstatement after decertification as specified in Intersil specification 236000, when reports are reviewed, approved and signed off by engineering.

NOTE 7: SEM Sampling for product in die form

On rare occasions the die are scribed, sorted and loaded into die trays without selecting the sample for the specific wafer quadrants.

On these occasions the following alternate SEM sample selection procedure will be used.

- **A Material Review Board that includes the CORE TRB members for Wafer Fab will review the product history, process technology characteristics, etc. and approve the use of the alternate sample plan on a case by case basis.**
- **The practice of transferring uninked die from the wafer into die trays is to start at the top of the wafer and place electrical good units in sequential order working from left to right across the wafer and loading the tray left to right until the die transfer is complete.**
- **Wafer identity is maintained by die tray.**
- **Operators will randomly select two wafers from the lot for SEM inspection.**
- **The individual die will be selected as follows:**
- **Divide the number of die trays for each selected wafer by four.**
- **Use the resulting whole number to select the trays to be sampled.**

Example: Wafer #5 was selected for inspection and has a total of 12 die trays (12÷4=3) Sample from trays 3, 6, 9 and 12

NOTE 8: Alternate SEM acceptance method for UHF2 CMOS, P6, P6SOI AND UHF2 BI-CMOS Technologies

The planar process eliminates oxide steps that generate metal step coverage issues that are traditionally screened using Test Method 2018 inspection criteria. Five positions on each wafer in the lot are electrically tested to verify metal integrity including step coverage. The failure of one test site for metal integrity from the five sites tested will reject the wafer.

SECTION 2.2.10 TECHNOLOGY CONFORMANCE INSPECTION (TCI) PROCEDURES

GENERAL

TCI testing is performed on a periodic basis to assure that the quality and reliability requirements of QML product are being met. TCI testing includes applicable groups A, B, C, D & E-inspections for Class V, Class Q, and Class T product.

TECHNOLOGY CONFORMANCE INSPECTION (TCI) PROCEDURES

Notes from DLA approved test optimization implementation are applicable for all Class V,Q, and T product unless stated for a specific class or manufacturing location.

Class Q

Sample sizes, MIL-STD-883 test methods, test method sequence, etc. for group A, B, C, D & E testing are documented and are in compliance with MIL-PRF-38535 unless test optimization has been implemented as defined in the notes following the Class V table. Inspection lot definitions are also documented in internal specifications

QCI Requirements	QCI Vehicle
Group A testing 4/	Actual Device
Group B testing 3/	Actual Device
Group C testing 2/	SEC or Actual Device
Group D testing 1/	SEC or Actual Device
Group E testing *	Actual Device

*** = Group E performed as required to the level in the SMD drawing**

Class T

- Class V and Class Q test results may be used as an approved reference when available. As a minimum Class T endpoint subgroup testing will be the same as Class Q
- Sample frequency
  Group B Monthly by seal date, die attach, and package group
  Group C once every 4 Fab. Quarters by microcircuit group
  Group D Every 26 weeks of production by assembly site, seal date and die attach

QCI Requirements	QCI Vehicle
Group B testing 3/	Actual Device
Group C testing 2/	SEC or Actual Device
Group D testing 1/	SEC or Actual Device
Group E testing (Reference SMD for RAD level testing requirements)	Actual Device

Class V
Sample sizes, MIL-STD-883 test methods, test method sequence, etc. for group A, B, C, D & E testing are documented and are in compliance with MIL-PRF-38535 unless test optimization has been implemented as defined in the notes following this table. Inspection lot definitions are also documented in internal specifications

QCI Requirements	**QCI Vehicle**
Group A testing 4/	Actual Device
Group B testing 3/	Actual Device
Group C testing 2/	Actual Device or SEC
Group D testing 1/	SEC or Actual Device
Group E testing *	Actual Device

*** = Group E performed as required to the Level in the SMD drawing**

Note 1: **Group D QML - DLA approved Best Practice**

Inspection windows will be maintained by die attach and assembly site.
Intersil will maintain a total of six package families consisting of twelve package groups
Package families and window groups are as follows:

CERDIP	3-groups
Multilayer - Metal Lid Packages	1-group
Multilayer - Ceramic Lid Packages	1-group
Can	2-groups
CERPACK/CERQUAD	3-groups
Power Packages	2-groups

End point electricals will be at room temperature electrical test only
Lead finish will not be a QCI window grouping factor
Critical members of the TRB will review the root cause of any Group D failures
Product containment and additional testing will be determined based on data analysis and product reliability considerations.

Note 2: **Group C Approved Test Optimization**

Die attach material will not be a factor in maintaining Group C windows**.**
Class V Life Test results may be used as an approved reference for a lesser Hermetic QML grade when from the same diffusion lot.

Note 3: **Group B Approved Test Optimization**

Bond strength testing is not required as part of the Group B Test subgroups

Note 4: **Group A Approved Test Optimization**

Group A testing for room, high, low temperature testing is device specific for product tested at the Palm Bay Facility. Actual product is controlled by the Intrepid system. Product additions must be approved by the TRB

QUALITY SUPPORT DOCUMENTS

240111-XXX QML, QCI Inspection Procedures (Domestic)

SECTION 2.2.11 MARKING

GENERAL

Marking of QML microcircuits shall be in accordance with the detail specification or drawing (excluding die) and shall be legible, complete and meet the resistance to solvents requirements of MIL-STD-883, Method 2015.

MARKING

The marking of each QML microcircuit shall be as specified by the traveler and shall include:

a. The index point
b. PIN (Part Identification Number)
c. "Q" or "QML" certification mark
d. Manufacturers identification
e. Country of origin
f. Date code
g. Special marking
h. Electrostatic Discharge Sensitivity identifier

All the brand elements as stated will be specified by the traveler, or electronic media. Container marking shall include all of the marking requirements as stated above with the exception of the index point, serialization, and “Q” or “QML” certification mark.

SUBCONTRACTOR AND PALM BAY ASSEMBLY MARKING

Subcontractor assembly supplier codes are marked as follows:
ChipPAC Malaysia = Code H
Millennium Microtech = Code R
Amkor Philippines = Code L
Intersil Palm Bay = Code X

QUALITY SUPPORT DOCUMENTS

999053	Intrepid System
999017	Product Number and Structure Definitions
597002	Brand Specification Palm Bay

Applicable part specific Brand Pack Card (BPC) documents as defined in Intrepid

SECTION 2.2.12 REWORK

GENERAL

Rework or reprocessing devices or part thereof through a manufacturing operation shall be documented in accordance with the internal procedures and performed subsequent to the next manufacturing operation.

REWORK

Rework documentation for wafer fab, assembly and test are clearly specified in internal procedures. Operations that allow reworks are in compliance with MIL-PRF-38535. Documented processes procedures are included in the Intersil Specification System.

SECTION 2.3 FUNCTIONAL ORGANIZATION CHART

GENERAL

The organizational chart for Intersil Corporation can be found on our web site:
http://www.intersil.com/en/about-intersil/management.html

SECTION 2.4 CHANGE CONTROL PROGRAM

GENERAL

All changes to the Intersil QML program that could potentially have an effect on the quality, reliability, performance, or interchangeability of the resulting microcircuits shall be evaluated and approved by the members of the technical review board.

CHANGE CLASSIFICATION

All changes critical to the Intersil QML program are defined in appendix A "Guidelines for Change Classification" of Intersil Corporation specification 999004 'Change Notification Policy and Procedure'

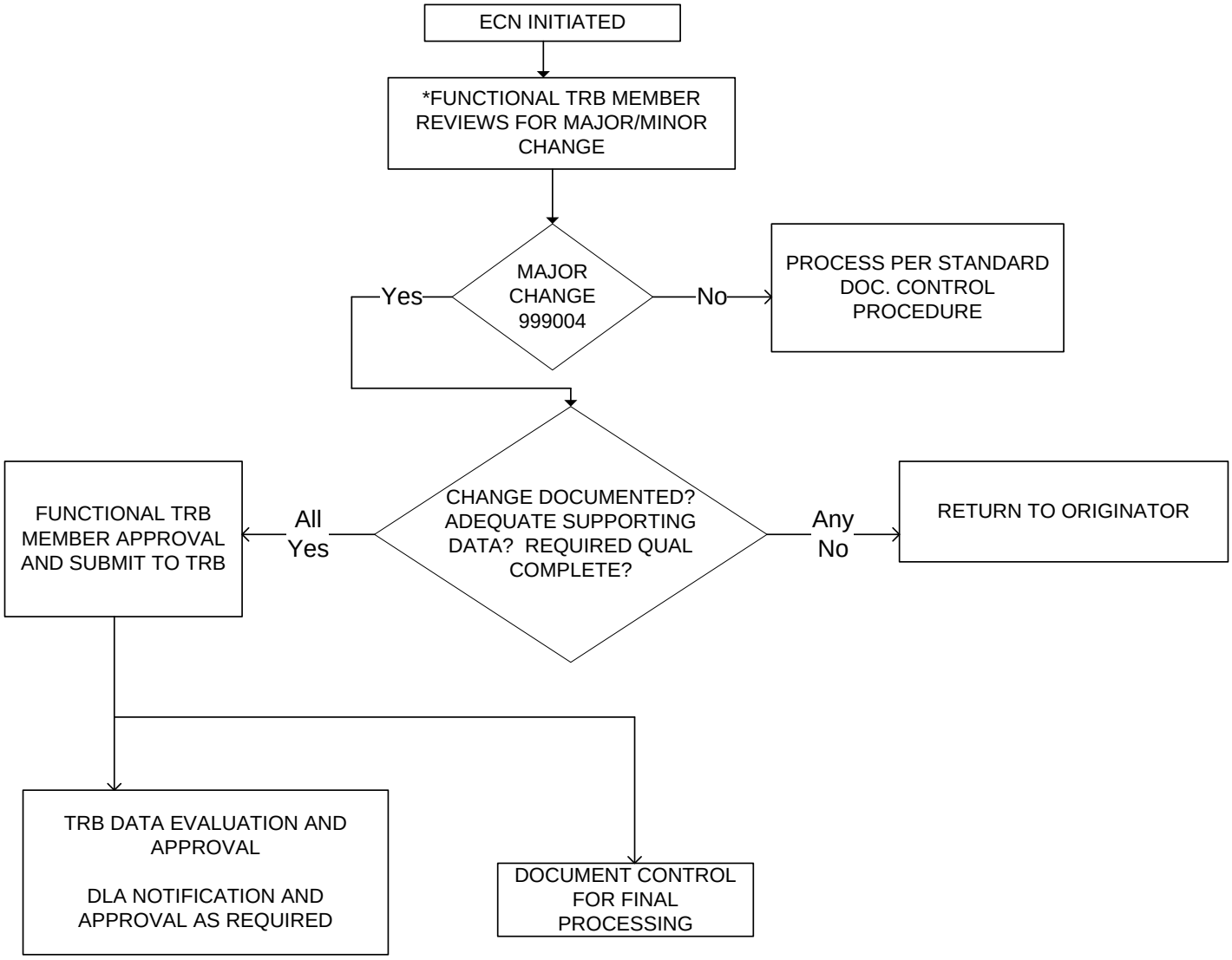
CHANGE PROCEDURES

The Intersil change control procedure is described in Intersil specification 999004 'Change Notification Policy and Procedure'

QUALITY SUPPORT DOCUMENTS

999004	Change Notification Policy and Procedure
DOC-PROC-ALL	Specification Control Procedures (Document Control)
999056-MASK	Change Review procedures for design changes
999056-PAT	Change Review procedures for Probe, Assembly, Test/Post Test
999056-FAB	Change Review Procedures for Wafer Fab and Wafer Fab Related operations

QML CHANGE CONTROL PROGRAM FLOW



*AREA FUNCTIONAL TRB MEMBER WITH SPECIFIC PROCESSING EXPERTISE AND 999004 KNOWLEDGE ON SUBJECT BEING CHANGED.

SECTION 2.5 FAILURE ANALYSIS PROGRAM

GENERAL

Intersil has established a failure analysis program, which analyzes failures from a wide variety of sources for determining the root cause of failure so that a meaningful corrective action and subsequent continuous improvement can be obtained. All failure analysis procedures have been established in accordance with MIL-STD-883, Method 5003.

FAILURE ANALYSIS PROGRAM

The responsibility of the Failure Analysis Laboratory is to provide the technical capabilities, equipment and personnel, necessary to support in-depth failure analysis of Intersil Corporation products. The analysis encompasses the isolation and identification of all failure modes/failure mechanisms, writing a comprehensive technical report and the assignment of appropriate corrective actions. Development of the capabilities for failure analysis also extends into research vital to understanding the basic physics of the failure.

Failure analysis is performed as a method of enhancing product quality and reliability and determining corrective actions. Failure analysis is the final and crucial step used to isolate potential reliability problems that may have occurred during reliability stressing. Accurate analysis results are imperative to assessing effective corrective actions. To ensure the integrity of the analysis, correlation of the failure mechanism to the initial electrical failure is essential throughout the failure analysis flow.

A general failure analysis procedure (see figure 2.5.A) has been established in accordance with the current revision of MIL-STD-883, Method 5003. The analysis procedure was designed on the premise that each step should provide information on the failure without destroying information to be obtained from subsequent steps. The exact steps used for an analysis are determined by laboratory personnel and contain data, the failure analyst's notes, the formal Product Analysis Report and the Failure Analysis Report.

The Failure Analysis Laboratory performs all analysis required internally for Intersil Corporation and externally for customers as described in Figure 2.5.B.

QUALITY SUPPORT DOCUMENTS

230354 Reliability Procedures for Failure Analysis

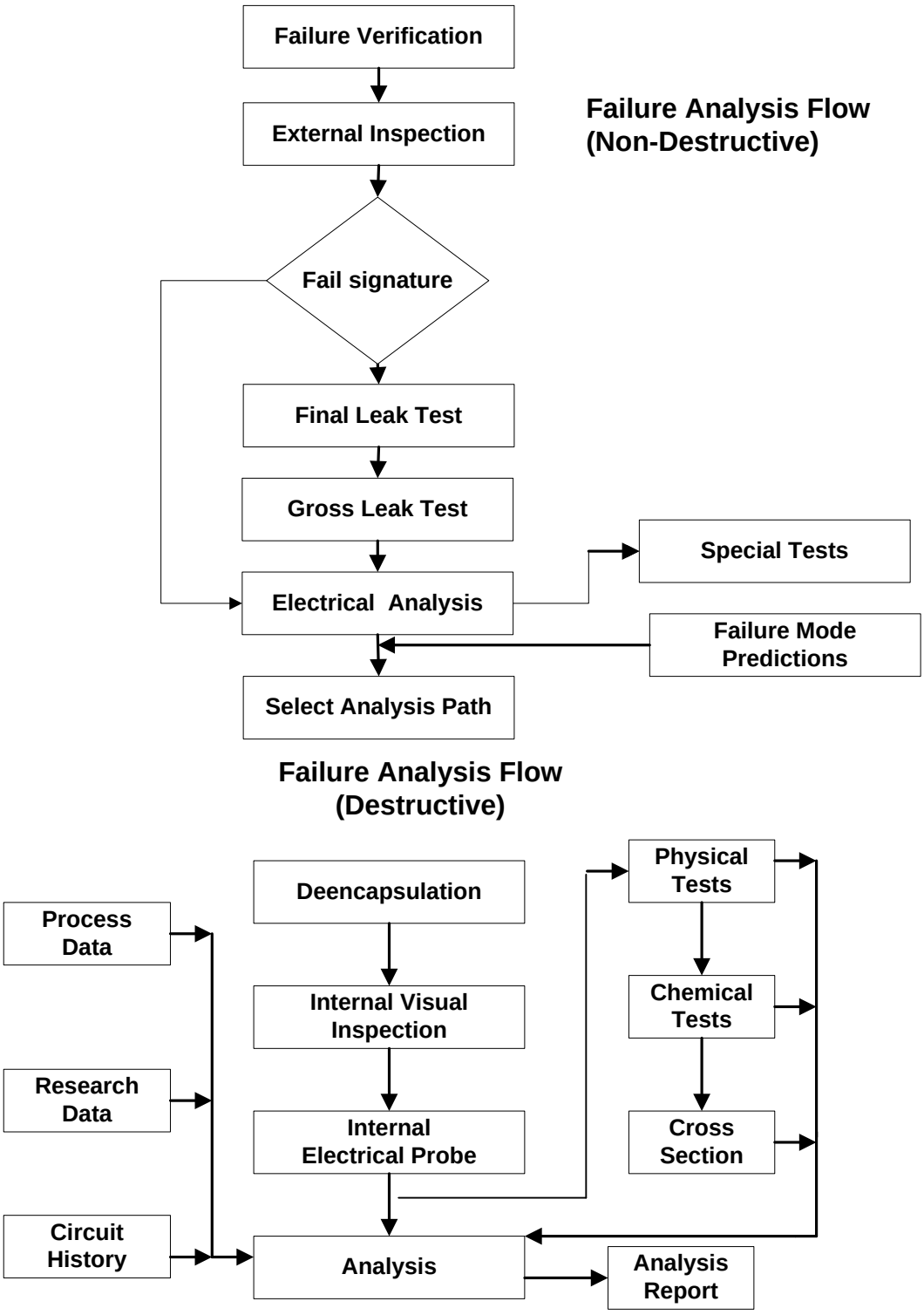


Figure 2.5.A

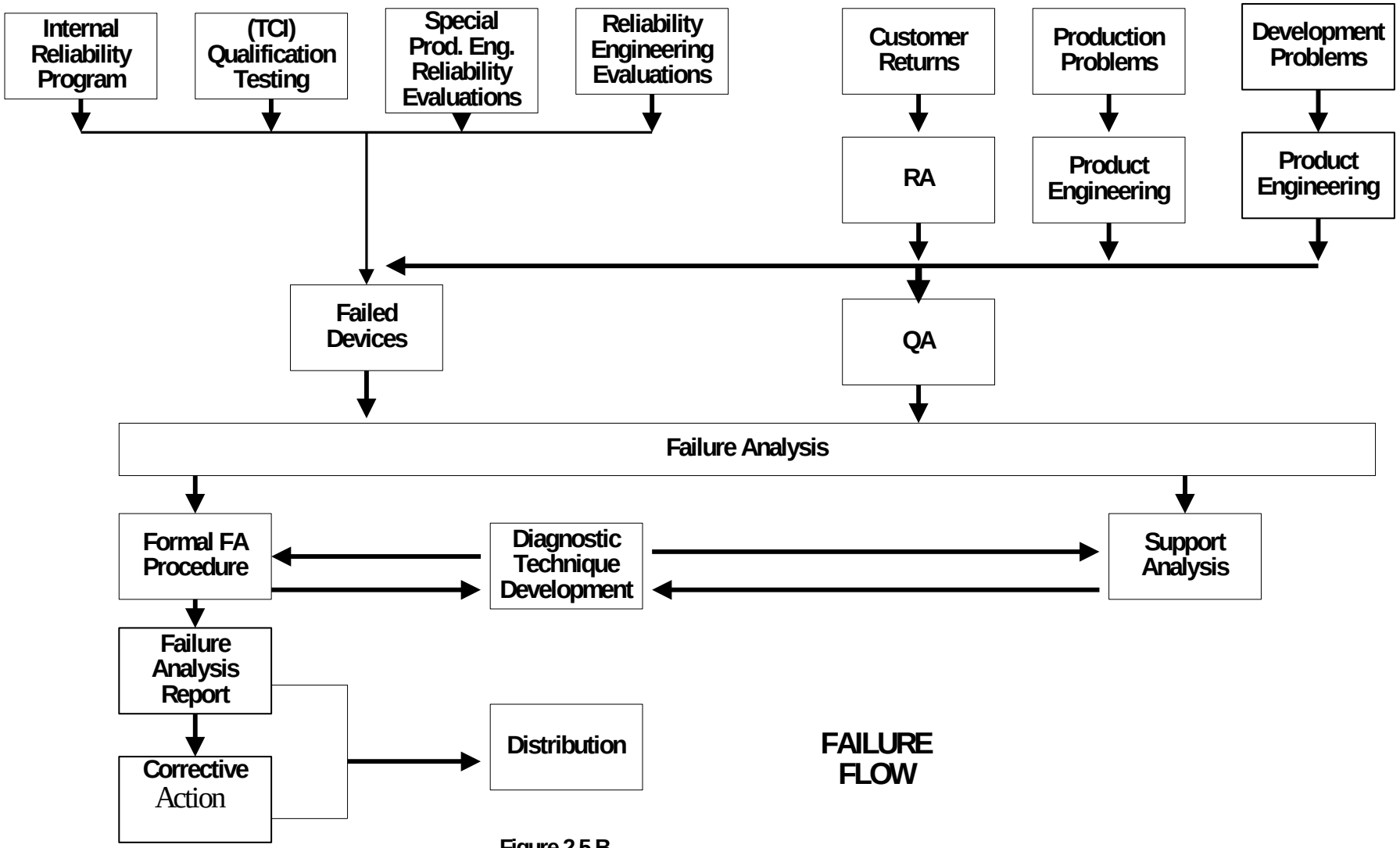


Figure 2.5.B

SECTION 2.6 SELF AUDIT PROGRAM

GENERAL

The internal quality audit is an essential element of the quality system. Regular audits are performed to ensure conformance to the overall quality system, specified process procedures, and specific customer requirements. Review of audit results identifies opportunities for continuous quality improvements.

SELF AUDIT PROGRAM

Reference the "Internal Audit System" section of Intersil's Quality Manual.

QUALITY SUPPORT DOCUMENTS

Reference the "Internal Audit System" section of Intersil's Quality Manual.

SECTION 2.7 TRB OPERATING PROCEDURES

GENERAL

Intersil has established a multi-disciplined TRB organization which is responsible for the development and maintenance of a Quality Management (QM) Plan, maintenance of all certified/qualified processes, process change control, reliability data analysis, failure analysis, corrective actions, QML microcircuit procedures, qualification status of the technology and reporting QML status to DLA.

TRB SYSTEM

The "Intersil" TRB is a multi-functional group representing worldwide operations. QML operations are located worldwide as shown in figure 3.2.A. The general TRB change control flow is shown in Figure 2.7.A.

The Intersil subcontractor quality team located in Kuala Lumpur Malaysia is responsible for reviewing all change notifications from the subcontractor. The Palm Bay TRB will review and approve major changes per guidelines established in 999004.

The Design Center at the Palm Bay facility is the only design active facility for QML products. Issues related to products initially designed at the Research Triangle Park facility in Raleigh N.C. (RTP) and the New Jersey facility are communicated through the TRB product engineering representatives. Each member is responsible for keeping management current on TRB/QML activities.

The Palm Bay TRB reviews and approves all subcontractor major changes.

The Intersil QML Coordinator is an active member of the Palm Bay TRB and coordinates all change communication to DLA and the end customer as appropriate.

DLA REPORTING REQUIREMENTS

The Intersil QML coordinator will notify DLA on a real time basis of Intersil major changes to product and or business activities. The notification will contain sufficient detail to provide DLA a basis for acceptance of the change.

On an annual basis, the QML coordinator will submit to DLA Intersil's status report in a format consistent with MIL-PRF-38535 appendix G paragraph G.3.2.3 and specification 999009 (Palm Bay "Technical Level" TRB – Rules and Procedures).

QUALITY SUPPORT DOCUMENTS

999009	Palm Bay "Technical Level" TRB Rules and Regulations
999004	Change Notification Policy and Procedures
999056-MASK	Change Review Procedures for design changes
999056-PAT	Change Review Procedures for Probe, Assembly and Test
999056-FAB	Change Review Procedures for Wafer Fab and Wafer Fab Related Operations

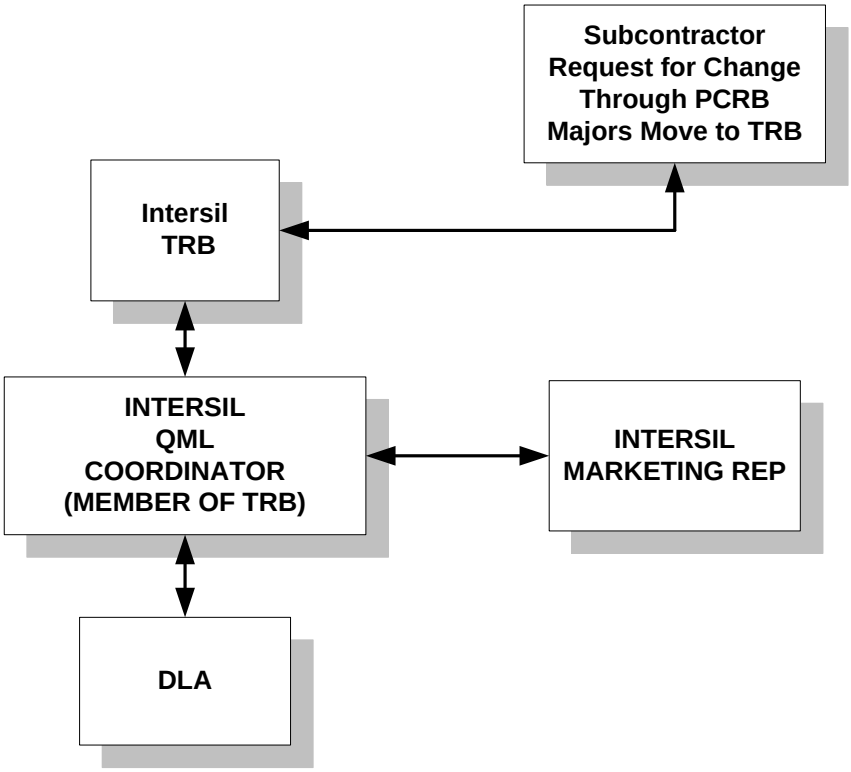


Figure 2.7.A

SECTION 2.8 YIELD/QUALITY IMPROVEMENT PROGRAM

GENERAL

Intersil operates on a policy of continuous improvement through the use of extensive employee involvement. To this end Intersil utilizes employee involvement teams (EIT's) and system involvement programs (SIP's) in continuous improvement activities using a variety of "problem solving" techniques. These continuous improvement activities are initiated when a need is identified by an area Team, Engineer or member of management.

YIELD/QUALITY IMPROVEMENT PROGRAM

Intersil has established 5 principles which guide its quality improvement efforts. These principles are customer focus, continuous improvement, employee involvement, supplier partnerships and highest standards of conduct, ethics and integrity. Each of these principles contributes to overall quality improvement. Both exempt and non-exempt employees can be involved in EIT's or SIP's. The appropriate levels of membership will be determined when the Team activity is initiated. Members of the various teams are trained in "team techniques" and "problem solving" methods in accordance with the training program available at their facility.

At the heart of all continuous improvement efforts is a corrective action system. Reference the "Corrective Action" section of Intersil's Quality manual, section 8.5.

QUALITY SUPPORT DOCUMENTS

Reference the "Corrective Action" section of Intersil's Quality Manual, section 8.5.

SECTION 2.9 SPC PROGRAM

GENERAL

Organized SPC activity at Intersil Corporation began in 1982 and has since matured into a culture that embraces SPC as a "way of doing business". Statistical Process Control is a significant tool used to achieve the goal, "to meet or exceed internal and external customer expectation", by providing continuous improvements in quality, value, and delivery of products and services. SPC for all designated critical processes are compliant to EIA 557 requirements.

SPC SYSTEM OF CONTROL

Reference the "Statistical Process Control" section of Intersil's Quality Manual.

QUALITY SUPPORT DOCUMENTS

Reference the "Statistical Process Control" section of Intersil's Quality Manual.

SECTION 2.10 LIST OF TEST METHODS FOR LAB SUITABILITY

GENERAL

Reference SECTION 2.2.10 for the Tables of Technology Conformance Test requirements for Class Q, V, and T. Testing is completed per MIL-STD-883 Method 5004/5005 and/or as defined by approved test optimization conditions documented in Section 2.2.10.

In the event of Intersil test equipment capacity restraints, the TRB may approve the use of a DLA approved test lab. The QML Coordinator will notify DLA of the temporary use of an alternate site not listed herein.

The SEM monitor program for Class Q product defined in MIL-PRF-38535, A.3.4.1.2.1 and A 3.4.1.2 has been modified as follows

The sample frequency and family groupings were determined by using the following guidelines.

- Product Family Identification and Sampling

  Group Technologies will be classified as families by process structure that impact step coverage and the wafer fabrication location.
- New QML technologies/products will be stand alone products and sampled on a routine basis until process controls demonstrate that there are no step coverage issue and the TRB approves the sample elimination.
- Class V lot acceptance SEM inspection data may substitute as the process monitor for the family process monitor requirements.
- Sampling and family groupings were approved by the TRB with DLA notification. The groupings are specified in Intersil document 241104.
- Routine SEM monitoring is not required for the following technologies:

  HBC-10
  HPA-2
  HVTDLM
  SAJI5/6

LIST OF TEST METHODS AND LOCATIONS FOR LAB SUITABILITY

TABLE 2.10 A

List of Lab Suitability by Location, Basic Test Method and Condition

Test Name	Method / Conditions	Intersil	Carsem	MMT	Amkor
Moisture Resistance	1004	X			
Steady State Life Test	1005/A-E	X	X[1]		
Salt Atmosphere	1009/A-D	X			
Temperature Cycling	1010/A-F	X		X	X
Thermal Shock	1011/B,C	X			
Seal	1014/A1,A2,B,C	X	X	X	X
Burn-in	1015/A-E	X	X[1]		
Internal Water Vapor Cont.	1018	X[2]			
Steady State Total Dose irradiation	1019/A,D	X			
Constant Acceleration	2001/A-E	X		X	X
Mechanical Shock	2002/B	X			
Solderability	2003	X	X	X	X
Lead Integrity	2004/B1,B2,D	X		X	X
Vibration, Variable Freq.	2007/A	X			
External Visual	2009	X	X	X	X
Internal Visual	2010/A,B	X		X	X
Bond Strength	2011/C,D	X	X	X	X
Radiography	2012	X			
Internal Visual for DPA	2013	X		X	X
Internal Visual and Mechanical	2014	X			
Resistance to Solvents	2015	X	X	X	X
Physical Dimensions	2016	X		X	X
SEM	2018	X			
Die Shear Strength	2019	X	X	X	X
PIND	2020/A,B	X		X	X

Test Name	Method / Conditions	Intersil	Carsem	MMT	Amkor
Glassivation Layer Integrity	2021	X			
Nondestructive Bond Pull	2023	X			
Lid Torque	2024	X	X	X	X
Adhesion of Lead Finish	2025	X	X		
Substrate Attach Strength	2027	X			
ESDS	3015	X			
Terminal Capacitance	3021	X			
Wafer Lot Acceptance	5007	X			
Electrical Test	Device Spec.	X	X		

1. Burn-in is subcontracted to KESM
2. IWV is subcontracted to Oneida or Pernicka

SECTION 2.11 CALIBRATION

GENERAL

The Calibration Laboratory functions are an integral part of the Intersil Corporation Quality Management System. Written procedures outlining the overall system and requirements for specific equipment calibration are maintained at each facility. All designated inspection, measuring, and test equipment used throughout the facility is identified and controlled in a known state of calibration.

CALIBRATION SYSTEM

Reference the "Inspection, Measuring and Test Equipment Calibration" section of Intersil's Quality Manual.

QUALITY SUPPORT DOCUMENTS

Reference the "Inspection, Measuring & Test Equipment Calibration" section of Intersil's Quality Manual.

SECTION 2.12 RETENTION OF QUALIFICATION

GENERAL

Intersil has defined internal process requirements to maintain qualification status once initial qualification has been completed. Intersil has established a set of criteria that is complied to. Non-compliance to this set of criteria results in removal of product or process from the QML listing by DLA.

RETENTION OF QUALIFICATION SYSTEM

The Intersil specification defining the qualification retention requirements also defines and addresses the issues of QML line shutdown and QML removal.

The following is a list of reasons for removal from the QML listing by the Qualifying Agency:

- The QML product does not meet the quality, reliability or performance requirements of MIL-PRF-38535 and Intersil is unable to implement a corrective action plan as defined in this document.
- The QML microcircuit offered under contract does not meet the device procurement specification requirements.
- Intersil has terminated the QML technology which was qualified.
- Intersil requests its name and associated product be removed from the list.
- One or more of the conditions under which certification and qualification was granted have been violated.
- Intersil has failed to notify the qualifying activity of change in procedures, processes, etc., in accordance with the change control procedures of MIL-PRF-38535.
- Intersil's name appears on the "Consolidated List of Debarred, Ineligible and Suspended Contractors".
- Intersil has not complied with the requirement for retention of qualification, as stated in its internal specification.
- Intersil has failed to provide a certified statement, when QML microcircuits are supplied under contract for direct or indirect Government use, that such QML microcircuits have been tested to and met all the requirements of MIL-PRF-38535.

QUALITY SUPPORT DOCUMENTS

240111 QCI Qualification Procedures

SECTION 2.13 TRAINING

GENERAL

Training is a key element in the overall quality system. The system is designed to provide Intersil employees with the necessary skills and knowledge to perform tasks in a highly technical environment. The Training Department, Human Resources Department and the Manufacturing Department have the responsibility and authority to identify and implement effective training programs for all personnel.

Employee development training opportunities include, but are not limited to: financial support for advanced education and employee growth training through the corporate-wide center for training and development. Services are provided for technical and administrative training and development.

TRAINING

Reference the "Training" section of Intersil's Quality Manual.

QUALITY SUPPORT DOCUMENTS

Reference the "Training" section of Intersil's Quality Manual.

SECTION 2.14 CLEANLINESS AND ATMOSPHERIC CONTROLS

GENERAL

Specifications that define the cleanliness and atmospheric controls in a variety of process areas have been established in order to build product of the highest quality and reliability.

CLEANLINESS AND ATMOSPHERIC CONTROLS

Unique cleanliness and atmospheric controls are required to fabricate integrated circuits. Intersil has established a required set of specifications which define the requirements in the wafer fab and assembly areas. Clean room standards have been developed to minimize product contamination during processing. In addition, temperature and humidity limits are defined for critical process and storage areas and are monitored accordingly.

QUALITY SUPPORT DOCUMENTS

880035	Clean Room Procedures (Fab 59)
233151-T	Test and QCI Environmental Control
233151-A	QC Environmental Monitor Assembly

SECTION 2.15 ESD PROGRAM

GENERAL

In order to preclude ESD damage to product, Intersil has established an ESD program for handling product in all areas starting with die separation and through final product shipment including shipment to customers.

ESD PROGRAM

The Intersil ESD program was established using MIL-HDBK-263 and MIL-STD-1686 as a guide. The system, compliant to JESD625, includes all areas beginning with die separation and continuing through final product shipment including shipment to customers. Specifications have been generated which define the use of static-free work stations, the use of air ionization, ion guns and details of proper ESD handling, packaging and storage procedures. All applicable Intersil Manufacturing and Support personnel receive ESD training.

QUALITY SUPPORT DOCUMENTS

233403	ESD Procedures (Palm Bay)

SECTION 2.16 CERTIFICATION TEST PLAN

GENERAL

Intersil Corporation has manufacturing operations in Palm Bay, Florida and subcontracted services for production as stated. Intersil manufactures a large variety of QML parts using many technology flows. Intersil has transitioned parts into QML via the "Transitional QML" option and has obtained QML status for existing technologies. This section describes a general (non-technology specific) certification test plan for new technologies. Specific technology flow certification test plans will be written on an as required basis.

CERTIFICATION TEST PLAN

QML Certification Test Plan for New Products.

- Process/Product capability demonstration.
- Intersil Quality internal validation.
- Qualifying activity management and technology validation.
- Demonstration of manufacturing control of any offshore operations.

QML Certification Test Plan for New Technology

A formal certification test plan will be approved by the TRB for each technology flow to be certified. This plan will include:

- Milestone charts outlining the tests to be used to certify the processes.
- Tests to be accomplished on the TCV, SEC, PM, and TCI.
- For RHA parts, a RH evaluation plan

QUALITY SUPPORT DOCUMENTS

230415-QML RELIABILITY QUALIFICATION SPECIFICATION- QML

QML PROGRAM

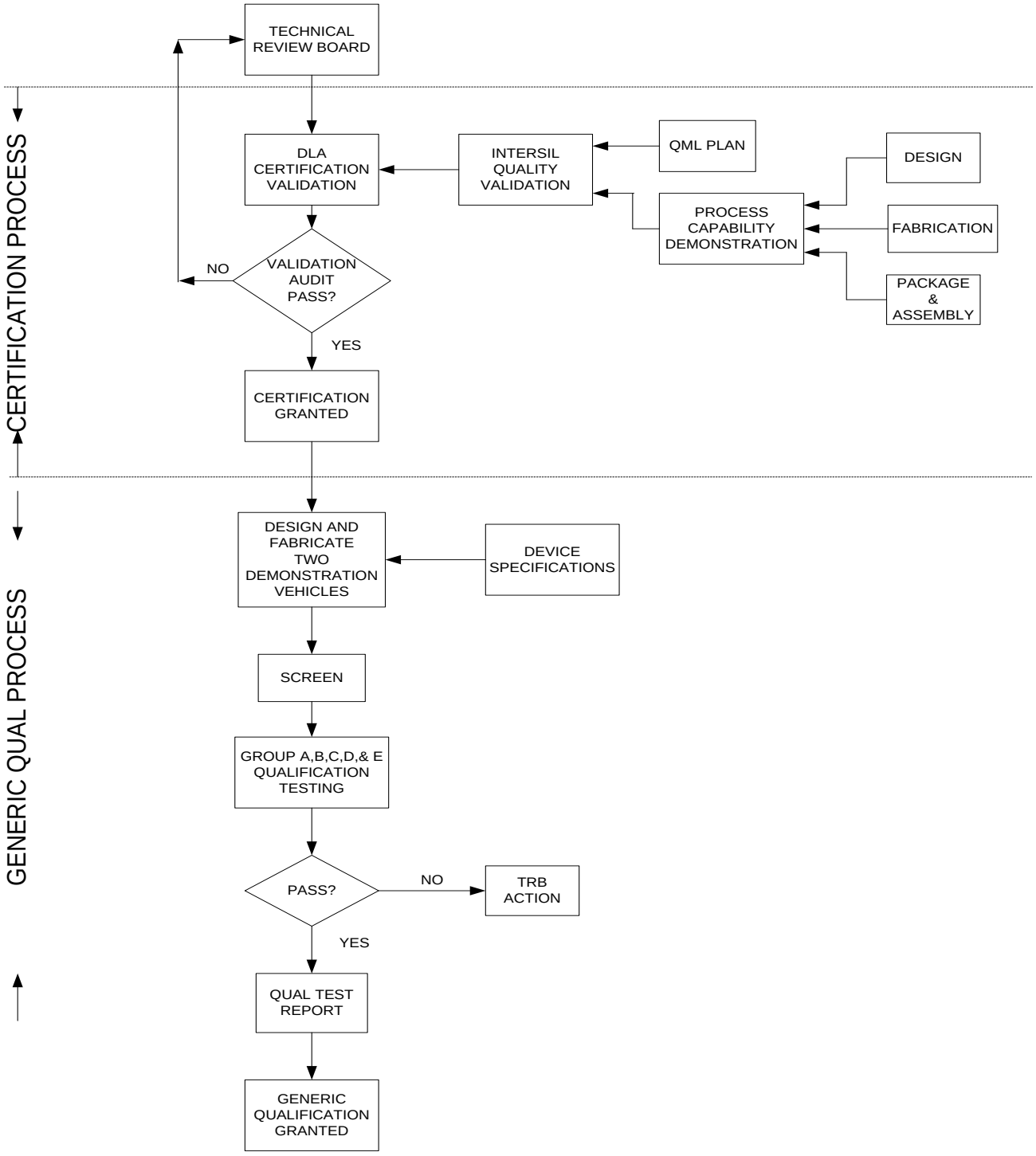


FIGURE 2.16.A

SECTION 2.17 QUALIFICATION TEST PLAN

GENERAL

Intersil manufactures a large variety of QML parts using many technology flows. Intersil has transitioned parts into QML via the "Transitional QML" option and has obtained QML status for existing technologies. This section describes a general (non-technology specific) certification test plan for new technologies. Specific technology flow certification test plans will be written on an as required basis.

QUALIFICATION TEST PLAN

A. **Qualification Test Plan for New Products/Technologies**

In order to obtain QML qualification for a specific technology flow, the following requirements must be met:

- Demonstration circuits will be designed and fabricated using the technology flow to be qualified.
- SMD format specifications will be generated for the demonstration circuits.
- The demonstration circuits will be assembled, tested, screened and submitted to qualification testing. See Figure 2.16.A.

B. **Qualification Test Report for New Products/Technologies**

A qualification test plan and report will be generated and submitted to TRB for formal acceptance.

.

This plan and subsequent report will typically include:

- test flow
- test limits
- % test coverage
- test sampling techniques
- traceability records
- technology flow
- SMD format specifications for the determined demonstration vehicles
- milestone charts

QUALITY SUPPORT DOCUMENTS

230415-QML	Reliability Qualification Specification – QML
230479	Technology Characterization Vehicles
	Section 3.3 of this document for additional information

SECTION 2.18 CORRECTIVE ACTION

GENERAL

The quality system provides an effective corrective action program which involves investigating the root cause of the problem and taking measures to prevent recurrence.

CORRECTIVE ACTION

Reference the "Corrective Action" section of Intersil's Quality Manual.

QUALITY SUPPORT DOCUMENTS

Reference the "Corrective Action" section of Intersil's Quality Manual.

SECTION 2.19 THIRD PARTY ACTIVITIES

GENERAL

Intersil exercises the option to use third party sources for product design, wafer foundry, assembly and test operations. The selected operation may be completed in part or in total by the third party.

THIRD PARTY

All third party suppliers are approved by an Intersil team to insure that an effective quality system has been implemented by the supplier. Standard operating procedures used by the supplier to generate the finished product/test will be assessed by Intersil personnel. Assessment tools may include but are not limited to a review of the process monitor program, physical assessment of the quality systems, and finished product evaluations.

Team members include applicable representatives from Quality, Reliability, Product, and Production Engineering. When the scope of the third party operation includes processes for QML material, required TRB members will review and approve the assessment plans and final data prior to product being processed for QML applications. The facility will be added to the QML plan.

Intersil personnel will generate a procurement specification for each third party supplier detailing the product/services and quality requirements necessary for compliance. All details of the specification will be negotiated and approved by the third party supplier and required Intersil personnel. Any major changes, as defined per 999004, will be presented to the applicable TRB for approval.

QUALITY SUPPORT DOCUMENTS

210XXX	Procurement Specifications
XXXXXXX	Specific series as identified with each purchase of product or services
449-816-003-X	Baseline Manufacturing Specification for Subcontractor
449-800-001	Intersil Quality and Reliability Requirements for Intersil Assembled Product

SECTION 3.0 QML TECHNOLOGY SPECIFIC

GENERAL

This section of the Intersil QM Plan provides a description of the following

- A database system used to control the internal Intersil specifications used to fabricate each part type of every technology.
- A list of critical process/product internal specifications
- Technology Grouping guidelines and list of QML technologies

SECTION 3.1 INTERSIL QML ELECTRONIC DATABASE SYSTEM

GENERAL

A listing of all the QML parts produced by Intersil Corporation can be found in the Intersil Electronic Database System. By using the database, reports can be generated to provide the following information for each part type:

Marketing (Military) Part Number
Intersil marketing part number
Product Description
Die technology name/flow
Process location (Design Center through Product Ship)
Starting Substrate material procurement specification
Base Wafer Mask Number
Flow/Traveler numbers (Wafer Fab/Assembly/Test/QCI)
Wafer Fab product parameter specification number (as applicable)
Bonding diagram specification number
Package procurement specification number
Package code
QCI traveler number

In addition, the Intersil Document Control electronic data base system (Intrepid) is capable of providing a listing of the required product flows, process travelers, material, inspection and testing documents, etc for each part number. Therefore the actual applicable specifications are not included in the QM Plan document.

SECTION 3.2 TECHNOLOGY FLOW

GENERAL

Intersil Corporation produces a multitude of QML parts from a wide variety of technologies. These parts are designed and manufactured in various locations throughout the world. For the purposes of this plan, a technology flow is defined as a manufacturing line which includes design, mask making, material fabrication, wafer fabrication, assembly/packaging and test. Each product family has a unique combination of the elements of a manufacturing line which form its "technology flow".

INTERSIL TECHNOLOGY FLOWS

The technology flows for each of the Intersil QML product families can be found by accessing the Intersil Electronic Databases. Figure 3.2A provides a listing of the manufacturing/design locations that are used by Intersil to produce its QML products. Each technology flow is a unique combination of the various location/fabrication sites found in Figure 3.2A.

INTERSIL TECHNOLOGY GROUPING GUIDELINES

The following guidelines will be used to identify the appropriate technology grouping for each new product and identify the TCV, PM and SEC circuits within the group.

- Products must have the same isolation type
  - JI – junction isolation
  - DI – dielectric isolation
  - LOCOS – local oxide
  - REOX – recessed oxide
  - BW – bonded wafer oxide isolation
  - SOS – silicon on sapphire
- Have the same basic device structures and technology
  - NPN/PNP (Bipolar)
  - P and N channel FET's (CMOS)
  - P/Nch FET's and Bipolar NPN/PNPs (Bi-CMOS)
- Have the same basic layout ground rules
  - Minimum feature size
  - Same number of metal levels
- Have the similar application voltage
- Have the same gate material
  - Poly
  - Aluminum
- Have the same FAB location
  - FAB 59
  - UMC
  - TowerJazz
  - Global (IBM)
  - FAB 54 (Fab is inactive, Product is in a Die Bank)
  - FNDLY 4/5 (Fab is inactive, Product is in a Die Bank)
  - MITEL (Fab is inactive, Product is in a Die Bank)
- Must contain ½ the number of transistors of the largest die (for Digital)
- Represents the functionality of the process (for Analog)
- Has all the major circuit elements
- Fully functional circuit
- Product designed to the ground rules of the technology
- Can be tested for RAD Hard Assurance if required
- Has sufficient volume that it should be readily available for testing
- For a product to be selected the subteam must reached consensus that if the product yields and is reliable other products on the process will yield and be reliable.
- When the subteam has reached consensus on the product selection the product listing will be presented to the TRB for approval.
- Once approved by the TRB the table in Section 3.3 of the QM Plan that list the, PM's & TCV's by technology and fab will be formally changed through an ECN (Engineering Change Notice).

	Intersil Palm Bay, Florida	Intersil New Jersey	Intersil RTP, N. C.	UMC Taiwan	Yamaha Japan	Global (IBM) Vermont	Stats ChipPAC Kuala Lumpur, Malaysia	Micro Millennium Thailand	Amkor Philippines	Criteria Labs Texas	Carsem Malaysia	Corwil CA.	Integra-Tech Kansas
DESIGN	X	X 1)	X 1)										
WAFER FAB	X			X	X	X							
WAFER PROBE	X									X	X		
ASSEMBLY	X							X	X			X	
TEST	X						X						X

NOTE: 1) NO DESIGN ACTIVE PRODUCT FOR QML IS CURRENTLY DESIGNED AT THE NORTH BRANCH OR RTP FACILITY.

FIGURE 3.2A

Section 3.3

General:

The following is a list of the PM's & TCV's by technology

LIST OF PM's & TCV's

Die Technology	PM	TCV	FAB LOCATION
CBL STD LINEAR HFHIB HFSTDB	TA3841 TA3772 TA3842 TA3772 TA3882 TA3772	Transitioned Process (See Note 1)	P59
CMOS2	TA 11462	Transitioned Process (See Note 1)	FNDLY
MGDE MGFFMGTF MGLF MGLV	TA XP0366X TA XP0366X	Transitioned Process (See Note 1)	FNDLY
MGHV	TA XP0364 TA XP0364	Transitioned Process (See Note 1)	FNDLY
MG_CMOS	TA 10916	Transitioned Process (See Note 1)	FNDLY
MGR_CMOS	TA 10916	Transitioned Process (See Note 1)	FNDLY
BIMOS-4	TA XP0365	Transitioned Process (See Note 1)	FNDLY
HVTCOM	TBD	Transitioned Process (See Note 1)	P54
VHF (DLM) HFStdB (DLM)	TBD	Transitioned Process (See Note 1)	P54
HFSB	TA 03226	Transitioned Process (See Note 1)	P54
ALPS	UNKNOWN	Transitioned Process (See Note 1)	P54

Die Technology	PM	TCV	FAB LOCATION
SAJI I SSAJI IV	TA 00309 TA 00823 TA 01223	Transitioned Process (See Note 1)	P59
SSAJI4RH	TA 3004 TA 3189 TA 1794 TA 3150 TA 3327 TA 1507 TA 3750 TA 3121	Transitioned Process(See Note 1)	P59
LCMOS	TA 3534	Transitioned Process (See Note 1)	P59
MGCMOS-RH	TA 10916	Transitioned Process (See Note 1)	P54
SOSLT	TA 13474 TA 14394 TA 14494 TA 13353 TA 13474	Transitioned Process (See Note 1)	FNDLY
CMOS3AMT	TA13086B used on projection aligned process TA13086C used on stepper aligned process	Transitioned Process (See Note 1)	FNDLY
SIGATE HVSIGATE	TA 03927 TA 3772 TA 50388	Transitioned Process (See Note 1)	P59
SAJI5/6	TA50552A	Transitioned Process (See Note 1)	P59
L7	TA 03352M TA 51122A	Transitioned Process (See Note 1)	P59
TSOS4	RTP FACILITY NO FURTHER PM PROBE REQUIRE-MENTS	Transitioned Process (See Note 1)	RTP
UHF	TA 50538	TA 50539 TA 50102	P59
UHF 1X	TA51410	TA51408	P59

Die Technology	PM	TCV	FAB LOCATION
BHFP	51328	TA51608	P54
BVHF	51329	TA51607	P54
AVLSI A1 A1	51600	51433	P59
AVLSI A1RA A1R	51600	51433	P59
AVLSI 1RF	51600	51433	P59
HBC-10	TA51422J01	TA50550J01	P59
HPA2 60V,21 Mask 420747	TA51233	TA50728B	P59
HVHPA2 100v,22Mask 420748	TA51233	TA51331A	P59
HPA2 60V,14 Mask 420749	TA51233	TA50728B	P59
SOS5	12379_C (MITEL)	TA51453 TA13133	Mitel
JIJFET	TA01761A	Transitioned Process (See Note 5)	P54
HFP		Transitioned Process (See Note 6)	P54
RH-SIGATE	TA51684	TA51685	P59
BL-TF	TA-(TBD)	Transitioned Process (See Note 5)	FNDLY
HVTDLM	TA52469A	TA52228A	P59
UHF2/CMOS	TA51843A	TA51843A	P59
BiMOS-ESD	52520A	ICL3224	Fab 59
PR40	TA53743	TA53850A	Fab 59
P6	N/A	53141A	Global (IBM)
P6SOI	N/A	54048C / D	TowerJazz

Notes:

1 Transitional Processes: Old technologies that have been transitioned to QML by Intersil Corporation do not have the QML tools such as Technology Characterization Vehicles (TCV's) and Standard Evaluation Circuit (SEC's), etc.; these technologies have years of QPL listing, extensive field history and compliant life test data

to supplement the TCV and SEC data. Reliability data reports are generally available on the World Wide Web at: http://www.intersil.com/en/support/qualandreliability.html

2 During the qualification and subsequent production of the AVLSI-A1,-A1A, -A1R and -A1RA Wafer Fabrication processes at the Palm Bay manufacturing facility, the Metal 1 Molybdenum (Moly) exhibited a seam at certain steps traversing closely spaced Poly silicon lines. Reliability analysis of these seams, which included SEM analysis, Field Emission SEM analysis, Electromigration stu8dies and Product Stress Testing, showed no failures on representative samples exhibiting these seams. Based on these test results, the Moly seams will be inspected during SEM but will not be dispositioned based on the physical appearance of a seam. All other Mil-Std-883, Test Method 2018, SEM criteria as modified by this QM Plan (see Note in Figure 2.2.9.B) will apply.
Reference Reliability Report: Reliability Special Report Covering Moly On AVLSI-A1, -A1A, -A1R & -A1RA Processes.

3 The AVLSI A1RF product periodically exhibits small reductions in Metal 1 width and Metal 1 depth caused by a wafer fabrication process anomaly. These reductions in Metal 1 dimensions can appear as a void during the assembly high power dice inspections. Reliability SEM analysis and current density analysis shows that void anomalies in Metal 1 that are $\leq 50\%$ are acceptable even in an extreme event that the Metal 1 conductor and barrier metal are missing. The assembly inspection criteria will be modified in Intersil internal documentation to reflect accepting AVLSI A1RF material exhibiting a $\leq 50\%$ Metal 1 line width reduction for voids as described herein.

4 Product technologies marked with an * are in the design and product qualification phase. Upon qualification completion and TRB approval product will be added to the QML product list and DLA certification listing.

5 Part overlooked when original list of transitional processes developed

6 Part and process added to support MMIII GRP.

SECTION 4.0 SITE QUALITY SYSTEMS MANUALS

The Quality Manual may be requested or may be accessed through the Intersil Corporation web page http://www.intersil.com/design/quality/manuals.asp. The specification number for the manual is:

QOP-ISL-001 Intersil Corporation Quality Systems Manual

APPENDIX A

RADIATION HARDNESS ASSURANCE (RHA)

SCOPE
This appendix presents Intersil' approach to RHA.

GENERAL
Microcircuits supplied to this document shall be manufactured and tested in accordance with Intersil' approved baseline manufacturing flow and requirements herein.

DESIGN APPROACH
Intersil uses three methods in its design approach to satisfied new circuit requirement:

1. Design specifically for radiation hardness to the approved ground rules of the intended radiation hard wafer process.

2. Standard commercial designs built using a qualified process that is capable of producing circuits that meet the intended radiation requirements.

3. Product that is hardened by design, built using a qualified process that is capable of producing circuits that meet the intended radiation requirements.

MODEL AND DESIGN RULE VERIFICATIONS
Various methods and procedures were used in the portfolio of standard radiation hardened products being offered under this QM PLAN. These products were all designed or design verified to meet the intent of MIL-M-38510 and were designed released prior to the requirements of MIL-PRF-38535. New products developed after October 1, 1995 will follow requirements as outlined in MIL-PRF-38535

WAFER FABRICATION PROCESS CONTROLS AND PROCESS MONITOR
All radiation hardened products are produced on a specific radiation hardened wafer process or a process capable of meeting the radiation requirements as required (see radiation technology table B-1). The process specification/flows contain the details of each process and controls applicable to the specific process.

Each technology has a unique Process Monitor (PM) structure which is used for wafer acceptance and process control.

TECHNOLOGY CHARACTERIZATION

Selected product types from each technology were tested/characterized by Intersil, our customers or a government agency to the following radiation testing:

a) Total Ionizing Radiation Dose (Condition A and Condition D)
b) Dose Rate Upset
c) Dose Rate Latch-up
d) Neutron Irradiation
e) Dose Rate Burn Out
f) SEP including SEU, SEL, SEGR, SEDR, etc…, as required..

The specific radiation testing and specified limits for each Radiation Technology will be contained in the specific product Standard Microcircuit Drawing (SMD).

Upon product redesign, a process change, or a design rule change, that effects radiation performance as determined by the TRB retesting and characterization will be performed.

GROUP E TESTING

Total Ionizing Radiation Dose testing (Condition A and Condition D) is performed per MIL-STD-883, Method 1019 latest revision on every wafer with a minimum accept level of 2 (0).

TABLE A-1

Die Technology	Technology Description	Product Family	Product Function	Process Design Active
MGR_CMOS	Metal Gate Radiation Hardened CMOS	CD4XXX	logic	No
SOSLT	Silicon Gate Radiation Hardened SOS	HCS/HCTS	logic	No
TSOS 4	Silicon Gate Radiation Hardened SOS	Acs/Acts	logic	No
TSOS 4	Silicon Gate Radiation Hardened SOS	HS6566XXXRH	64K Rams	No
SOS 5	Silicon Gate Radiation Hardened SOS	Acs/Acts	logic	No
SOS 5	Silicon Gate Radiation Hardened SOS	HS6566XXXRH	64K Rams	No
AVLSI 1RA	Radiation Hardened JI CMOS	HS9008RH	A/D	No
AVLSI 1RF	Radiation Hardened JI CMOS	HS6664RH	64K Prom	No
AVLSI 1R	Radiation Hardened JI CMOS	26cxxxRH	Line Driver/Receiver	No
SSAJI4RH	Hardened Field Self Aligned JI CMOS	HS'80C86RH,82CXXRH	uP'S & Peripherals	No
SSAJI4RH	Hardened Field Self Aligned JI CMOS	HS6617RH	16K Prom	No
SSAJIIV	Self Aligned JI CMOS 7um EPI	MD'80C86,82CXX	uP'S & Peripherals	No
MGCMOS	DI Radiation Hardened Metal Gate CMOS	HS3XXRH	Analog Switches	No
STD LINEAR	DI Bipolar	HS2XXX	OP AMPS	No
HFHIB	DI Bipolar	HS565A	12 BIT A/D	No
HFSTDB	DI Bipolar	HS5104ARH	QUAD OP AMP	No
HFSB	DI Bipolar	HS245RH	Line Transmitter	No
ALPS	DI Bipolar	HS246RH,HS248RH	Line Receiver	No
BVHF	Bipolar Bonded Wafer	MM III	Various	No
BHFP	Bipolar Bonded Wafer	MM III	Various	No
RH-SIGATE	DI CMOS	HS1840ARH	Analog Multiplexer's	Yes
UHF	Ultra high frequency Bipolar bonded wafer	ISL7312X	Transistor array	No
LCMOS	Linear BI-CMOS	HS-0546, HS-0547	Analog multiplexer	No
EHV60	UMC CMOS Embedded High Voltage	ISL7457	CMOS driver	Yes
P6	Global (IBM) BiMOS	ISL70001XX	Regulators	Yes
HVTDLM	Bipolar Bonded Wafer	IS-2981	High current driver	No
UHF2	Ultra High Frequency Bipolar bonded wafer	IS-705	uP Supervisory ckt	No
PR40	Complimentary BiCMOS 40V Bonded Technology	ISL70218	Dual Op Amp	Yes
P6SOI	Complimentary BCD SOI process	ISL7184xEH	Analog multiplexer	Yes

APPENDIX B

QML SHIP AHEAD OF QUALIFICATION TESTING (QCI/TCI) TO MEET CUSTOMER REQUIREMENTS

1.0 SCOPE

QML system for shipping QML product prior to QCI/TCI test completion.

NOTE: 1 This procedure is to be used in the event of hardships that would be incurred by the customer, by delaying shipments for qualification (QCI/TCI) test completion. The procedure may also be used with joint concurrence with the customer for other mutually agreed to situations.

2.0 REFERENCE DOCUMENTS

999032 SHIP AHEAD OF QUAL INSTRUCTIONS AND NON-STD

3.0 RESPONSIBILITIES and REQUIREMENTS

3.1 The Intersil Marketing Manager is responsible for completing and routing the Ship Ahead of Qualification approval form contained in specification 999032.

3.2 The following minimum information will be included on the Ship Ahead of Qualification request: SMD part number and Date Code. The Date Code is only applicable to the form if the product is past the assembly seal operation.

Customer name and name of the customer contact making the request for Ship Ahead of Product QCI/TCI test results.

Reason for shipping ahead of qualification.

3.3 The initiator is responsible for routing the request to the following minimum for Material Review and Approval:
Military Marketing Manager
Production Control Manager
Contracts Administrator
Customer Engineering Manager
Test Area Quality Engineering (See para 3.4 for approval responsibility).

3.4 The Test Area Quality Engineering representative is responsible for:
Reviewing Product/Technology QCI/TCI history and supplying quantitative data of acceptance history.
Contacting and obtaining approval from the responsible Product and Reliability Engineer.
Note: The Quality and Reliability engineers are typically members of the TRB board or use the TRB respective member as a resource.

3.5 The Marketing representative is responsible for obtaining the signature of the Intersil Contract Administrator, Marketing Manager, Quality Engineering and Customer Representative on the agreement to accept product prior to QCI/TCI test completion. Reference specification 999032 for forms.

3.6 The Marketing representative is responsible for providing Customer Engineering and the QML Coordinator with a copy of the completed form and customer agreement letter.

3.7 Product will be shipped as a specific Intersil Custom Specific drawing number "R4573" specification.

3.8 The QML representative is responsible for submitting the completed request from to the CORE TRB. Upon TRB review a copy of the information will be forwarded to the DLA office.

3.9 In the event of a QCI/TCI failure, the failure mode will be evaluated, the customer notified, and product jeopardy evaluated jointly by the customer and Intersil personnel as defined in 240111 for QCI/TCI failure disposition. Appropriate MRB disposition will be determined and the TRB notified. The QML representative is responsible for notifying the DLA office.