# Ordering Nomenclature

## INTERSIL NOMENCLATURE GUIDE

# Nomenclature Guide

## Intersil Nomenclatures

### ISL Types

**ISL X XXXX X I XX X XXX Z -T**

**PREFIX**

**FAMILY DESIGNATOR**
1: DSL, RTC, Clocks, ATE, Energy LED Lighting
2: Reference, DCPs, Buffers, Sensors, Precision Op Amp, Precision ADC & DAC
3: Interface, Data Communication
4: Analog Component Solutions
5: High Speed Amps, Switch/MUX, ADCs, DACs, Optical, Video, Telecom VoIP, DSP Function Specific
6: Desktop Power
7: Space, Auto
8: Analog Switches, General Purpose Power
9: Notebook, Handheld
A: High Speed ADCs

**PART NUMBER**
3 to 5 Digits

**OPTION**
E: 15kV ESD Protected
DCP Resistance Options
W: 10k
U: 50k
T: 100k

**TEMPERATURE RANGE**
C: 0°C to +70°C (Commercial)
D: 0°C to +85°C
H: -10°C to +100°C (Hi-Temp Comm.)
E: -20°C to +85°C (Extended Comm.)
I: -40°C to +85°C (Industrial)
A: -40°C to +105°C (Automotive)
F: -40°C to +125°C (Full-range Industrial)
P: -40°C to +130°C (Power Supply)
M: -55°C to +125°C (Military)
RHV: QML Class V (Radiation Hardened)
RHQ: QML Class Q (Radiation Hardened)
RHT: QML Class T (Radiation Hardened)
EHV: QML Class V (Radiation Hardened)
EHQ: QML Class Q (Radiation Hardened)
EHT: QML Class T (Radiation Hardened)

**PACKAGE DESIGNATOR**
A: Shrink Small Outline Plastic (SSOP/QSOP)
B: Small Outline Plastic (SOIC)
BE: Exposed Pad SOIC (EPSOIC)
C: Available
D: Ceramic Dual-In-Line Metal Seal (SBDIP)
E: Small Outline Transistor Plastic (SC-70)
F: Ceramic Flatpack
FE: Ceramic Flatpack w/Heatsink
G: Single In-line Plastic (SIP) TO-220
GS: Single In-line Plastic, Surface Mount (SIP) TO-263
H: Small Outline Transistor Plastic (SOT-23)
HT: Thin Small Outline Transistor Plastic (TSOT)
I: Chip Scale Package (CSP)
J: Ceramic Dual-In-Line Frit Seal (CERDIP)
K: Ball Grid Array (FBGA/PBGA/LGA)
KE: Heat Sink Ball Grid Array (HBGA)
KV: Very Thin Fine Pitch BGA (VFBGA)
L: Ceramic Leadless Chip Carrier (CLCC, SMD 0.5)
M: Plastic Leaded Chip Carrier (PLCC)
N: Thin Plastic Quad Flatpack (TQFP/LQFP)
NE: Thin Plastic Quad Flatpack (TQFP/LQFP w/Exposed Pad)
O: Do Not Use
P: Dual-In-Line Plastic (PDIP)
Q: Metric Plastic Quad Flatpack (MQFP/PQFP)
R: Quad/Dual Flat No Lead (QFN/DFN)/HDA (High Density Array)
RA: Array Flat No Lead (AFN)
RO: Optical Quad/Dual Flat No Lead (OQFN/ODFN)
ROM: Optical Quad/Dual Flat No Lead Module
RT: Thin Quad/Dual Flat No Lead (TQFN/TDFN)
RU: Ultra Thin Quad/Dual Flat No Lead (UTQFN/UTDFN/ePad UTQFN)
RS: Top Exposed Pad QFN (TEPQFN)
RX: Extreme Thin Flat No Lead (X2DFN/X2QFN)
S: Header (TO-257)
T: Metal Can (TO-39)
U: Mini Small Outline Package (MSOP)
UE: Thermally Enhanced Mini Small Outline Package (HMSOP)
UO: Optical Mini Small Outline Package (OSOP)
V: THIN Shrink Small Outline Plastic (TSSOP)
VE: Thermally Enhanced Thin Shrink Small Outline Plastic (HTSSOP/EPTSSOP)
W: Wafer Sale
WMB: Wafer Sale With Solderable Metal Backing Layer
XM: Die Sale , Military Visual (Condition B)
XC: Die Sale, Commercial Visual
XB: Die Sale, Bumped Die (FCP)
Y: Available
Z: Do Not Use

**OPTIONAL ELECTRICAL GRADE**
To Denote Speed or Precision Grading as Defined in Datasheet

**SPECIAL SELECTIONS**
Optional Characters to Denote Operating Conditions or Package Options:
18: 1.8V
33: 3.3V
EP: Enhanced Product (DSCC Vendor Item Drawing)
EPZ: Enhanced Product w/100% Matte Tin Lead Finish
A, B etc.: Firmware revision. This will not appear on part marking

**PB-FREE OPTION**
Z: ROHS and IEC61249-2-21 Halogen Free

**SUFFIX/ POST PROCESSING/ SPECIAL SERVICES**
-T: Tape and Reel
-T1: Tape and Reel
-T2: Tape and Reel w/Vacuum Pack
-T7: 7” Reel
-TS: 7” Reel, 100 pc.
-T7A: 7” Reel, 250pc.
-T13: 13” Reel
-T5: 500pc Tape and Reel
-TK: 1,000pc Tape and Reel
-T5K: 5,000pc Tape and Reel
-EV: Evaluation Board
-EVZ: Evaluation Board ROHS Compliant
-DM: Demo Board
-DMZ: Demo Board ROHS Compliant
-RF: Ref Design Eval Board
-RFZ: Ref Design Eval Board ROHS Compliant
-EC: Enhanced Commercial (Enhanced EOL, MIL-PRF-38535 Change Notice, Traceable to Wafer Lot)

# Nomenclature Guide

## EL Types

**EL 1503 A I R Z -T**

**EL** – **PREFIX**

**1503** – **PART NUMBER**

**A** – **OPTIONAL SUFFIX OR PART VARIATION**

**I** – **TEMPERATURE RANGE**

C: (Commercial) 0°C to +70°C
I: (Industrial) -40°C to +85°C
M: (Military) -55°C to +125°C
A: (Automotive) -40°C to +105°C
D: 0°C to +85°C
E: (Extended Comm) -20°C to +85°C

**R** – **PACKAGE FAMILY**

| PACKAGE TYPE | PACKAGE DESIGNATOR |
|---|---|
| Bare Die | D |
| CerDip | J |
| QFN/DFN<br>(Saw Singulate) | L |
| SO (0.300") and HSOP | M |
| PDIP | N |
| TSSOP (4.4 mm) | R |
| HTSSOP (4.4 mm) | RE |
| SO (0.150") | S |
| TO-220 | T |
| QSOP | U |
| SOT-23 | W |
| MSOP | Y |
| HMSOP | YE |
| TSOT | WT |
| SC-70 | C |

**Z** – **PB-FREE OPTION**

Z: Pb-Free Product

**-T** – **SUFFIX/POST PROCESSING/ SPECIAL SERVICES**

-T: Tape and Reel
-T7: 7" Reel
-T7A: 7" Reel (250 pcs)
-T13: 13" Reel

## X Types

### System Management Products (SMP)

**X 5 32 3 S8 I Z - 4.5A T1**

**PREFIX**
All Xicor Products

**INTERFACE**
4: 2-Wire Interface
5: SPI Interface

**EEPROM MEMORY SIZE**
00: 0kb
02: 2kb
04: 4kb
08: 8kb
16: 16kb
32: 32kb
64: 64kb
28: 128kb
56: 256kb

**RESET POLARITY**
0: Active High
1: Active Low
3: Active Low
4: Active High
5: Active High
7: Active High
8: Active Low
9: Active High

**PACKAGE DESIGNATOR**
P: PDIP
S: SOIC
V: TSSOP
M: MSOP
Q: QFN
#: Number of Pins

**TEMPERATURE RANGE**
(blank): Commercial 0°C to +70°C
I: Industrial -45°C to +85°C

**PB-FREE OPTION**
Z: Pb-Free Product
ZA: Pb-Free with Anneal

**VOLTAGE TRIP POINT**
2.7: 2.62V
2.7A: 2.85V or 2.92V
4.5A: 4.63V
(Blank): 4.38V or Other
A: Other
B: Other
C: Other

**TAPE AND REEL**
T1: Tape and Reel
T2: Dry Pack

**EXCEPTIONS TO RESET POLARITY**
X40015
X40231
X40233
X40035

**EXCEPTIONS TO EEPROM MEMORY SIZE**
X40626
X40030
X40031
X40034
X40035
X4C105

### Real Time Clocks (RTC)

**X XXXX S X I - 4.5A T1**

**PREFIX**

**PART NUMBER**

**PACKAGE DESIGNATOR**
S: SOIC
V: TSSOP

**# PINS**
8: 8 Ld
14: 14 Ld
16: 16 Ld

**TEMPERATURE RANGE**
(blank): Commercial 0°C to +70°C
I: Industrial -40°C to +85°C

**SPECIAL VOLTAGE SECTION**
Signifies Different V Trip Point
2.7
2.7A
4.5
4.5A

**TAPE AND REEL**
T1: Tape and Reel
T2: Dry Pack

# Nomenclature Guide

## Voltage References (VREFs)

**X 6 XXXX X I - X -XX T1**

**PREFIX**

**FAMILY DESIGNATOR**
Voltage References

**PART NUMBER**
4 Digits

**PERFORMANCE GRADE**
Refer to Datasheet for Details

**TEMPERATURE RANGE**
(blank): Commercial 0°C to +70°C
I: Industrial -40°C to +85°C

**PACKAGE DESIGNATOR**
G3: 3 Ld SOT23
S8: 8 Ld SOIC

**OUTPUT VOLTAGE**
-12: 1.25V
-25: 2.50V
-41: 4.096V
-50: 5.00V

**TAPE AND REEL**
T1: Tape and Reel
T2: Dry Pack

## Digitally Controlled Potentiometers (DCPs)

**X 9x XXX X XX X Z XX XX**

**PREFIX**

**FAMILY DESIGNATOR**
90 to 96, also 9C
NOTE: Does not include X952x, X9530, X9601x, and 90100

**PART NUMBER**
2 to 3 digits

**RESISTANCE OPTIONS**
W: 10k
U: 50k
T: 100k
Y: 2k
M: 2/10/10/50
Z: 1k

**PACKAGE DESIGNATOR** (followed by lead count)
B: CSP
M: MSOP
P: PDIP
S: SOIC
U: T/DFN
V: TSSOP

**TEMPERATURE RANGE**
Blank: Commercial (0°C to +70°C)
I: Industrial (-45°C to +85°C)

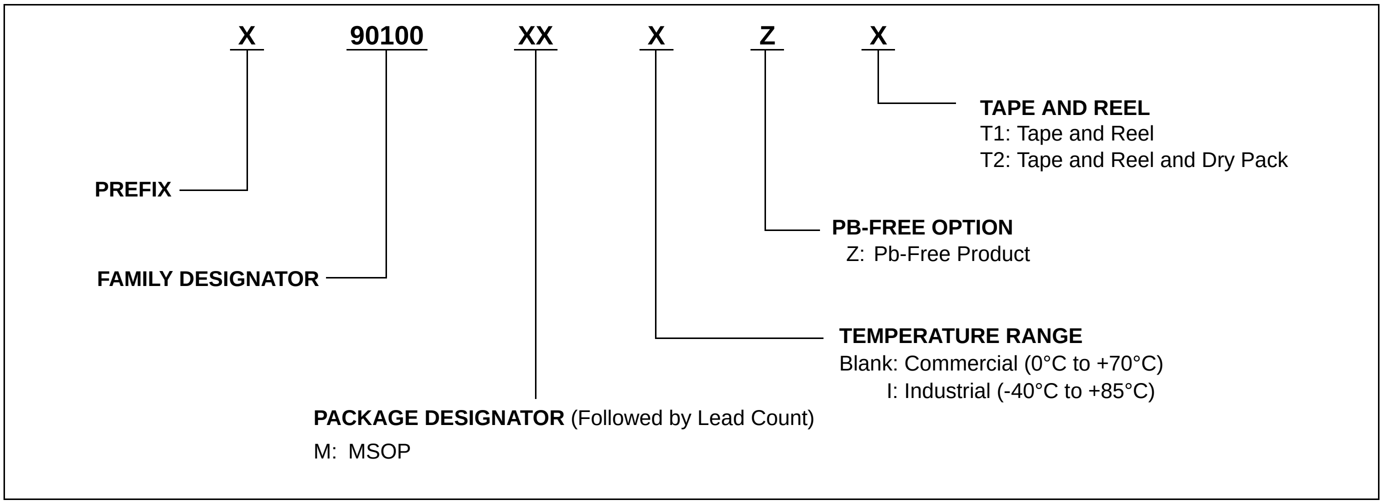
**PB-FREE OPTION**
Z: Pb-Free Product

**VOLTAGE IDENTIFIER**
Blank: 5V ±10%
-3: 3V ±10%
-2.7: 2.7V to 5.5V

**TAPE AND REEL**
T1: Tape and Reel
T2: Tape and Reel and Dry Pack

# Nomenclature Guide

## Digitally Controlled Capacitors (DCCs)



X 90100 XX X Z X

**PREFIX**

**FAMILY DESIGNATOR**

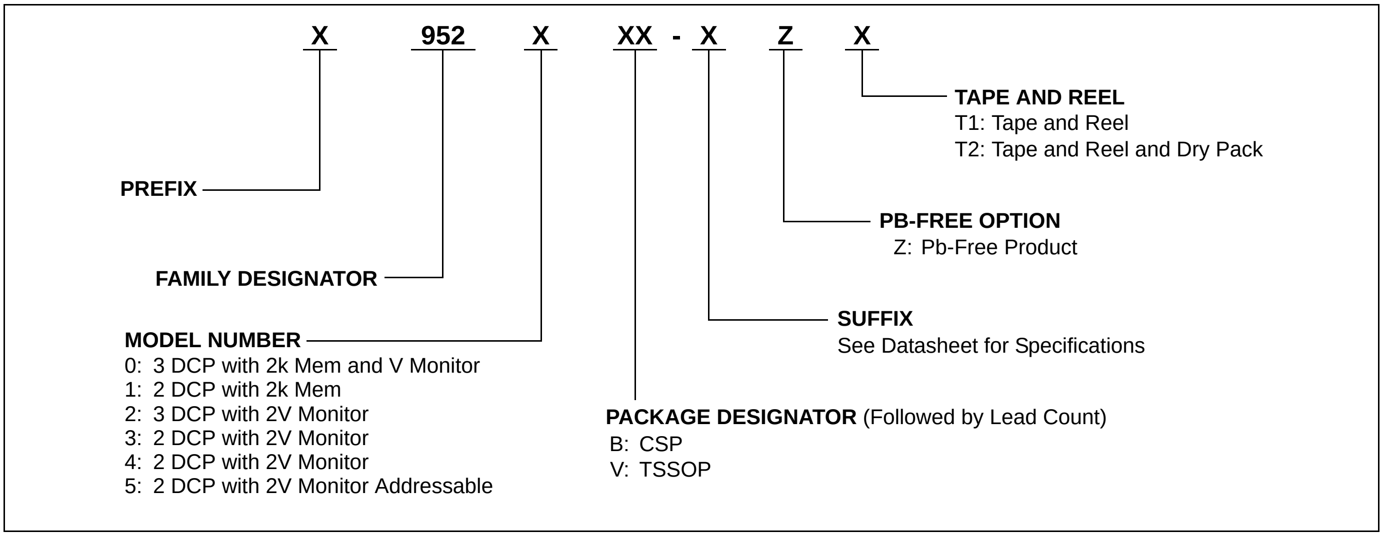
**PACKAGE DESIGNATOR** (Followed by Lead Count)
M: MSOP

**TEMPERATURE RANGE**
Blank: Commercial (0°C to +70°C)
I: Industrial (-40°C to +85°C)

**PB-FREE OPTION**
Z: Pb-Free Product

**TAPE AND REEL**
T1: Tape and Reel
T2: Tape and Reel and Dry Pack

## Bias and Control for Laser Diode with Integrated DCP



X 952 X XX - X Z X

**PREFIX**

**FAMILY DESIGNATOR**

**MODEL NUMBER**
0: 3 DCP with 2k Mem and V Monitor
1: 2 DCP with 2k Mem
2: 3 DCP with 2V Monitor
3: 2 DCP with 2V Monitor
4: 2 DCP with 2V Monitor
5: 2 DCP with 2V Monitor Addressable

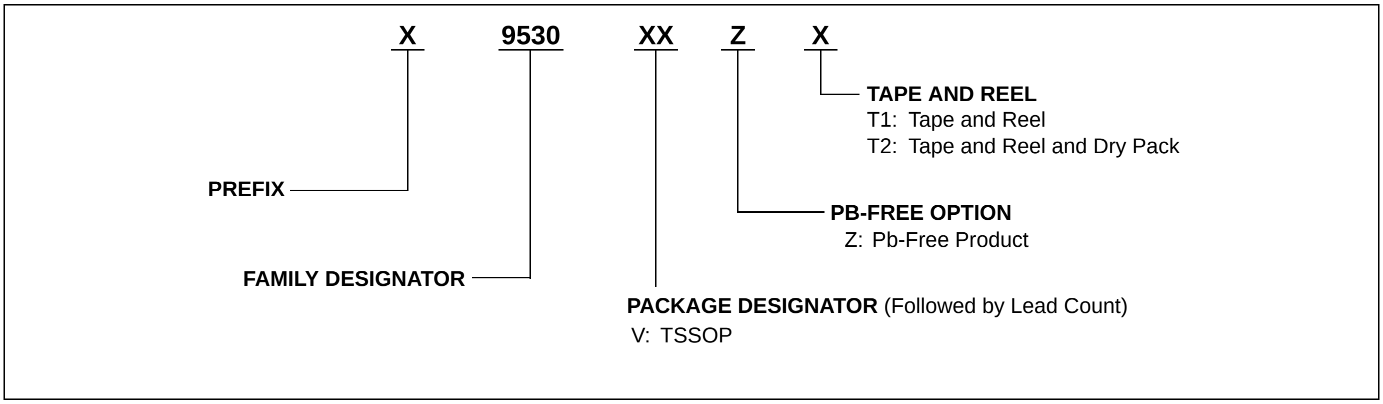
**PACKAGE DESIGNATOR** (Followed by Lead Count)
B: CSP
V: TSSOP

**SUFFIX**
See Datasheet for Specifications

**PB-FREE OPTION**
Z: Pb-Free Product

**TAPE AND REEL**
T1: Tape and Reel
T2: Tape and Reel and Dry Pack

## Bias and Control for Laser Diode



X 9530 XX Z X

**PREFIX**

**FAMILY DESIGNATOR**

**PACKAGE DESIGNATOR** (Followed by Lead Count)
V: TSSOP

**PB-FREE OPTION**
Z: Pb-Free Product

**TAPE AND REEL**
T1: Tape and Reel
T2: Tape and Reel and Dry Pack

# Nomenclature Guide

## General Purpose Sensor Conditioners with Look-Up Table Memory

**X 9601 X XX Z X**

**PREFIX**

**FAMILY DESIGNATOR**

**SENSOR OPTION**
1: Sensor Conditioner with Dual Look Up Table Memory and DAC
2: Temperature Sensor with Look Up Table Memory and DAC
3: Universal Sensor Conditioner with Dual Look Up Table Memory and DACs

**PACKAGE DESIGNATOR** (Followed by Lead Count)
B: CSP
V: TSSOP

**PB-FREE OPTION**
Z: Pb-Free Product

**TAPE AND REEL**
T1: Tape and Reel
T2: Tape and Reel and Dry Pack

## Parallel E$^2$PROM

**X XXXX X XX -XX T1**

**PREFIX**

**PART NUMBER**

**PACKAGE DESIGNATOR**
D: Cerdip
E: Ceramic LCC
F: Flatpack
H: Ceramic SOIC
J: PLCC
K: Pin Grid Array
L: TQFP
N: Stretched Ceramic LCC
P: Plastic DIP
S: SOIC
T: TSOP

**TEMPERATURE RANGE**
Blank: Commercial (0°C to +70°C)
I: Industrial (-40°C to +85°C)
M: Military = -55°C to +125°C
MB: MIL-STD-883
MHR: Military High Rel

**ACCESS TIME**
Blank: 300ns
-25: 250ns
-20: 200ns
-15: 150ns
-90: 90ns
-70: 70ns
-55: 55ns
-45: 45ns

**TAPE AND REEL**
T1: Tape and Reel

## Serial E$^2$PROM

**X XXXX XX XX -XX T1**

**PREFIX**

**PART NUMBER**

**PACKAGE DESIGNATOR**
A: 8 Ld SOIC (EIAJ)
D: CERDIP
P: Plastic DIP
S: SOIC
S8: 8 Ld SOIC
S14: 14 Ld SOIC
V: TSSOP

**TEMPERATURE RANGE**
Blank: Commercial (0°C to +70°C)
I: Industrial (-40°C to +85°C)
M: Military = -55°C to +125°C
MB: MIL-STD-883

**$V_{CC}$ RANGE**
Blank: 4.5V to 5.5V
-3: 3V to 5.5V
-2.7: 2.7V to 5.5V

**SPECIAL REQUIREMENT**
**TAPE AND REEL**
T1: Tape and Reel

# Nomenclature Guide

## ZL Types

**ZL BBBBB P T S L F -CC**

**ZL = ZILKER LABS DESIGNATOR**

**BASE PART NUMBER**
5 Character Max.

**PACKAGE DESIGNATOR**
A: (QFN)

**OPERATING TEMPERATURE RANGE**
J: (0°C to +85°C)
K: (0 to +70°C)
L: (-40°C to +85°C)
Z: (-55°C to +125°C)

**FIRMWARE REVISION**
Any alphanumeric character

**LEAD FINISH**
F (Lead-free Matte Tin)
N (Lead-free NiPdAu)

**SHIPPING OPTION**
J: (Trays)
T1 or TK: (Tape and Reel - 1000 piece)
T3: (Tape and Reel - 3000 piece)
T4: (Tape and Reel - 4000 piece)
T5: (Tape and Reel - 5000 piece)
T6: (Tape and Reel - 6000 piece)
T: (Tape and Reel - 100 piece for Zilker legacy products)
T: (Tape and Reel - Full reel Qty. for Intersil Zilker products)
W: (Waffle pack)

**CUSTOM CODE**
Any alphanumeric character

## ZL Power Modules

**ZL 9XXXM* I R Z -T**

**ZL = ZILKER LABS DESIGNATOR**

**BASE PART NUMBER**
6 Character Max.
ZL90XXM* - Power Modules
ZL91XXM* - Power Modules
ZLS4XXX - Module Component

*An alpha character succeeding the “M” represents a Firmware or Configuration change and will not appear on part marking

**OPERATING TEMPERATURE RANGE**
I: -40°C to +85°C

**PACKAGE DESIGNATOR**
R: QFN

**ROHS**
Z: ROHS Compliant

**SHIPPING OPTION**
No Suffix Trays
-T: Tape and Reel Full Reel Qty.
-TK: Tape and Reel 1000 pc.

## ZL Evaluation Boards

**ZL BBBBB EV S R -CC**

**ZL = ZILKER LABS DESIGNATOR**

**BASE PART NUMBER**
5 Character Max.

**EVALUATION BOARD DESIGNATOR**
EV = Evaluation Board

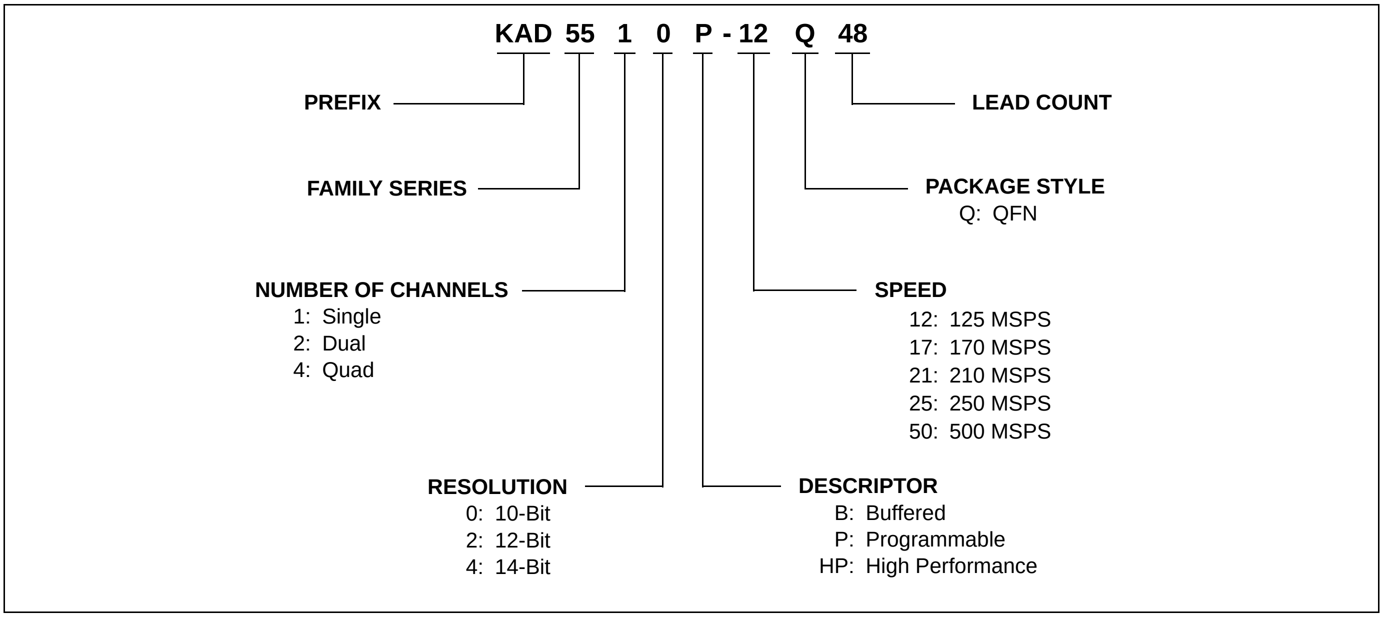
**KIT OPTION**
K = Kit containing collateral
Blank = Board only

**BOARD VARIATION**
Any number

**CUSTOM CODE**
Any alphanumeric character

# Nomenclature Guide

## KAD Types



**KAD 55 1 0 P - 12 Q 48**

**PREFIX**

**FAMILY SERIES**

**NUMBER OF CHANNELS**
1: Single
2: Dual
4: Quad

**RESOLUTION**
0: 10-Bit
2: 12-Bit
4: 14-Bit

**LEAD COUNT**

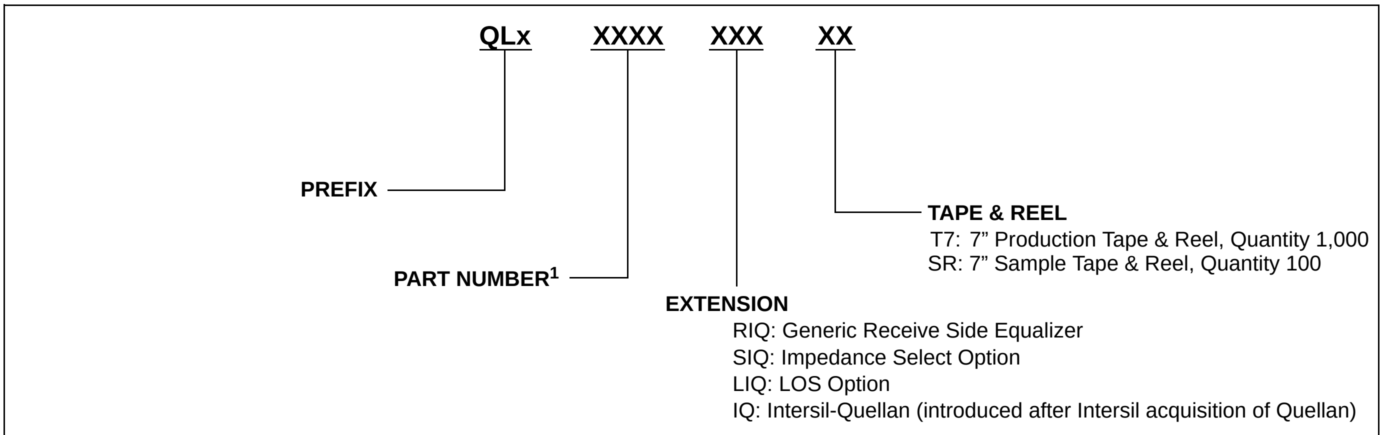
**PACKAGE STYLE**
Q: QFN

**SPEED**
12: 125 MSPS
17: 170 MSPS
21: 210 MSPS
25: 250 MSPS
50: 500 MSPS

**DESCRIPTOR**
B: Buffered
P: Programmable
HP: High Performance

## QLx Types

### Wired Signal Integrity Parts



**QLx XXXX XXX XX**

**PREFIX**

**PART NUMBER**[1]

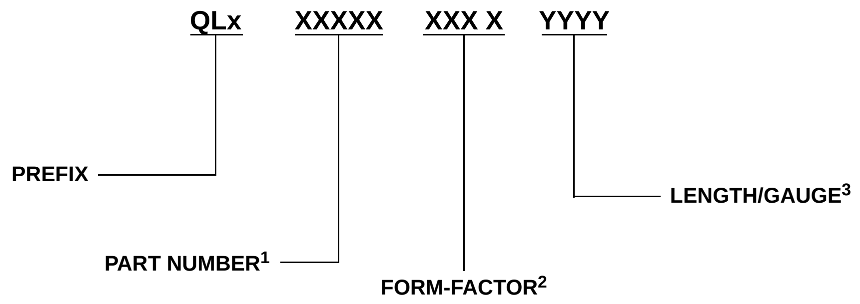
**TAPE & REEL**
T7: 7” Production Tape & Reel, Quantity 1,000
SR: 7” Sample Tape & Reel, Quantity 100

**EXTENSION**
RIQ: Generic Receive Side Equalizer
SIQ: Impedance Select Option
LIQ: LOS Option
IQ: Intersil-Quellan (introduced after Intersil acquisition of Quellan)

NOTE:

1. Usually Number of Channels + Data rate, e.g. 4600: Quad 6G; 411G: Quad 11G.

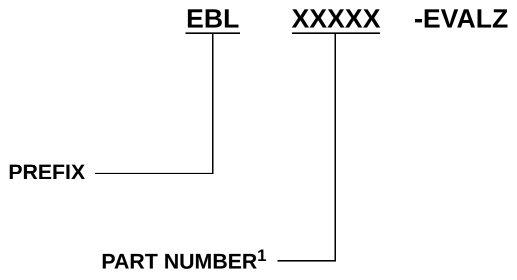
### Active Cables



NOTES:

1. Data Rate followed by Special Designator, followed by Customer Designator (if applicable), followed by “C” for cable.
   Special Designators:
   0 for half-active (chip on RX side only)
   1 for generic full-active (chips on both TX and RX ends)
   2 for full-active Ethernet
   Customer Designator:
   0 for general market, other numbers for specific customers, e.g. 600C (6G half-active cable), 4000C (40G half-active cable), 4100C (40G full-active cable)
2. For example, connector type or form-factor: SFP for SFP+, QSFP for QSFP, MSAS for Mini-SAS, SDP for mini DisplayPort, SDP for Standard DisplayPort, SMDP for mini-to-standard DisplayPort.
3. For example, 1028 = 10m 28 AWG.

## QL Evaluation Boards

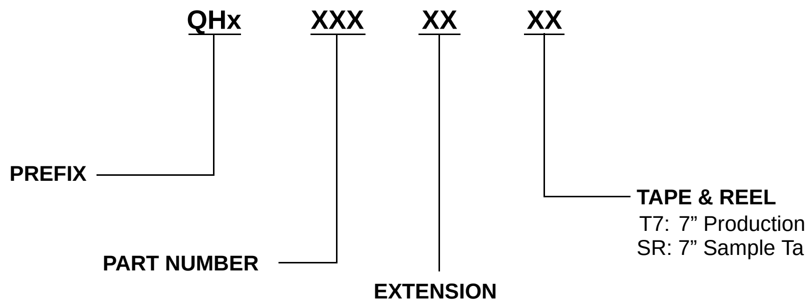


NOTE:

1. Same as the part marking on the respective IC.

## QHx Types

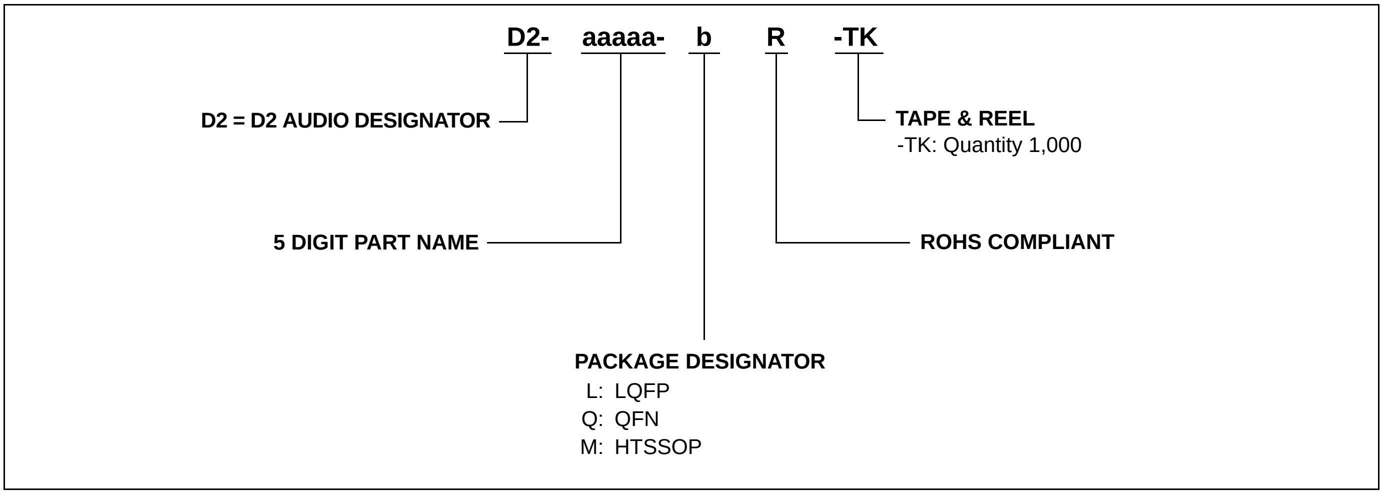
### Wireless Noise Cancellation Parts



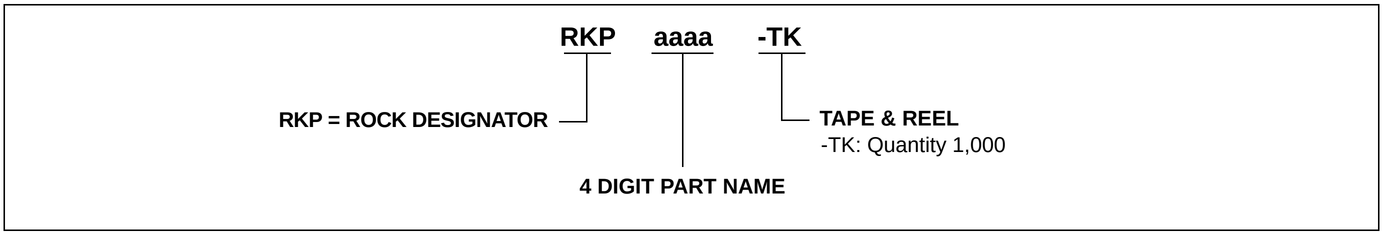
**TAPE & REEL**
T7: 7” Production Tape & Reel, Quantity 1,000
SR: 7” Sample Tape & Reel, Quantity 100

**EXTENSION**
IQ: Intersil-Quellan (introduced after Intersil acquisition of Quellan)

## D2 Types



## RKP Types



## TW Types

**TW aaaa bb - c d e f g# - h j k l**

**PREFIX**

**DEVICE NUMBER**

AT: Auto Wafer
EP: Epi Wafer

**c - PROCESS**

This character is included in the marking of legacy products only.

| PROCESS | CODE |
|---|---|
| TSMC, 0.35µm, Polycide, SPQM or SPTM Logic | A |
| TSMC, 0.25µm | B |
| X-FAB, 0.25µm | C |
| TSMC, 0.18µm | D |
| X-FAB, 0.18µm | E |
| TSMC, 0.18µm, EPI, Ar Anneal, Hi | G |
| Goyatek/Vanguard, 0.25µm | H |
| TSMC 0.25µm EPI, Ar Anneal, Hi | J |
| TSMC 0.18µm Automotive Process | K |
| TSMC 0.13µm | M |
| TSMC 90nm | N |
| Fujitsu 90nm | P |
| TSMC 0.13µm 12” Wafer | Q |
| TSMC 65nm | R |
| TSMC 45nm | S |

**d - ASSEMBLY VENDOR**

This character is included in the marking of legacy products only.

| ASSEMBLY VENDOR | CODE |
|---|---|
| ASEK | A |
| ASECL | B |
| GAPT | C |
| i2a/IPAC, Quick Pak | D |
| SPIL | E |
| ChipMOS | G |
| UTAC | J |
| Fujitsu | K |
| Amkor Korea | M |

**e -**

Q: 12” Wafer

**f - PACKAGE TYPE A**

| PACKAGE TYPE | CODE |
|---|---|
| BGA package | B |
| LQFP package | L |
| PQFP package | P |
| TQFP package | T |
| QFN package | N |
| PQFP package with Exposed Heat Spreader | E |

**g# - DIE REVISION**

It starts from A1. If full layers are changed, the die revision changes like A1→B1→C1, etc.

If some layers are changed, the die revision changes like A1→A2→A3, etc.

**h - PACKAGE TYPE B**

| PACKAGE TYPE | CODE |
|---|---|
| Green (Halogen Free) and Lead Free package | G (Note) |
| Normal package | N |
| Green (Halogen Free) and Lead Free package with Cu Bond Wires | C |
| Flip Chip | F |

NOTE: The following FG’s also use Cu wire:
TW6815-LA1-GR
TW6816-LA1-GR
TW6817-LA1-GR
TW6818-LA1-GR
TW6932-LA1-GR

**j - PACKAGE TYPE C**

| PACKAGE TYPE | CODE |
|---|---|
| Drop-in heat spreader | D |
| Exposed heat spreader | E |
| Regular package without heat spreader | R |

**k - PACKAGE VARIANT**

| PACKAGE VARIANT | CODE |
|---|---|
| This is only used when one product type is offered in 2 different sizes or lead counts of the same package style. The last FG# created will include the lead count. | 128 (lead count) |

**l - OPTIONS**

S = SLT
B = Burn-in
H = High Temp. Testing
I = Industrial
V = High Volt Testing
T = Tape & Reel Packing

## Intersil Legacy Nomenclatures

### 5962 SMD/DSCC - QML Types

**5962 - XXXXX 0X X X X**

**SMD ID NUMBER**
(Does Not Change) (ID Not Applicable in Earlier DSCC Items)

**TOTAL DOSE DESIGNATOR**
-: Non-Rad Hard
M: 3 krad (Si)
D: 10 krad (Si)
R: 100 krad (Si)
F: 300 krad (Si)

**DRAWING NUMBER**
(DSCC and SMD)

**DEVICE TYPE**
(Paragraph 1.2.1 Of SMD/DSCC Drawing)

**DEVICE CLASS DESIGNATOR**
(If Applicable)
Q: QML Class Q (MIL-PRF-38535)
M: QML Class B (MIL-STD-883)
V: QML Class V, (MIL-PRF-38535)
N: Non-Traditional Packages and Temp Ranges (i.e., Plastic Packages, -40°C to +85°C Temperature Range)
T: QML Class T, Star*Lite Flow

**CASE OUTLINE**
Case Outlines are Listed in the Specific SMD and Detailed in MIL-STD-1835, Section 4.

**LEAD FINISH**
A: Solder Dip
C: Gold

NOTE: Nomenclature Per MIL-PRF-38535

### 80C, 82CXXX Types

**M D 80C86 - 2 /B Z**

**TEMPERATURE RANGE**
C: 0°C to +70°C
I: -40°C to +85°C
M: -55°C to +125°C

**PACKAGE DESIGNATOR**
P: Dual-In-Line Plastic (PDIP)
D: Ceramic Dual-In-Line Frit-Seal (CERDIP)
or Ceramic Dual-In-Line Metal Seal (SBDIP)
G: Ceramic Pin Grid Array (CPGA)
R: Ceramic Leadless Chip Carrier (CLCC)
S: Plastic Leaded Chip Carrier (PLCC)
M: Small Outline Plastic (SOIC)
MS: OKI Pin for Pin Cross (PLCC)
MQ: OKI Pin for Pin Cross (MQFP)

**PART NUMBER**
80CXXX: CMOS Microprocessors
82CXXX: CMOS Peripherals

**SPEED DESIGNATION**

| Peripherals | µProcessors |
|---|---|
| -5: 5MHz | Blank: 5MHz |
| Blank: 8MHz | -2: 8MHz |
| -10: 10MHz | -10: 10MHz |
| -12: 12MHz | -12: 12MHz |
|  | -20: 20MHz |
|  | -25: 25MHz |

**SUFFIX**
/B: -55°C to +125°C with Burn-In
/883: Current Rev Compliant
/7: Thin EPI, Current Rev 883 Compliant

**PB-FREE OPTION**
Z: Pb-Free Product
ZA: Pb-Free with Anneal

# Nomenclature Guide

## ACS, ACTS, HCS, HCTS Radiation Hardened Types

**ACSXXX D MS R**

**PART NUMBER**
ACS, HCS: CMOS Compatible
ACTS, HCTS: TTL Compatible

**PACKAGE DESIGNATOR**
D: Ceramic Dual-In-Line Metal-Seal (SBDIP)
H: Die
K: Ceramic Flatpack

**CLASS**
MS: Class V (Note 1)
T: QML Class T, Star*Lite Flow

**HARDNESS ASSURANCE LEVEL**
R: 200 krad(Si) HCS/HCTS
F: 300 krad(Si) ACS/ACTS

NOTE:

2. FLIGHT UNITS MUST BE ORDERED BY SMD#.
A cross reference table is available on the Intersil website at www.intersil.com

## AD Types

**ADC0803LC WM -T**

**PART NUMBER**
Converters
AD, ADC

**PACKAGE DESIGNATOR**
D: Ceramic Dual-In-Line Frit-Seal (CERDIP) or Ceramic Dual-In-Line Metal Seal (SBDIP)
H: TO-52 Can
N: Dual-In-Line Plastic (PDIP)
WM: Small Outline Plastic (SOIC)

**SUFFIX**
-T: Tape and Reel

## CA Types

**CA3260 A T Z 3**

**PART NUMBER**
CAXXXX

**ELECTRICAL OPTIONS**
A, B, C, Blank

**PACKAGE DESIGNATOR**
D: Ceramic Dual-In-Line Metal-Seal (SBDIP)
E: Dual-In-Line Plastic (PDIP)
F: Ceramic Dual-In-Line Frit-Seal (CERDIP)
J: Ceramic Leadless Chip Carrier (CLCC)
M: Small Outline Plastic (SOIC)
Q: Plastic Leaded Chip Carrier (PLCC)
S: DIL Formed TO-5
T: Can
Z: Single-In-Line Plastic (SIP)
Blank: Refer to Data Sheet for Package Type

**SUFFIX**
3: -55°C to +125°C Modified Class B
3W: Modified Class B without High & Low Temperature DC
96: Tape and Reel

**PB-FREE OPTION**
Z: Pb-Free Product
ZA: Pb-Free with Anneal

NOTE: If the part number contains three digits, add a leading zero when ordering. Example: CA555 becomes CA0555.

## CD22XXX Types

**CD22 XXXXX A E X**

**PREFIX DESIGNATION** for Intersil Telecom IC's

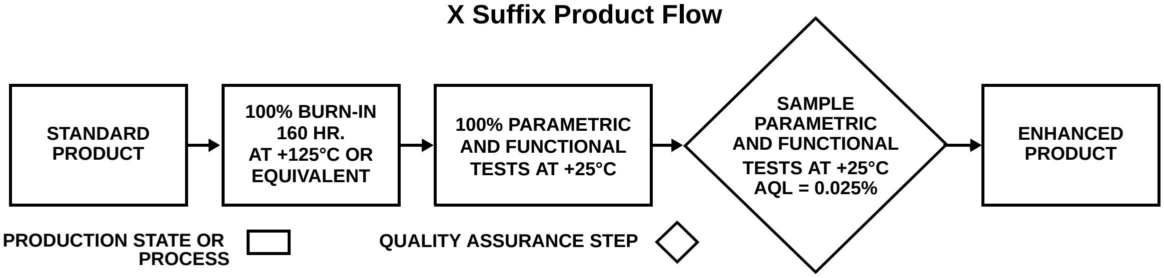
**PART NUMBER**

**REVISION**
A: 1st
B: 2nd etc.

**PACKAGE DESIGNATOR**
D: Ceramic Dual-In-Line Metal-Seal (SBDIP)
E: Dual-In-Line Plastic (PDIP)
F: Ceramic Dual-In-Line Frit-Seal (CERDIP)
M: Small Outline Plastic (SOIC)
Q: Plastic Leaded Chip Carrier (PLCC)
H: Chip

**SCREENING OPTION**
X: Enhanced Product Screening i.e., Burn-In
(Optional for D, E Package Types)

### X Suffix Product Flow



## CD4000 Radiation Hardened Types

**CD4000 B D MS R**

**PART NUMBER**
CD4000

**SERIES**
B: Buffered
UB: Un-Buffered

**PACKAGE DESIGNATOR**
D: Ceramic Dual-In-Line Metal-Seal (SBDIP)
H: Die
K: Ceramic Flatpack

**CLASS**
MS: Class V (Note 1)
NS: Class V with Neutron Irradiation (Note 1)
T: Class T, Star*Lite Flow

**HARDNESS ASSURANCE LEVEL**
R: 100 krad(Si)

NOTE:

1. FLIGHT UNITS MUST BE ORDERED BY SMD#.
A cross reference table is available on the Intersil website at http://www.intersil.com

## CDP Types

**CDP1802 A C D 3**

**PART NUMBER** (CMOS LSI)
CDP18XX

**REVISION**
A: 1st
B: 2nd

**VOLTAGE**
C: 5V Device

**PRODUCT ASSURANCE LEVEL**
X: -40°C to +85°C with Burn-In
3: Non-Compliant with MIL-STD-883

**PACKAGE DESIGNATOR**
D: Ceramic Dual-In-Line Metal-Seal (SBDIP)
E: Dual-In-Line Plastic (PDIP)
K: Ceramic Flatpack
Q or N: Plastic Leaded Chip Carrier (PLCC)

## CDP68HC68 Types

**CDP68HC68 T1 M**

**PART NUMBER** (Peripherals)
HC: Standard

**FAMILY SERIES**
A2, P1, R1, S1, T1, W1

**PACKAGE DESIGNATOR**
E: Dual-In-Line Plastic (PDIP)
M: Small Outline Plastic (SOIC)
H: Chip

## CDP65C51 Types

**CDP65C51 A E 4**

**PART NUMBER** (Peripherals)

**FAMILY SERIES**
A: Non-Standard Clear to Send (CTS) Operation
Blank: Standard Clear to Send (CTS) Operation

**PACKAGE DESIGNATOR**
E: Dual-In-Line Plastic (PDIP)
M: Small Outline Plastic (SOIC)
H: Chip
SM: Shrink Small Outline Plastic (SSOP)

**SPEED OPTIONS**
1: 1MHz Operation
2: 2MHz Operation
4: 4MHz Operation

## CD74HC Types

**CD74 HC22106 E**

**PREFIX DESIGNATION**

**PART NUMBER**

**PACKAGE DESIGNATOR**
E: Dual-In-Line Plastic (PDIP)

## DG Types

**DG XXXX X X Z /883**

**DEVICE FAMILY PREFIX**
Switches and MUXs

**PART NUMBER**

**TEMPERATURE RANGE**
A: -55°C to +125°C
B: -25°C to +85°C
C: 0°C to +70°C
D: -40°C to +85°C

**PACKAGE DESIGNATOR**
A: Can
J: Dual-In-Line Plastic (PDIP)
K: Ceramic Dual-In-Line Frit-Seal (CERDIP)
N: PLCC
P: Ceramic Dual-In-Line Metal Seal (SBDIP)
V: Thin Shrink Small Outline Plastic (TSSOP)
Y: Small Outline Plastic (SOIC)
Y-T: Tape and Reel

**PB-FREE OPTION**
Z: Pb-Free Product
ZA: Pb-Free with Anneal

**HIGH RELIABILITY DESIGNATOR**
/883: Fully Compliant to MIL-STD-883 Class B/QML
/883B

# Nomenclature Guide

## HX Types

**H A 1 - 5134 A -2 Z 96**

**PREFIX**

**FAMILY**
A: Analog
C: Communications
D: Digital
I: Interface
M: Memory
V: Analog High Voltage

**PACKAGE DESIGNATOR**
1: Ceramic Dual-In-Line Frit-Seal (CERDIP)
1B: Ceramic Dual-In-Line Metal-Seal (SBDIP)
2: Can
3: Dual-In-Line Plastic (PDIP)
4: Ceramic Leadless Chip Carriers (CLCC)
4P: Plastic Leaded Chip Carrier (PLCC)
6: Narrow Dual-In-Line Plastic (PDIP) or Ceramic Dual-In-Line Frit-Seal (CERDIP)
7: 8 Lead Ceramic Dual-In-Line Frit-Seal (CERDIP)
9P: Small Outline Plastic (SOIC)
0: Chip

NOTE: If the package designator is 2 characters the hyphen is omitted from the part number.

**PART NUMBER**

**PERFORMANCE GRADE**
A, B: High Performance
C: Relaxed Specification
S: Very High Speed

NOTE: Applies to HA, HD and HM products only.

**TEMPERATURE RANGE**
-2: -55°C to +125°C
-4: -25°C to +85°C
-5: 0°C to +75°C
-6: +25°C Chip Probe
-7: Dash-7 High Reliability Commercial Product 0°C to +75°C, Includes 96 hour Burn-In
-8: -55°C to +125°C Intersil Class B Equivalent Devices for use in Military and Flight Systems
-9: -40°C to +85°C
/883: Fully Compliant to MIL-STD-883, Class B/QML
BXXXX: Customer Specific Screening
RXXXX: Customer Specific Screening
SXXXX: Customer Specific Screening

**SUFFIX**
96: Tape and Reel Option for SOIC, PLCC
X96: Tape and Reel Option for SOIC, PLCC
EVAL: Evaluation Platform

**PB-FREE OPTION**
Z: Pb-Free Product
ZA: Pb-Free with Anneal

## HX, HXX Types

**H A 4314B C B Z 96**

**PREFIX**

**FAMILY**
A: Analog
C: Communications
FA: Ultra-High Frequency Analog
I: Data Acquisition, DSP Function-Specific
V: Analog High Voltage

**PART NUMBER**

**TEMPERATURE RANGE**
C: 0°C to +70°C
I: -40°C to +85°C
M: -55°C to +125°C

**PACKAGE DESIGNATOR**
A: Shrink Small Outline Plastic (SSOP)
B: Small Outline Plastic (SOIC)
D: Ceramic Dual-In-Line Metal-Seal (SBDIP)
H: Plastic Small Outline Transistor (SOT)
J: Ceramic Dual-In-Line Frit-Seal (CERDIP)
L: Ceramic Leadless Chip Carrier (CLCC)
M: Plastic Leaded Chip Carrier (PLCC)
N: Thin Quad Flatpack (TQFP), or Metric Quad Flatpack (MQFP)
Q: Metric Plastic Quad Flatpack (MQFP), or Plastic Quad Flatpack (PQFP)
P: Dual-In-Line Plastic (PDIP)
T: Can
Y: Chip (Commercial Visual)
W: Wafer

**SUFFIX**
/883: Fully Compliant to MIL-STD-883 Class B/QML
96: Tape and Reel
-T: Tape and Reel
EVAL: Evaluation Platforms

**PB-FREE OPTION**
Z: Pb-Free Product
ZA: Pb-Free with Anneal

## HCS, HCTS, ACS, ACTS, Radiation Hardened Types

**HCSXXX D MS R**

**PART NUMBER**
ACS, HCS: CMOS Compatible
ACTS, HCTS: TTL Compatible

**PACKAGE DESIGNATOR**
D: Ceramic Dual-In-Line Metal-Seal (SBDIP)
H: Die
K: Ceramic Flatpack

**CLASS**
MS: Class V (Note 1)
T: Class T, Star*Lite Flow

**HARDNESS ASSURANCE LEVEL**
R: 200 krad(Si) HCS/HCTS
F: 300 krad(Si) ACS/ACTS

NOTE:

1. FLIGHT UNITS MUST BE ORDERED BY SMD#.
   A Cross Reference Table is Available on the intersil Website at http://www.intersil.com/

## HIN Types

**HIN XXX X X X Z - T**

**DEVICE FAMILY PREFIX**
Interface

**PART NUMBER**

**A:** High Speed
**E:** 15kV ESD Protected

**TEMPERATURE RANGE**
C: Commercial (0°C to +70°C)
I: Industrial (-40°C to +85°C)

**PACKAGE DESIGNATOR**
A: Shrink Small Outline (SSOP)
B: 300 mil Small Outline Plastic (SOIC)
BN: 150 mil Small Outline Plastic (SOIC)
P: Dual-In-Line Plastic (PDIP)
Y: Die
J: Dual-in-Line Ceramic (CDIP)
N: Metric Quad Flat Package (MQFP)

**PB-FREE OPTION**
Z: Pb-Free Product
ZA: Pb-Free with Anneal

**TAPE AND REEL**

## HIP Types

**H I P 4082 I B * Z T**

**PREFIX**

**FAMILY**
IP: Intelligent Power
V: High Voltage

**FUNCTION CODE**
00XX: Low Side Switches
10XX-XX: 00 to 29 Hot Plug
-XX: 30 to 99 High Side Switches
206X: Integrated MOSFETs
21XX-XX: 00 to 19 Half Bridges
40XX: Full or Three Phase Bridges
50XX: Integrated Controllers
60XX: PWM Controllers
62XX: ICs for Portable Applications
63XX: Multiphase Buck PWM Controllers
65XX: ACPI Controllers
66XX: Synchronous-Rectified Buck MOSFET Drivers
72XX: Automotive Communication (J1850)
9XXX: Special Function
(X: Sequential numbers assigned by design)

**TEMPERATURE RANGE**
A: Automotive (-40°C to +105°C)
C: Commercial (0°C to +70°C)
I: Industrial (-40°C to +85°C)
M: Military (-55°C to +125°C)
D: EDP (0°C to +85°C)
F: Full-Range Industrial (-40°c to +125°C)

**PACKAGE DESIGNATOR**
B: Small Outline Plastic (SOIC)
D: Chip
K: SOT-23
M: Plastic Leaded Chip Carrier (PLCC)
P: Dual-In-Line Plastic (PDIP)
Q: Metric Plastic Quad Flatpack (MQFP)
S: Single-In-Line Plastic (SIP)
V: TSSOP
W: Wafer
Y: Die
RT: Thin Quad/Dual Flat No Lead (TQFN/TDFN

**SPECIAL SELECTIONS**
Optional characters to denote operating conditions, voltage selections defined in datasheet

**PB-FREE OPTION**
Z: Pb-Free Product

**PACKING DESIGNATOR**
T: Tape and Reel (If Available)
(See Note)

NOTE: Suffix EVAL: Evaluation Kit (Available for some products).

# Nomenclature Guide

## HMP Types

**H MP 8117 A C N**

**PREFIX**

**FAMILY**
MP: Multimedia Products

**PART NUMBER**

**REVISION**
If Applicable

**TEMPERATURE RANGE**
C: Commercial, 0°C to +70°C

**PACKAGE DESIGNATOR**
N: Metric Plastic Quad Flatpack (PQFP)

NOTE: PQFP is also known as QFP and MQFP.

## HMU/HMA Types

**H MU 16 J C - 35 /883**

**PREFIX**

**FAMILY**
MU: Multiplier
MA: Multiplier/Accumulator

**DEVICE TYPE**
16, 17, 510

**PACKAGE DESIGNATOR**
J: Plastic Leaded Chip Carrier (PLCC)
G: Ceramic Pin Grid Array (CPGA)

**TEMPERATURE RANGE**
C: Commercial, 0°C to +70°C
I: Industrial, -40°C to +85°C
M: Military, -55°C to +125°C

**PERFORMANCE GRADE**

| | | | |
|---|---|---|---|
| -35: | 35ns | -60: | 60ns |
| -45: | 45ns | -65: | 65ns |
| -55: | 55ns | -75: | 75ns |

**HIGH RELIABILITY DESIGNATOR**
883: -55°C to +125°C Fully Compliant to MIL-STD-883, Class B/QML

## HS/IS Radiation Hardened Types

**H S 1 - 6664 RH -8**

**PREFIX**
H: Harris
I: Intersil

**FAMILY**
Rad Hard/High-Rel Products

**PACKAGE DESIGNATOR**
1: Ceramic Dual-In-Line Frit-Seal (CERDIP) or Ceramic Dual-In-Line Metal-Seal (SBDIP)
2: Can
4: Ceramic Leadless Chip Carriers (CLCC)
7B: 8 Lead Ceramic Dual-In-Line Side-Brazed (SBDIP)
8: Ceramic Pin Grid Array (CPGA)
9: Ceramic Flatpack
0: Die
YE: SMD 0.5
9S: TO-257 Hermetic Surface Mount

**PART NUMBER**

**HARDNESS**
RH: Radiation Hardened (Note 3)
EH: Radiation Hardened (Note 3)

**CLASS**
-8: -55°C to +125°C QML SMD Class Q (Note 1)
-Q: -55°C to +125°C QML SMD Class V (Note 1)
-T: -55°C to +125°C QML SMD Class T (Note 1)
/PROTO: -55°C to +125°C Temperature Tested (Note 2)

NOTES:

1. FLIGHT UNITS MUST BE ORDERED BY SMD#. A cross reference table is available on the Intersil website at http://www.intersil.com/
2. /PROTO available for design-in/breadboarding - NOT FOR FLIGHT.
3. Refer to specific device type SMD for radiation hardness level.

## HSP Types

**H SP XXXXX A J C - XX /883**

**PREFIX**

**FAMILY**
SP: Signal Processing,
DSP Function-Specific

**DEVICE TYPE**
43XXX: Digital Filters
45XXX: Signal Synthesis/Special Function
48XXX: Image Processing
95XX: Building Blocks
50XXX: Freq. Conversion and Modulation/Demodulation

**MASK REVISION**

**PACKAGE DESIGNATOR**
D: Die
G: Ceramic Pin Grid Array (CPGA)
J: Plastic Leaded Chip Carrier (PLCC)
P: Dual-In-Line Plastic (PDIP)
S: Small Outline Plastic (SOIC)
V: Metric Quad Flatpack (MQFP)
W: Wafer

**TEMPERATURE RANGE**
C: Commercial, 0°C to +70°C
I: Industrial, -40°C to +85°C
M: Military, -55°C to +125°C

**SPEED GRADE IN MHz**

**HIGH-RELIABILITY DESIGNATOR**
/883: -55°C to +125°C Fully Compliant to MIL-STD-883, Class B/QML

NOTE: Suffix EV, EVAL: Evaluation Kit (Available for some products).

## ICL, ICM Types

**ICL 8069D C B A Z T**

**DEVICE FAMILY**
ICL
ICM

**PART NUMBER**

**TEMPERATURE RANGE**
C: Commercial, 0°C to +70°C
I: Industrial, -25°C to +85°C or -40°C to +85°C (Specified on Data Sheet)
M: Military, -55°C to +125°C

**PACKAGE DESIGNATOR**
B: Small Outline Plastic (SOIC)
D: Ceramic Dual-In-Line Metal-Seal (SBDIP)
F: Ceramic Flatpack
H: Small Outline Transistor Plastic (SOT)
J: Ceramic Dual-In-Line Frit-Seal (CERDIP)
M: Metric Plastic Quad Flatpack (MQFP)
P: Plastic Dual-In-Line
S: TO-52 Can
T: Can (TO-99, TO-100)
Z: TO-92 (Plastic)
/W: Wafer
/D: Chip

**PIN COUNT DESIGNATOR**

| SUFFIX | PIN COUNT | DIAMETER |
|---|---|---|
| A | 8 | |
| B | 10 | |
| C | 12 | |
| D | 14 | |
| E | 16 | |
| F | 22 | |
| G | 24 | |
| H | 42 | |
| I | 28 | |
| J | 32 | |
| K | 35 | |
| L | 40 | |
| N | 18 | |
| P | 20 | |
| Q | 2 | |
| R | 3 | |
| V | 8 | 0.200″ Pin Circle, Isolated Case |
| W | 10 | 0.230″ Pin Circle, Isolated Case |
| X | 10 | 0.230″ Pin Circle, Case to Pin 5 |
| Y | 8 | 0.200″ Pin Circle, Case to Pin 4 |
| Z | 8 | 0.230″ Pin Circle, Case to Pin 5 |
| 44 | 44 | |

**PB-FREE OPTION**
Z: Pb-Free Product
ZA: Pb-Free with Anneal

**SUFFIX**
/883B: Fully Compliant to MIL-STD-883 Class B/QML
T: Tape and Reel

## ICL Types (Interface Circuits)

**ICL 3243 E C V - T**

**DEVICE FAMILY**
ICL Interface

**PART NUMBER**

**E:** 15kV ESD Protected

**TEMPERATURE RANGE**
C: Commercial (0°C to +70°C)
I: Industrial (-40°C to +85°C)

**PACKAGE DESIGNATOR**
A: Shrink Small Outline (SSOP)
B: 300 mil Small Outline Plastic (SOIC)
BN: 150 mil Small Outline Plastic (SOIC)
P: Plastic Dual-In-Line (PDIP)
V: TSSOP
Y: Die

**TAPE AND REEL**

## JM JAN-QML Types

**JM38510/ 051 51 B C A**

**GENERAL SPECIFICATIONS**

**DEVICE FAMILY**

**SPECIFIC DEVICE**

**DEVICE CLASS**
B: Class B/QML

**PACKAGE DESIGNATOR**
See Specific Data Sheets

**LEAD FINISH**
A: Solder
C: Gold