CAN Controller

IPextreme

National Semiconductor® CAN Controller

PRODUCT BROCHURE

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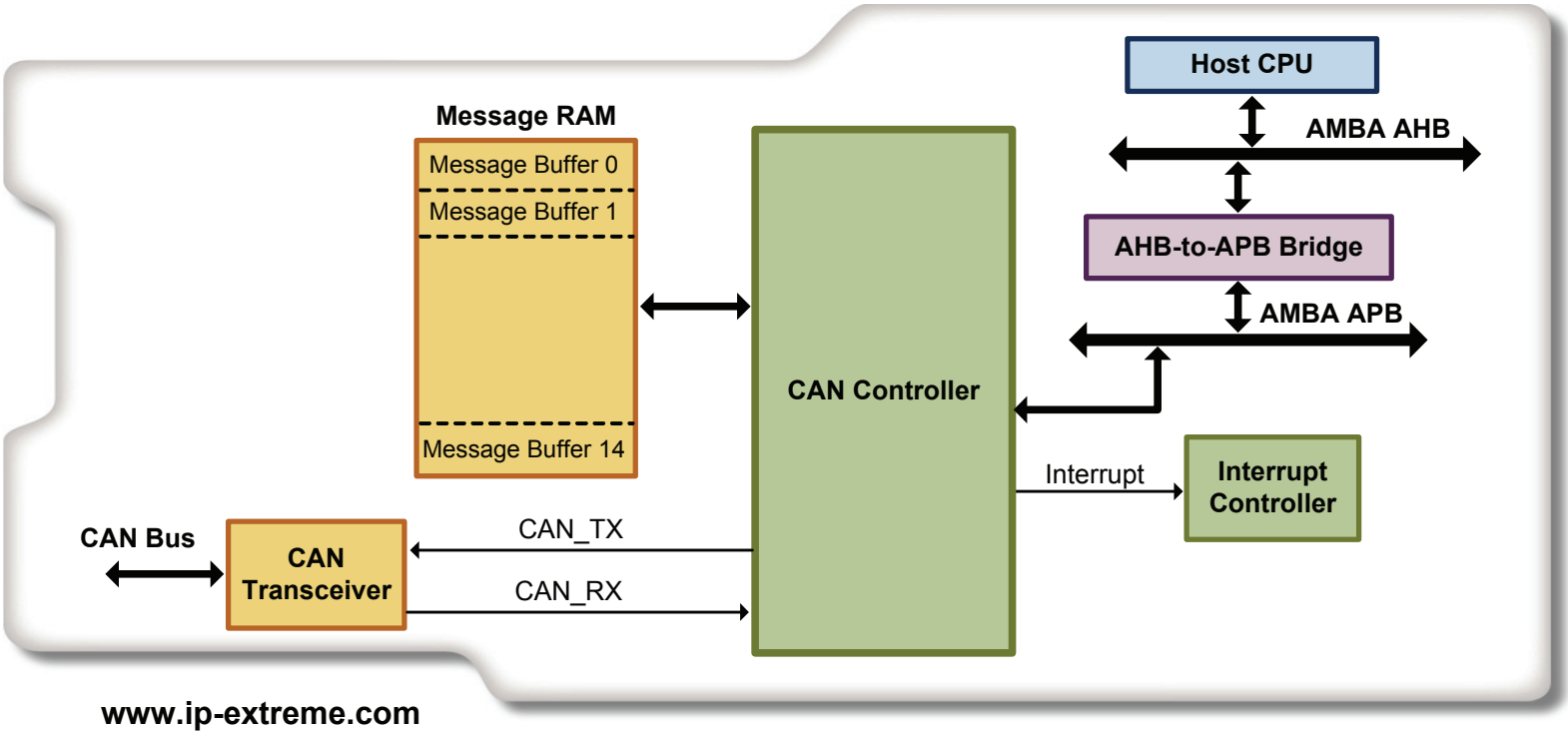
The CAN Controller is a synthesizable IP block providing Controller Area Network (CAN) functionality compliant with the *CAN Specification* Revision 2.0 Part B. Proven in high-volume standard devices from National Semiconductor, the CAN Controller features a programmable bit rate to support applications that require a high-speed (up to 1 Mbit/s) or a low-speed CAN interface. Fifteen message buffers, each configurable for transmit or receive, and programmable acceptance filtering provide support for both Full-CAN and Basic-CAN operation.

The host interface of the CAN Controller complies with the AMBA 2.0 APB protocol. Host-accessible control registers provide CPU control of bit rate, diagnostic functions, enabling/disabling the CAN Controller, CAN pin logic level, CAN bit time partitioning, incoming message filtering, transmit message prioritization, and enabling/disabling interrupts. Status registers provide CAN node, interrupt, and error/diagnostic status.

The CAN bus interface consists of serial transmit and receive signals that connect to an external transceiver through chip-level I/O pads. To reduce chip-level pin count, the transmit and receive signals can be shared with other on-chip functions through a General Purpose I/O (GPIO) Controller.

FEATURES

- Programmable bit rate—up to 1 Mbit/sec
- Standard or extended frames
- 15 message buffers—each configurable for transmit or receive
- Remote frame support
  - Automatic transmission after reception of a Remote Transmission Request (RTR)
  - Automatic receive after transmission of an RTR
- Programmable acceptance filtering
  - Global mask for message buffers 0–13
  - Individual mask for message buffer 14
- Programmable transmit priority
- Time stamp counter—programmable for automatic reset on transmit/receive
- Interrupt capabilities
  - Interrupts available for message buffer transmit/receive and CAN error conditions
  - Interrupts can be individually enabled/disabled



FEATURES (CONTINUED)

- Diagnostic functions
  - Error identification
  - Loopback (internal or external)
  - Listen-only mode for initialization

PROGRAMMABLE ACCEPTANCE FILTERING

The CAN Controller provides Full-CAN support through programmable acceptance filtering, minimizing CPU interaction. Message buffers 0–13 use a single global mask (GMASK) to accept either specific message IDs or a range of message IDs. The host CPU determines, by either polling or interrupt, when an accepted message is available in a receive message buffer.

A separate, dedicated mask (BMASK) allows message buffer 14 to be configured for Basic-CAN operation, in which the CPU implements the message filtering. If Basic-CAN support is not required, message buffer 14 can be programmed as an additional Full-CAN path by setting BMASK equal to GMASK.

PROGRAMMABLE TRANSMIT PRIORITY

Using two levels of transmit priority (programmable priority level and message buffer number), the host CPU can schedule several messages for transmission. The CAN Controller then automatically transmits the messages in the desired sequence. Performance is optimized because the CAN Controller continues to transmit scheduled messages in sequence, releasing the CAN bus only if bus arbitration is lost.

INTERFACES

- AMBA 2.0 APB host interface
  - 16-bit read/write data buses
  - 10-bit address bus
- CAN transmit and receive pins to/from an external transceiver
- Memory interface to the message buffer RAM (128 x 16 bits)
- One clock input
- One asynchronous reset input
- Interrupt signal to interrupt controller and/or host CPU
- DFT signals

HARDWARE CONFIGURATION OPTIONS

OPTION	RANGE	DEFAULT
Local clock gating for low-power operation	On or Off	Off

GATE COUNT AND PERFORMANCE

Gate count and maximum frequency depend on synthesis tool and target technology. Example values for a typical 130-nm technology are:

- 5500 (NAND2 equivalent) gates
- 100 MHz (APB clock)

DELIVERABLES

The CAN Controller is available in Source and Encrypted products. The Source product is fully configurable and is delivered in plain text Verilog source code. The Encrypted product, which is available in the Core Store, offers limited configurability (default parameter values) and is delivered in encrypted source code. Both products include:

- Synthesizable Verilog source code (encrypted in the Encrypted product)
- Integration testbench and tests
- Documentation
- Automatic configuration through the IPextreme IP distribution and support portal
- Scripts for simulation and synthesis with support for common EDA tools

IPextreme

IPextreme, Inc.
307 Orchard City Drive
Suite 202
Campbell, CA 95008
800-289-6412 (toll-free)
408-608-0421 (fax)

www.ip-extreme.com