e200 Core Family

IPextreme

Freescale Power Architecture™ IP

PRODUCT BROCHURE

Freescale Semiconductor, a founding member of Power.org and a driving force in the evolution of the Power Architecture since the original PowerPC, is the world's leading supplier of 32-bit controllers. Freescale's e200 family of Power Architecture cores are well proven in a range of embedded applications, including their popular MPC5500 series of automotive MCUs. Those same e200 cores are now available from IPextreme, enabling any SoC or ASSP designer to benefit from the Power Architecture.

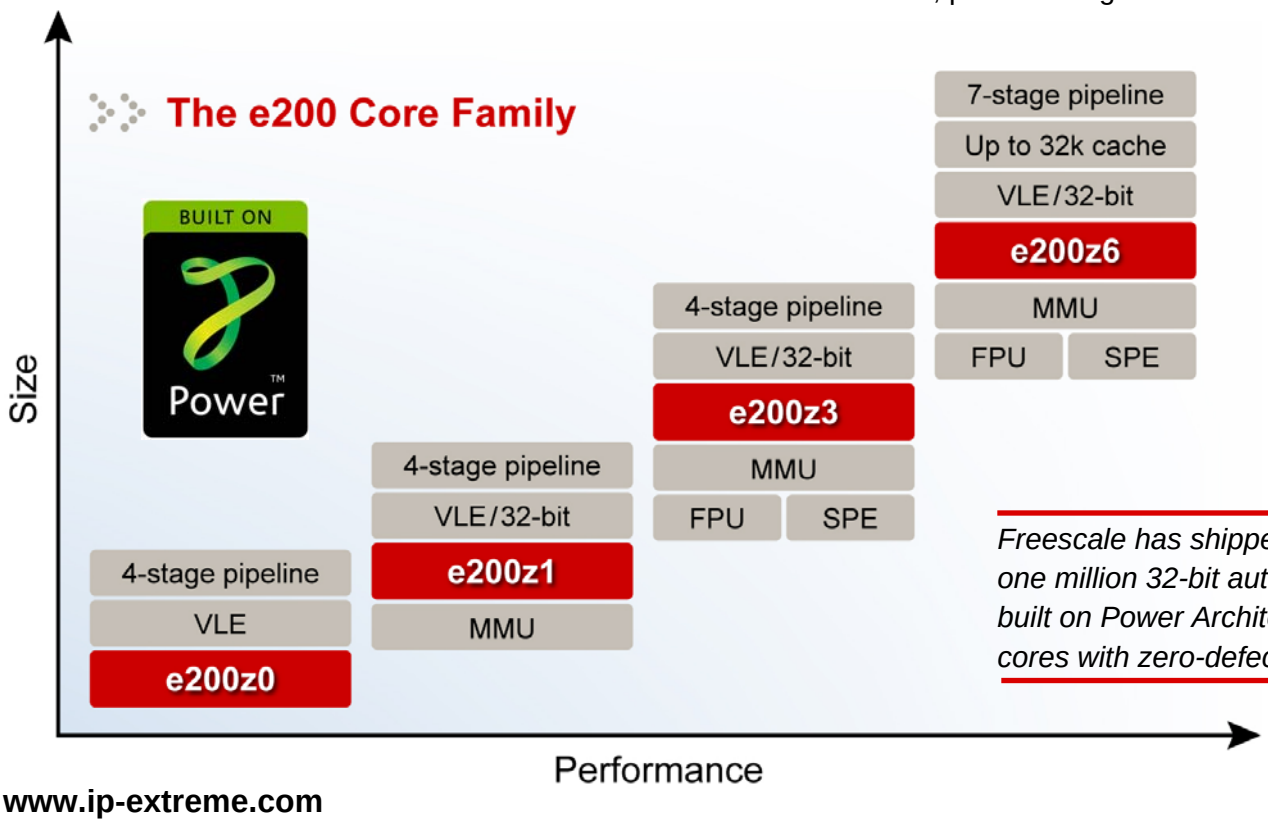
Freescale's e200 family of synthesizable, high-efficiency cores is intended for cost-sensitive, embedded real-time applications with significant performance requirements. The four e200 cores available through IPextreme—e200z0, e200z1, e200z3, and e200z6—provide a range of features ideal for automotive, avionics, robotics, industrial control, medical devices, and compact networking applications.

Built to Power Instruction Set Architecture (ISA) Version 2.03, all four cores support variable length encoding (VLE); all except the z0 also implement the full 32-bit Book E instruction set. The cores offer low interrupt latency, AMBA AHB connectivity, and low-power design through clock gating. Debug features include static debug through Nexus Class 1 and real time debug through Nexus Class 2/3.

The small-footprint z0 core has a compact four-stage pipeline and runs only the VLE instruction set, which delivers exceptional code density. Reduced memory requirements and compact design make the z0 ideal for low-cost applications.

In addition to running the full 32-bit and VLE instruction sets, the z1 and z3 feature an MMU for full operating system support. For applications with significant signal processing requirements, the z3 also includes a signal processing engine (SPE) and single-precision floating-point unit (FPU), which often eliminates the need for an additional DSP.

The z6 is the highest-performance core of the family, with a seven-stage pipeline machine, all of the features of the z3, plus an integrated cache unit.



Freescale has shipped more than one million 32-bit automotive MCUs built on Power Architecture e200 cores with zero-defect quality.

e200 FAMILY ADVANCED FEATURES

The e200 cores offer valuable extensions and advanced features while maintaining Power ISA Version 2.03 compatibility and support for PowerPC toolchains.

Variable Length Encoding (VLE)

VLE is a feature developed by Freescale and adopted by Power.org for inclusion in Power ISA Version 2.03. VLE optimizes code density by encoding 32-bit PowerPC instructions into mixed 16 and 32-bit instructions, reducing code footprint by up to 30 percent. 16 and 32-bit instructions may be freely intermixed. VLE is supported by most Power Architecture toolchains and is available on all four of the e200 family cores.

Signal Processing Engine (SPE)

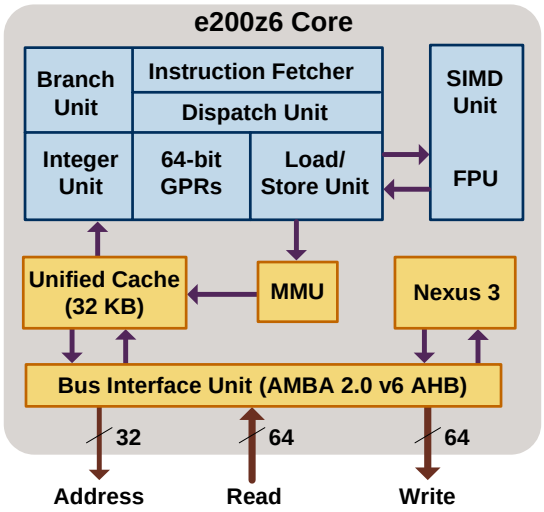
SPE features available on the z3 and z6 cores provide single-instruction multiple-data (SIMD) operations—execution of one operation on multiple sets of data. On the z3 and z6 cores, SIMD support is coupled with a floating point unit (FPU) for enhanced DSP operation including 16 and 32-bit integer and fractional data types, signed and unsigned arithmetic, and IEEE single-length floating point operations, with double-precision support available through software.

Memory Management (MMU)

The z1, z3, and z6 cores include an MMU, each with identical functionality and user interface, and cross-core code compatibility. The MMU is ideal for systems that require full operating system support. Its features include:

- Translation from 32-bit effective to 32-bit real addresses:
  - 32-entry MMU in the z6
  - 16-entry MMU in the z3
  - 8-entry MMU in the z1
- Support for nine page sizes (4 KB, 16 KB, 64 KB, 256 KB, 1 MB, 4 MB, 16 MB, 64 MB, and 256 MB)
- Accesses qualified by:
  - Address spaces: 2 data and 2 instruction
  - 8-bit process identifier (supervisor accessible or global resource)
- Selectable access privileges:
  - User Read/Write/Execute (UR/UW/UX)
  - Supervisor Read/Write/Execute (SR/SW/SX)

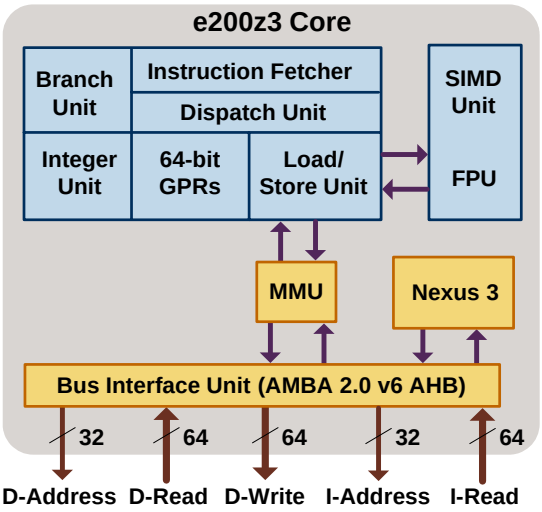
e200z6 CORE FEATURES



The z6 core is the high-end member of the e200 core family and offers the following features:

- 7-stage pipeline with in-order execution
- Single-issue (one instruction issued per clock cycle)
- 32-bit Power Architecture Book E CPU core
- VLE for code density
- Unified 32-KB, 8-way set-associative cache
- 32-entry unified MMU
- SIMD and FPU for enhanced DSP support
- AMBA AHB 2.0 v6 bus interface
- Single-cycle execution for most instructions
- Integer and floating point multiply and multiply-accumulate in 3 clocks, fully pipelined
- Integer divide in 6 to 16 clocks, unpipelined
- 3-cycle loads
- 1 to 3-cycle branches
- Small branch target address cache (BTAC) to accelerate loops
- Nexus Class 3 support

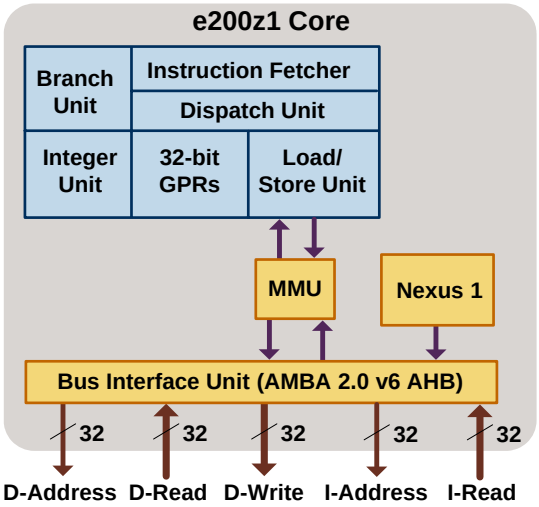
e200z3 CORE FEATURES



The z3 core is intended for SoC designs with fast on-chip memory access; it offers:

- Single-issue, in-order, 4-stage pipeline
- 32-bit Power Architecture Book E CPU core
- VLE for code density
- 16-entry unified MMU
- SIMD and FPU for enhanced DSP support
- AMBA AHB 2.0 v6 bus interface
- Single-cycle execution for most instructions
  - 1-cycle load, store, arithmetic, logical, and multiply
  - 1 to 2-cycle branches
  - Integer divide 6 to 16 clocks (unpipelined)
- Nexus Class 3 support

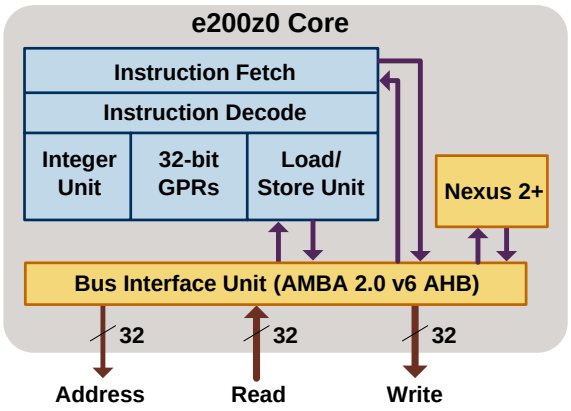
e200z1 CORE FEATURES



The z1 core is ideal for cost-sensitive applications that require an MMU but do not need enhanced DSP support. It offers:

- Single-issue, in-order, 4-stage pipeline
- 32-bit Power Architecture Book E CPU core
- VLE for code density
- 8-entry unified MMU
- AMBA AHB 2.0 v6 bus interface
- Single-cycle execution for most instructions
  - 1-cycle load, store, arithmetic, logical, and multiply
  - 1 to 2-cycle branches
  - Integer divide 6 to 16 clocks (unpipelined)
- Nexus Class 1 support

e200z0 CORE FEATURES



The z0 core is intended for low-end cacheless MCU implementations that do not require an MMU and can benefit most from very compact code. Its features include:

- In-order, 4-stage pipeline with pipeline stages mapped directly to 2-cycle AHB
- Power Architecture compatible VLE core
- Support for existing PowerPC VLE compilers
- Single-issue machine with 32-bit unified bus
- Single-cycle simple operations
- Single-cycle loads and stores
- Branches: 1-cycle not-taken, 2-cycle taken
- Nexus Class 2+ support (Nexus Class 2 plus selected Nexus Class 3/4 features)

SUMMARY OF SUPPORTED e200 FAMILY FEATURES				
Feature	**e200z0**	**e200z1**	**e200z3**	**e200z6**
Architecture	Power ISA 2.03 (VLE only)	Power ISA 2.03	Power ISA 2.03	Power ISA 2.03
VLE	Yes	Yes	Yes	Yes
Pipeline stages	4	4	4	7
L1 Unified Cache	—	—	—	32-KB, 8-way
MMU	—	8-entry	16-entry	32-entry
SPE	—	—	64-bit	64-bit
FPU	—	—	32x32	32x32
Bus Interface	Single AMBA 2.0 v6 32-bit read 32-bit write 32-bit address	Dual AMBA 2.0 v6 32-bit read 32-bit write 32-bit address	Dual AMBA 2.0 v6 64-bit read 64-bit write 32-bit address	Single AMBA 2.0 v6 64-bit read 64-bit write 32-bit address
Debug Interface	Nexus Class 2+	Nexus Class 1	Nexus Class 3	Nexus Class 3

DEVELOPMENT TOOLS

Power Architecture technology is supported by world-class development tools suites offered through leading tools developers, including:

- Compilers:
  - CodeWarrior
  - Green Hills
  - WindRiver
  - GNU
- Debuggers:
  - Green Hills
  - Lauterbach
  - iSystem
  - P&E Micro
- Simulators:
  - CodeWarrior (Core only)
  - Green Hills (Core only)
- Hardware:
  - Freescale Evaluation Board (EVB)
  - Green Hills (Nexus Class 1 and Class 2+)
  - Lauterbach (Class 1 and Class 2+)
  - iSystem (Class 1 & Class 2+)
  - P&E Micro (Nexus Class 1)
- Initialization tools: RAppID Init
- Modeling/Code generation:
  - dSpace TargetLink
  - MathWorks Simulink

Also supported are a rich set of real time operating systems, stacks, and drivers from Freescale partners. For more information, go to www.freescale.com.

DELIVERABLES

Each of the Freescale e200 Power Architecture cores is in technology-independent RTL source code format and includes:

- Synthesizable Verilog source code
- Integration testbench
- Documentation
- IPextreme XPack for design configuration, simulation, and synthesis with support for common EDA tools

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