



Infineon Technologies, a leading supplier of ICs for automotive and industrial applications, has developed the Multiprocessor Link Interface (MLI) as a standard chip-to-chip serial interface for:

- ▶ High-speed, inter-processor communications enabling parallel operations and resource sharing
- ▶ High-speed communication between processors and smart companion devices such as A/D converters (ADCs) which typically operate at different voltages and clock rates than the associated processor

MLI enables parallel processing with independent, heterogeneous CPUs operating in different clock domains. Like a DMA controller, MLI attaches directly to the system bus and transfers data autonomously with respect to the CPU. Using pre-defined address windows at the local (master) and remote (slave) end of the link, MLI executes serial data transfers automatically and transparently in response to system read/write commands.

A single MLI can function as both a local (master) controller and remote (slave) controller at the same time. Independent transmit and receive lines provide high-speed (typically 40 Mbps) full-duplex operation.

With just four wires each for transmit and receive, MLI is an easy-to-integrate, low-cost solution for parallel processing in distributed systems. MLI is also scalable, supporting up to four remote devices from a single MLI controller.

Infineon is deploying MLI in its TriCore series ECUs and in its ADC smart companion and FlexRay controller devices. To keep advanced automotive electronics systems affordable, IPextreme is making the MLI specification available and offering production-proven implementation IP. MLI IP from IPextreme is technology-independent and fully synthesizable.

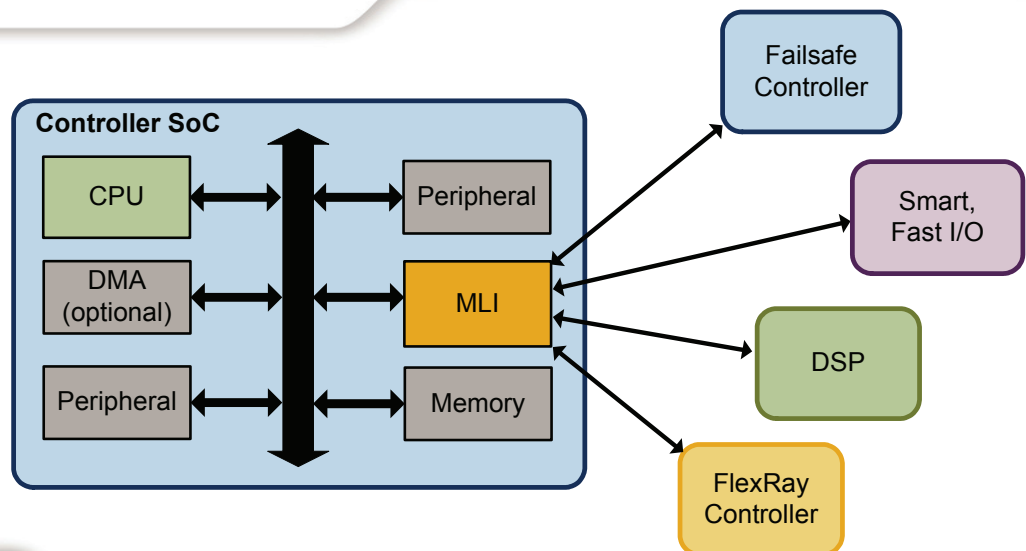
MLI PROVEN IN INFINEON CONTROLLERS AND COMPANION DEVICES



- ▶ TC1130/116x Families
- ▶ AUO-Next Generation Family
- ▶ CIC751
- ▶ CIC310

MLI connects up to 4 devices through high-speed serial links.

Read/write access to a predefined address window causes automatic serial data transfer from/to the corresponding remote device.



MLI FEATURES

- Synchronous high-speed serial protocol
- Automatic data transfer/request transaction between local and remote controller
- Fully transparent read/write access (supports remote programming)
- Complete address range of remote controller available (4 GB)
- Memory protection available on remote controller
- Can trigger interrupts in the remote controller by sending a command.
- Optimized frame protocol for efficient data transfers
- Transfers commands, address, and data
- Supports 32, 16, and 8-bit data transfers
- Error control through parity bit and handshake signals
- Programmable baud rate, maximum $F_{MLI}/2$
- Multiple remote controllers supported (up to 4)
- Full-duplex transmit and receive
- Low pin count: 4 signals for transmitting; 4 signals for receiving
- Loop delay between local and remote controllers can be up 15 clock cycles
- Security: MLI is locked after hardware reset and must be unlocked by the device itself

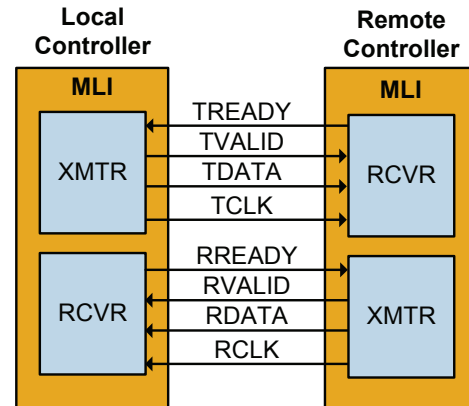
LOOP DELAY COMPENSATION

MLI achieves higher baud rates than can be achieved with SPI for off-chip communication partly because each MLI transmitter provides its own transmit clock; the transmit clock and data signals each travel the same length of wire. With SPI, the SPI master clock is used for both transmitting and receiving; the delay imposed by the round-trip cable length limits the maximum frequency at which the master and slave SPI devices can stay in sync when the slave is transmitting data to the master.

In addition, the MLI protocol does not limit the handshake signals to one clock period. MLI measures the handshake signal delay at initialization and compensates for it during operation, thereby achieving higher baud rates.

MLI CONNECTIONS

The transmit and receive paths each use four signals: clock, data, and two handshake signals. Up to four remote controllers can be connected using the same transmit data and clock signals. Transmit handshake signals and all four receive signals are unique for each remote controller.



MLI IMPLEMENTATION IP DELIVERABLES

- Synthesizable VHDL source code
- Integration testbench
- Documentation
- IPextreme XPack packaging technology for design configuration, simulation, and synthesis with support for common EDA tools

MLI SPECIFICATION

The MLI specification is also available from IPextreme. For information, go to www.ip-extreme.com.

IPextreme

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