National Semiconductor
The Sight & Sound of Information

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The Real-Time Clock is a counter that provides real-time information to the system. It is the same Real-Time Clock proven in high-volume controllers from National Semiconductor and is available exclusively from IPextreme as synthesizable IP.

The Real-Time Clock has alarm functions that can trigger periodic system interrupts or can be used to return the system to full operation from a low-power mode at predetermined times. In addition, the Real-Time Clock has a tuning mechanism that allows software to fine-tune the generation of the 1-Hz clock signal by compensating for deviations in input frequency.

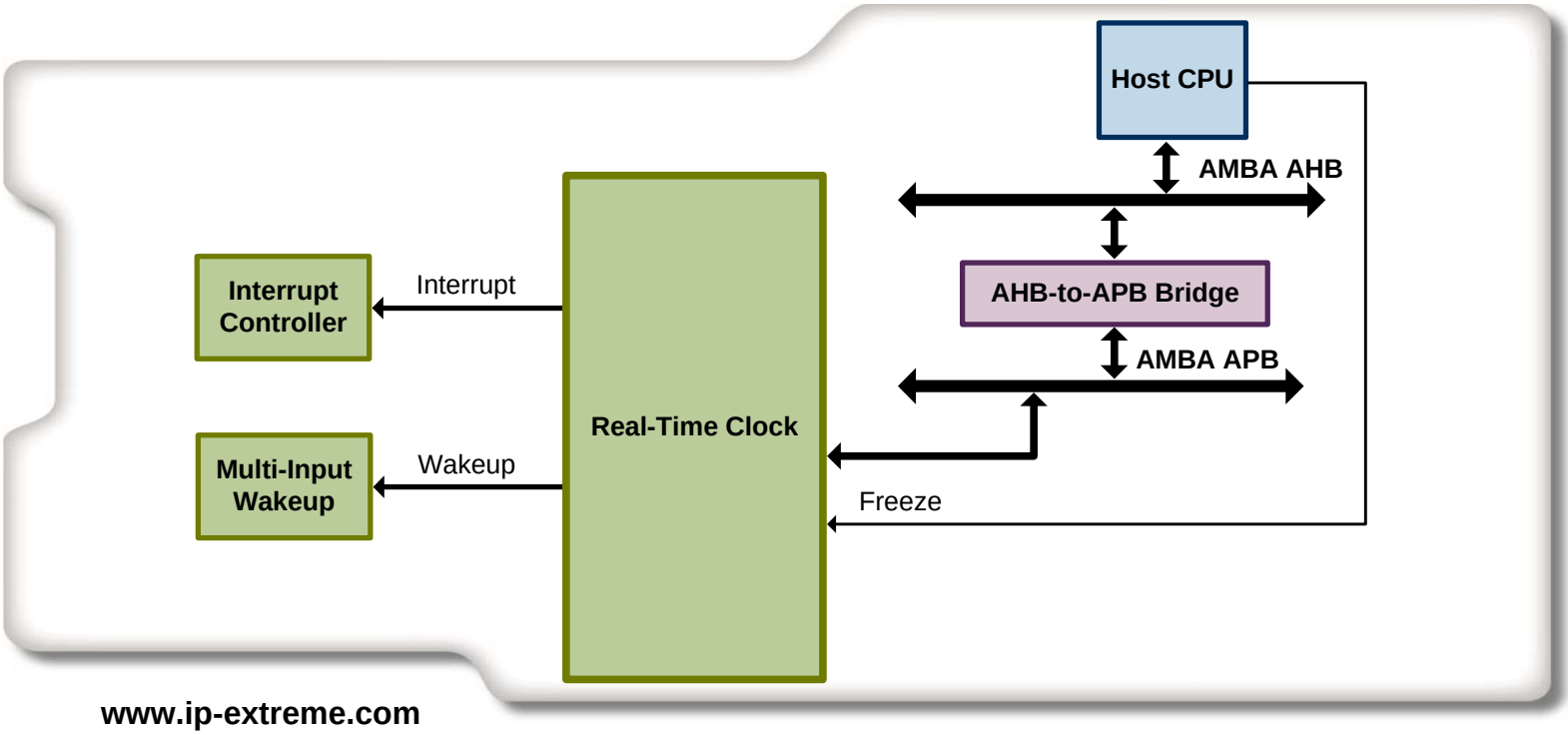
The Real-Time Clock provides real-time information based on a 32.768-kHz input clock and provides three alarm/interrupt capabilities based on the real-time count through independent programmable compare functions.

The host interface of the Real-Time Clock complies with the AMBA 2 APB protocol. Control registers within the Real-Time Clock provide CPU control of counter start/stop, counter register load, and compare values. Status registers indicate prescaler and counter values and interrupt status.

Interrupt and wakeup output signals are available for connection to an on-chip interrupt controller and/or wakeup controller.

FEATURES

- Slow clock input, typically 32.768 kHz – Input clock frequency variable up to the system clock frequency when using main oscillator prescaler output
- 16-bit prescaler counter
  - Restart upon programmable compare match or under software control
  - Generates accurate 1-Hz clock for Main Real-Time Counter
- 32-bit main real-time counter
  - Allows up to 136 years of time information based on 1-Hz input clock
  - Two compare registers with interrupt capabilities upon match
  - Software load to restart/set time after power-down
- Separate interrupt capability with enable for each compare match
- Slow clock event outputs for each compare match to be used as wakeup from power-down mode
- Debug support: Freeze or suspend Real Time Clock activity



INTERFACES

- AMBA 2 APB host interface
  - 32-bit read/write data buses
  - 10-bit address bus
- Clock interface
  - APB clock for registers and interrupt functions, and optionally as timer clock source
  - Slow clock input selectable as timer clock source
- Interrupt interface (one interrupt signal for each match event, plus combined interrupt)
- Wakeup interface (one wakeup signal for each match event)
- Reset interface (one asynchronous reset input and one power-on reset input)
- Freeze/suspend interface
- DFT signals

HARDWARE CONFIGURATION OPTIONS

OPTION	RANGE	DEFAULT
Local clock gating for low-power operation	On or Off	Off

GATE COUNT AND PERFORMANCE

Gate count and maximum frequency depend on synthesis tool and target technology. Example values for a typical 130-nm technology are:

- 4000 (NAND2 equivalent) gates
- 100 MHz (APB clock)

DELIVERABLES

The Real-Time Clock is available in Source and Encrypted products. The Source product is fully configurable and is delivered in plain text Verilog source code. The Encrypted product, which is available in the Core Store, offers limited configurability (default parameter values) and is delivered in encrypted source code. Both products include:

- Synthesizable Verilog source code (encrypted in the Encrypted product)
- Integration testbench and tests
- Documentation
- Automatic configuration through the IPextreme IP distribution and support portal
- Scripts for simulation and synthesis with support for common EDA tools

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