

The ColdFire V4 Core (CFV4CORE) is a high-performance implementation of the ubiquitous ColdFire architecture from Freescale Semiconductor, offering over 500 DMIPS of performance. Fully code compatible with ColdFire V1 and V2 devices, the ColdFire V4 Core offers high-end features such as cache and Memory Management Unit (MMU), plus advanced arithmetic units including hardware divider (DIV), enhanced MAC (EMAC), and an optional Floating Point Unit (FPU).

Like all ColdFire processor cores available from IPextreme, the ColdFire V4 Core is a production-proven design. The ColdFire V4 Core is the same IP implemented in Freescale's MCF5441x microcontrollers. By either including or excluding the FPU, you can configure the ColdFire V4 Core to match either the V4e or V4m processor configuration used in Freescale MCF54xx devices. And, like the ColdFire V1 and V2 cores, the ColdFire V4 Core benefits from the extensive ecosystem of development systems, tools, and software supporting the ColdFire architecture.

INDUSTRY-LEADING 32-BIT PERFORMANCE

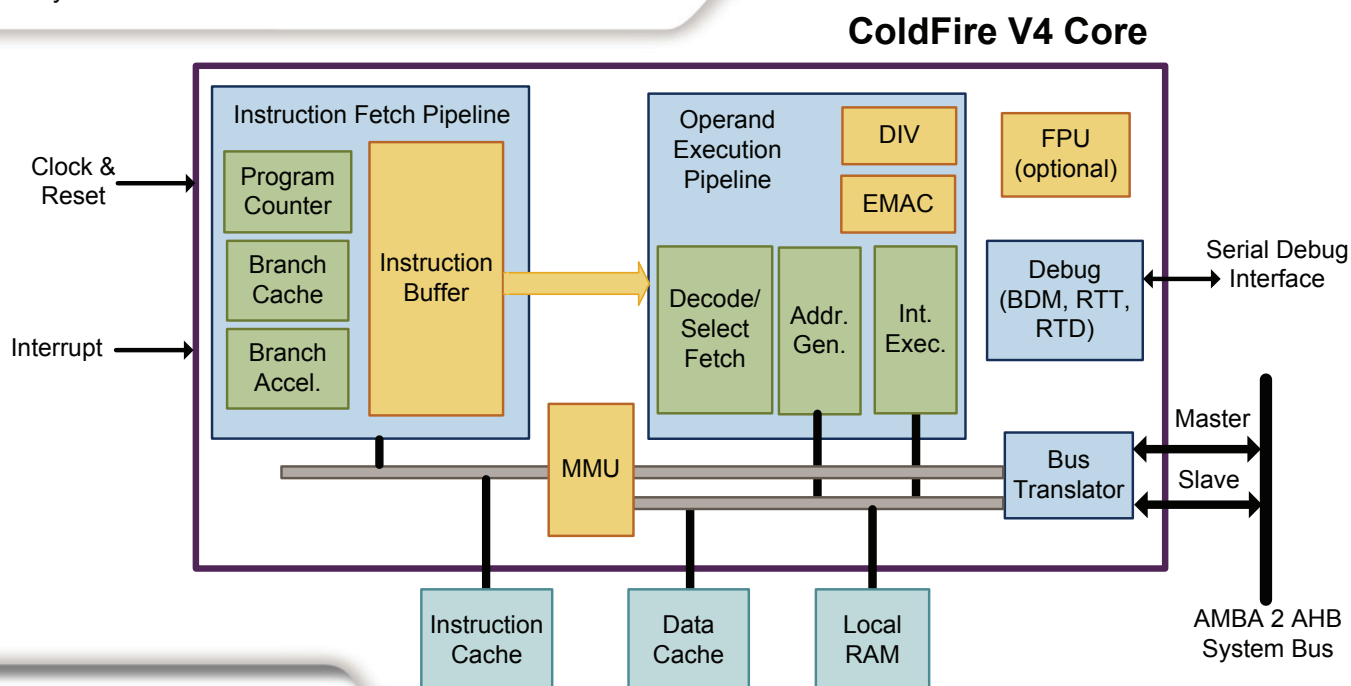
The ColdFire V4 Core achieves best-in-class 32-bit processor performance through a combination of features including a 9-stage pipeline with limited superscalar (dual-issue) instruction execution. The 9-stage pipeline consists of a 4-stage Instruction Fetch Pipeline (IFP) and 5-stage Operand Execution Pipeline (OEP) decoupled by a FIFO instruction buffer. The optional FPU executes instructions in parallel with the OEP. Separate clocks for the CPU and system bus enable the V4 ColdFire Core to operate at a higher frequency than the rest of the system.

The ColdFire V4 Core achieves 1.54 DMIPS/MHz and can run at up to 345 MHz in a 90-nm process technology.

Local RAM and cache, running at the CPU clock rate, further maximize system efficiency by reducing the overall number of system bus accesses, leaving more system bus bandwidth available for other system resources such as another processor or DMA controller. The system bus is the industry standard AMBA 2 AHB. The ColdFire V4 Core includes both an AHB master port and an AHB slave port, which enables an external AHB master to access the ColdFire V4 local RAM, either while the ColdFire V4 Core is running or while it is in low-power STOP mode.

APPLICATIONS

Processors based on the ColdFire architecture can be found in over 500 million devices worldwide, powering systems ranging from cameras and printers to robotics and factory automation. The superior performance of the ColdFire V4 Core makes it suitable for the most demanding applications such as high-end home entertainment, network storage, telecommunications, and networked gaming devices. Tightly integrated DIV and EMAC units support DSP-like algorithms for applications such as VoIP. For applications requiring floating-point calculations, the optional FPU provides IEEE-754 compliant floating-point support, operating on 64-bit, double-precision floating-point data and supporting single-precision and signed-integer input operands.



FEATURES

- ▶ 32-bit address and data paths
- ▶ Variable-length RISC architecture for maximum code density
- ▶ ColdFire ISA Revision C plus dedicated instructions for integrated arithmetic hardware (DIV, EMAC, and FPU)
- ▶ Branch acceleration for minimal change-of-flow execution time
- ▶ Big-endian data organization
- ▶ Up to 64 KB of local RAM with single-cycle access
- ▶ Separate instruction/data caches (up to 32 KB each)
- ▶ MMU with variable page sizes (up to 16 MB)
- ▶ AMBA 2 AHB system bus with master and slave ports
 - Master port for ColdFire V4 Core accesses
 - Slave port for external AHB master access to ColdFire V4 local RAM
- ▶ Bootable from local RAM or system (AHB) memory
- ▶ STOP mode for low-power operation
- ▶ ColdFire Debug Architecture Revision D+
 - Background Debug Mode (BDM)
 - Real-Time Trace (RTT)
 - Real-Time Debug (RTD)
 - On-chip, 128-entry trace buffer for low-cost trace over BDM
- ▶ Fully synchronous, synthesizable, scannable design

MEMORY ARCHITECTURE

The ColdFire V4 Core supports up to 4 GB of physical memory, including system memory accessed through the AMBA 2 AHB system bus and up to 64 KB of local RAM connected directly to the processor high-speed local bus for single-cycle access. The size of the local RAM is configurable (specified by input pin value) and may be 0 (no local RAM), 4, 8, 16, 32, or 64 KB.

The ColdFire V4 Core supports separate instruction and data caches, also connected to the processor high-speed bus with single-cycle access. The caches are independently sized, non-blocking, four-way set-associative with 16-byte line sizes. Each cache can be configured to be 0, 2, 4, 8, 16, or 32 KB (also specified by input pin value).

The MMU provides virtual-to-physical address translation using separate, software-managed instruction and data translation-lookaside buffers (TLBs), which are implemented as flip-flops within the ColdFire V4 Core. The MMU supports software-configurable memory page sizes of 4 KB, 8 KB, 1 MB, and 16 MB. The MMU is disabled upon exit from reset and must be enabled by software before it can be used.

DEVELOPMENT SUPPORT

The ColdFire architecture, including the ColdFire V4 Core, is supported by a vast assortment of development systems/tools and run-time software including libraries, stacks, drivers, and operating systems from providers such as Freescale, Green Hills Software, Wind River Systems, CodeSourcery, and many more. For example, the Sourcery G++ tool suite from www.codesourcery.com supports ColdFire V4 targets and can be used to develop new code or to retarget ColdFire V1/V2 programs to ColdFire V4 devices. A free version of the GNU compiler supporting ColdFire V4 targets is also available from www.gnu.org.

Freescale offers development boards, software, and CodeWarrior Development Tools (including a free version supporting the ColdFire V4 architecture). In addition, there are several operating systems supporting the ColdFire V4 architecture, including Linux/uClinux and several RTOS's, such as the MQX RTOS from [Embedded Access, Inc.](http://EmbeddedAccess.com) For a complete listing of ColdFire V4 development resources, visit www.freescale.com.

GATE COUNT/MAXIMUM FREQUENCY

The ColdFire V4 Core gate count depends on configuration, synthesis tool, and target technology. Example values for a typical 90-nm technology are:

- 250K gates with the FPU not included
- 315K gates with the FPU included

The maximum frequency for the same target technology is approximately 345 MHz.

DELIVERABLES

- Verilog source code
- Integration testbench and tests
- Documentation
- Scripts for simulation and synthesis with commonly-used EDA tools

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