CFV1CORE_ALTERA

IPextreme

Freescale™ ColdFire® V1 Core for Altera™ Cyclone™ III

PRODUCT BROCHURE

IPextreme freescale semiconductor ALTERA

The CFV1CORE_ALTERA, available free-of-charge from IPextreme, is the same ColdFire V1 processor core implemented in Freescale's MCF51QExx devices, delivered to you as a complete IP package ready for rapid integration into Altera Cyclone III FPGAs. The ColdFire V1 Core's system bus has been adapted to the Altera Avalon system interface for the CFV1CORE_ALTERA implementation. However, there are no architectural changes from the standard ColdFire V1 Core, which means that the CFV1CORE_ALTERA fully supports the ColdFire V1 Instruction Set Architecture (ISA_C) and is code-compatible with existing ColdFire V1 devices.

The CFV1CORE_ALTERA IP that you receive from IPextreme is fully compatible with Altera's Qsys and Quartus II tools. That means you can quickly and easily build a system from the CFV1CORE_ALTERA and your selected peripheral IP blocks, then generate a bitfile of the whole system and program it onto your Cyclone III device. You can then download software through the ColdFire V1 Core's single-wire debug interface and start running your application.

A free ColdFire processor on a low-cost, low-power Cyclone III FPGA gives you an ideal solution for both prototyping and production. And, should you want to migrate to an ASIC implementation in the future, you can get the same ColdFire V1 Core from IPextreme as fully-synthesizable RTL source code.

RESOURCES FOR HW/SW DEVELOPMENT

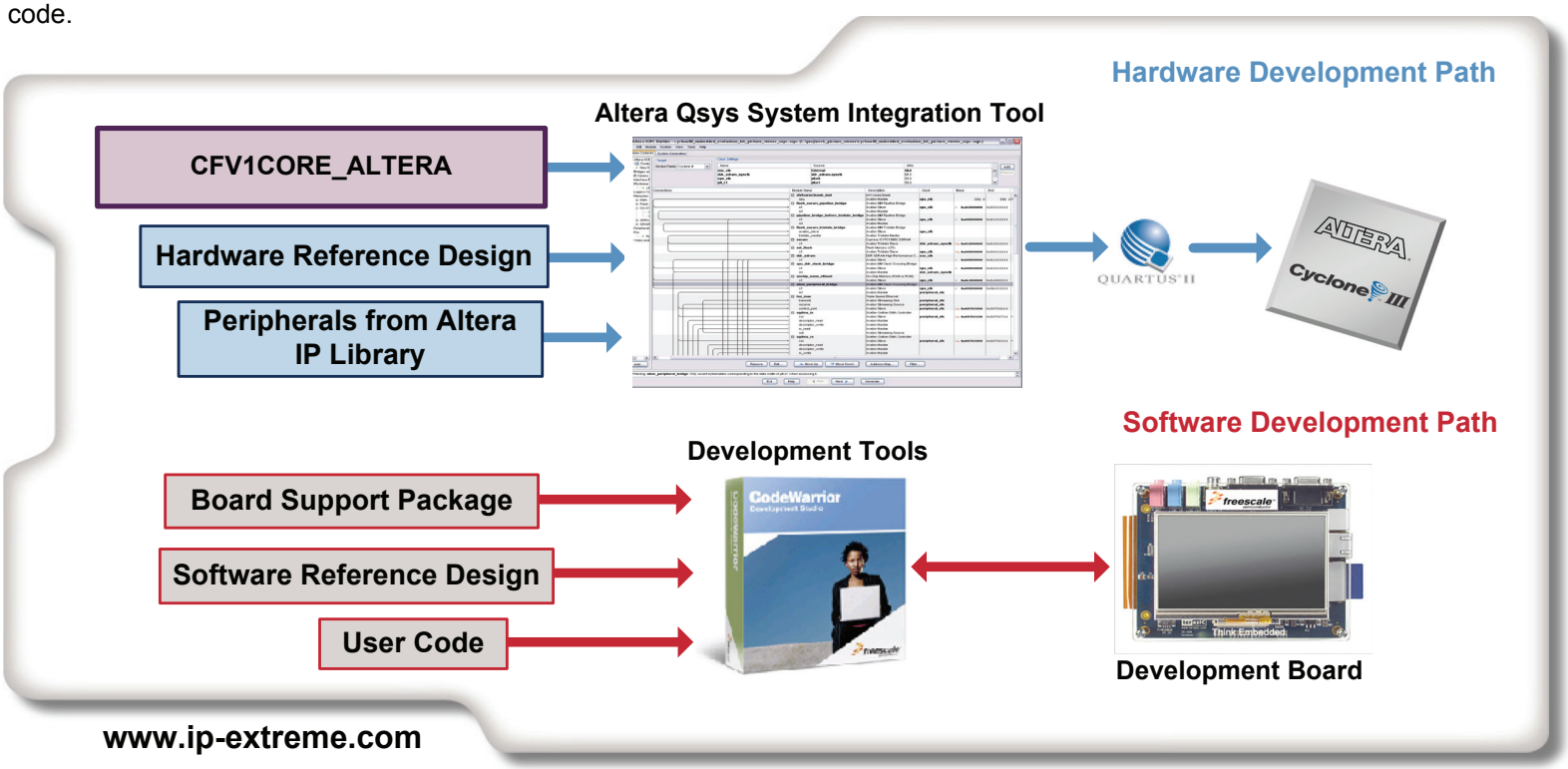
IPextreme provides the CFV1CORE_ALTERA, while resources from Altera and Freescale give you a jumpstart on hardware and software development.

Hardware development resources from Altera:

- A rich library of peripheral IP blocks
- Qsys system integration tool for drag-and-drop IP selection and integration
- Quartus II for synthesis, place-and-route, and device programming
- Cyclone III FPGAs—low-cost 65-nm FPGAs

ColdFire V1 reference board from Freescale:

- Evaluation/development board similar to Altera's Nios II embedded evaluation kit, but containing a ColdFire V1 based hardware reference design and equipped with a ColdFire debug connector
- CodeWarrior development tools
- Board support package
- Software reference design



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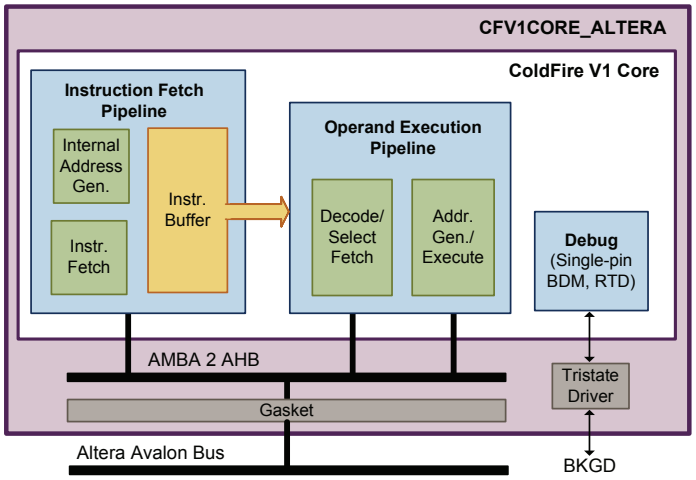

FEATURES

The ColdFire V1 Core offers a low-cost entry point to the ColdFire architecture. A simplified version of the ColdFire V2 Core, the ColdFire V1 Core is a low-power, low-area implementation that is fully upward compatible to higher-end ColdFire implementations such V2, V3, and V4.

Features of the ColdFire V1 Core as implemented in the CFV1CORE_ALTERA include:

- 32-bit processor core with 24-bit address bus (upper 8 bits of 32-bit Avalon address bus are 0x00)
- Unified instruction/data bus
- Independent, decoupled pipelines
  - 2-stage Instruction Fetch Pipeline
  - 2-stage Operand Execution Pipeline
  - FIFO Instruction Buffer is the decoupling mechanism
- ColdFire Instruction Set Architecture Rev. C (ISA_C)
- Variable-length RISC architecture with 16-bit, 32-bit, and 48-bit instructions
- Standard ColdFire user programming model with 16 general-purpose, 32-bit registers
- Simplified supervisor programming model supporting a supervisor stack pointer, vector base register, and CPU configuration register
- Static branch prediction mechanisms to minimize change-of-flow execution time
- Execute engines including ALU and barrel shifter
- Programmable response upon detection of certain illegal opcodes and illegal addresses (processor exception or system reset)
- ColdFire Debug B+ functionality mapped to the ColdFire V1 single-wire Background Debug Mode (BDM) interface
- Real time debug (RTD) support, with 6 hardware breakpoints (four PC, one address, and one data) that can be configured into a 1- or 2-level trigger with a programmable response (processor halt or interrupt)

In comparison to the configurable ColdFire V1 Core for ASIC implementation, the CFV1CORE_ALTERA is available in a single, fixed configuration:

- The hardware divider (DIV) and multiply-accumulate (MAC) unit are not included
- The single-wire debug module is included but the 64-entry trace buffer is not, which means program trace is not supported

ECOSYSTEM

Like all ColdFire architecture devices and IP products, the CFV1CORE_ALTERA is supported by a rich ecosystem of development tools, software stacks, and drivers from Freescale and other leading providers such as GNU, Green Hills Software, Wind River Systems, Accelerated Technology/Mentor Graphics, and many others.

TECHNICAL SPECIFICATIONS

- Size: ~6000 LUTs
- Frequency: 80 MHz (typical)

DELIVERABLES

- Encrypted RTL source code and Qsys component for the CFV1CORE_ALTERA
- Quartus IP license
- Integration testbench and example test programs
- Documentation

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