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The National Semiconductor IP Library for AMBA Interconnect is a collection of AMBA 2 compliant building blocks providing both the AMBA bus fabric and a rich set of peripheral functions.

The AMBA IP Library components connect to the AMBA 2 AHB and/or APB and are suitable for use with any AMBA 2 compatible controller—for example, the National Semiconductor CR16CP. The CR16CP is also available from IPextreme; however, AMBA IP Library components can be used with or without the CR16CP.

IP FOR A VARIETY OF FUNCTIONS

AMBA IP Library components implement a wide range of functions, enabling rapid development of complete subsystems. Available functions include:

- AMBA bus fabric (AHB and APB)
- System functions such as DMA, interrupt control, real-time clock, timers, and wakeup
- Standard interfaces such as USART, CAN, I2S, I2C, Smart Card, GPIO, and an advanced audio interface

Several of the components support DMA operation for reduced CPU utilization.

To support system debug, several of the peripherals also have a freeze input signal to halt the activity of the peripheral.

Each component implements clock gating for low-power operation and offers suitable configuration options for device-specific features.

AMBA BUS FABRIC IP

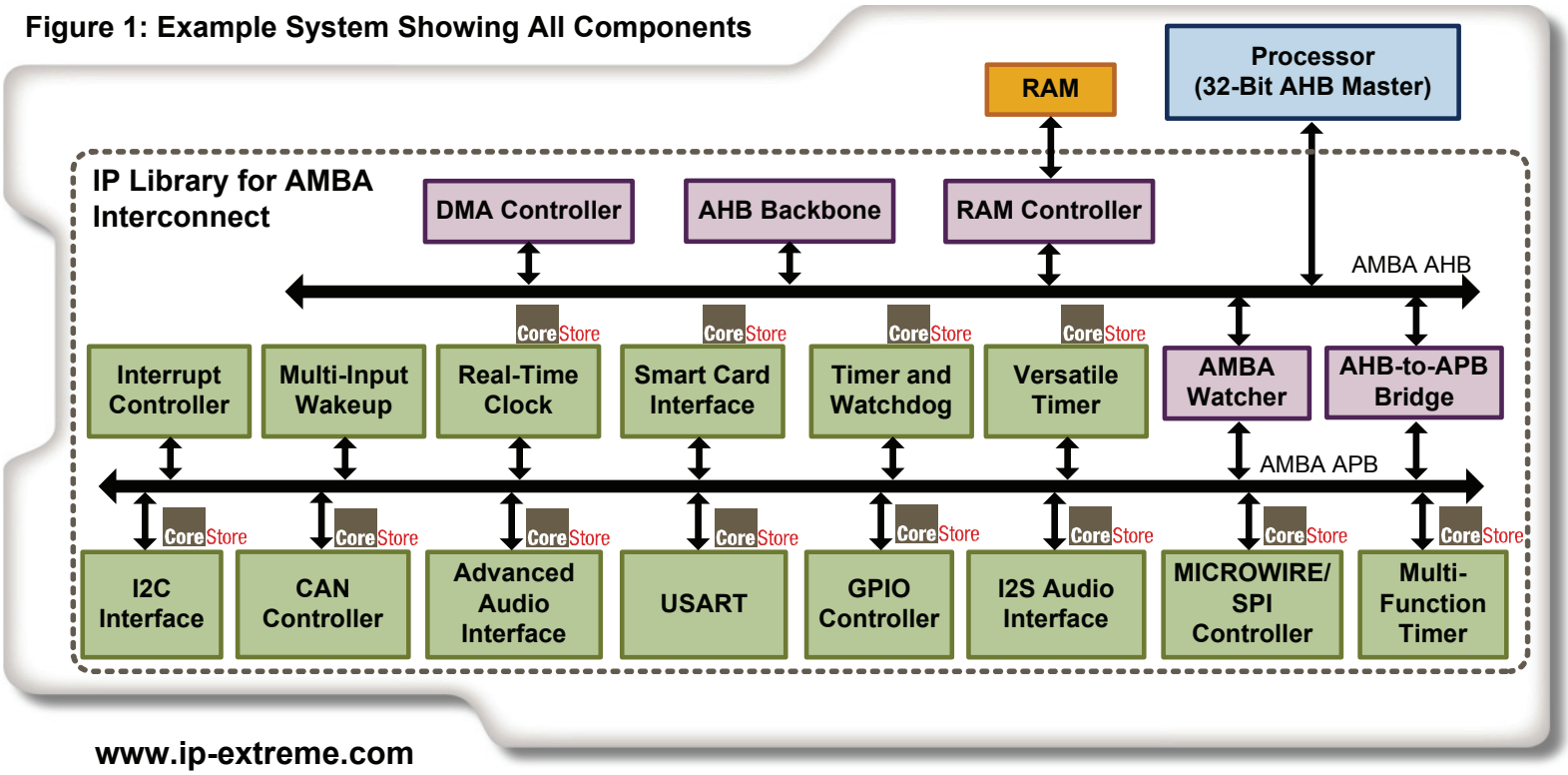
AHB Backbone

The AHB Backbone provides the AHB fabric to connect AHB masters and slaves. It consists of two main modules: Arbiter and Decoder.

The Arbiter ensures that only one bus master can initiate data transfers at any given time. It contains an optional register interface for allocating priorities and algorithms, and for selecting the default AHB master.

The Decoder generates a select signal for the selected slave, based on the address driven by the current AHB master. The Decoder supports up to 8 address regions for each slave.

Figure 1: Example System Showing All Components



AHB Watcher

The AHB Watcher monitors the AHB and logs bus errors as well as attempts to access illegal address locations by any of the AHB bus masters (for example, a CPU or DMA controller). The AHB Watcher status can be checked by polling or through a maskable interrupt.

AHB-to-APB Bridge

The AHB-to-APB Bridge provides the interface between the AMBA AHB and APB, acting as a slave on the AHB and as the bus master on the APB. It supports up to 16 APB slaves, 16 or 32-bit APB bus widths, and AHB:APB clock ratios ranging from 1:1 to 16:1 (in integer intervals).

SYSTEM FUNCTIONS (AHB)

DMA Controller

The DMA Controller attaches to the AMBA AHB and provides up to 16 DMA channels for transferring blocks of data between memory and I/O devices with minimal CPU intervention. The DMA Controller supports hardware DMA requests from up to 64 sources. In addition, each DMA channel supports a software DMA request.

RAM Controller

The RAM Controller attaches to the AHB and enables connection of on-chip RAM, providing a generic interface compatible to a single-port, synchronous SRAM.

SYSTEM FUNCTIONS (APB)

Interrupt Controller

The Interrupt Controller receives internal and external interrupt sources and generates maskable and non-maskable interrupts to the CPU when required. For non-maskable interrupts (NMIs), the Interrupt Controller supports:

- 1–7 internal NMI sources
- External NMI
- External In-System Emulator (ISE) interrupt (optional)

For maskable interrupts, the Interrupt Controller supports:

- 1–127 level-sensitive or software-triggered interrupt sources
- CPU vectored-interrupt mode
- Fixed priority allocation between interrupt sources
- Enabling/disabling of individual interrupt sources
- Polling of interrupt sources through a status register, regardless of whether the interrupts are enabled or disabled

Timer and Watchdog CoreStore

The Timer and Watchdog generates the clocks and interrupts used for periodic functions in the system and provides watchdog protection of software execution. Features include:

- Programmable input clock prescaler
- 16-bit programmable interrupt timer
- 8-bit watchdog counter
- Detection and watchdog signal generation for a variety of conditions
- Watchdog freeze input
- Lock option for fully protected watchdog
- Data match mechnanism for watchdog service

Multi-Function Timer CoreStore

The Multi-Function Timer is a 16-bit timer that can be programmed to support a wide range of application requirements. It contains two independent 16-bit timer/counters and two 16-bit reload/capture registers. The independent timer/counters can operate from several clock sources in PWM mode, input capture mode, pulse accumulate mode, PWM pulse train mode, or as system timers.

Versatile Timer CoreStore

The Versatile Timer controls eight I/O pins, each of which can function either as a PWM output with programmable output polarity or as a capture input with programmable event detection and timer reset. The Versatile Timer supports a flexible interrupt scheme with four separate system-level interrupt requests and a total of 16 interrupt sources, each with a separate interrupt pending flag and interrupt enable bit. It can be configured to provide up to:

- Eight fully independent 8-bit PWM channels
- Four fully independent 16-bit PWM channels
- Eight 16-bit input capture channels

The Versatile Timer implements four timer subsystems, each of which contains:

- One 16-bit counter
- Two 16-bit capture/compare registers
- One 8-bit fully programmable clock prescaler

Each timer subsystem can operate in the following modes:

- Low-power mode (all clocks stopped)
- Dual 8-bit PWM mode
- 16-bit PWM mode
- Dual 16-bit input capture mode

Multi-Input Wakeup CoreStore

The Multi-Input Wakeup module provides a wakeup signal interface to exit from various low-power modes. It supports 32 wakeup or interrupt sources and provides signal conditioning and grouping of external interrupt sources.

Real-Time Clock CoreStore

The Real-Time Clock module provides real-time information to the system. It implements a real-time counter and provides alarm functions that can trigger periodic system interrupts or can be used to return the system from a low-power mode at predetermined times. Features include:

- Programmable input clock divider
- 16-bit prescaler counter
- 32-bit main real-time counter
- Compare registers with interrupt capability upon match
- Interrupt generation for individual events
- Combined interrupt output

STANDARD INTERFACES

USART CoreStore

The USART module is a full-duplex synchronous/asynchronous receiver-transmitter capable of operating in either synchronous or asynchronous (UART) mode. It supports a wide range of software programmable baud rates and data formats, parity generation, error detection, flow control, and wakeup pattern detection. It can generate interrupts for several conditions—each with a separate enable—and supports DMA for both transmit and receive (also with separate enables).

I2S Audio Interface CoreStore

The I2S Audio Interface provides a dedicated serial link between an APB subsystem and off-chip audio devices. The I2S Audio Interface complies with the *I2S Bus specification*, Philips Semiconductors, February 1986 (Revised June, 1996). Features include:

- Bidirectional synchronous transceiver operation in either master or slave mode
- Support for a variety of audio data widths and sample rates
- Four 8-bit FIFOs (left/right transmit and left/right receive)
- Interrupt and DMA support

Advanced Audio Interface CoreStore

The Advanced Audio Interface provides a serial, synchronous, full-duplex interface to codecs and similar serial devices. It is functionally similar to a Motorola Synchronous Serial Interface (SSI). However, it only provides a subset of a standard Motorola SSI implementation. Features include:

- Synchronous or asynchronous receive/transmit paths
- 8 or 16-bit data words
- 16-word receive and transmit data FIFOs
- DMA support for reduced CPU utilization
- A variety of clocking and frame synchronization options

CAN Controller CoreStore

The Controller Area Network (CAN) Controller implements Full-CAN functionality compliant with *CAN Specification* Revision 2.0 Part B. It supports applications that require a high-speed (up to 1 Mbit/s) or a low-speed interface with CAN bus master capability. Features include:

- Programmable bit rate
- Standard or Extended Frames
- 15 message buffers, each configurable for transmit or receive, with one message buffer providing an optional Basic-CAN path
- Remote Frame support
- Acceptance filtering
- Interrupt capabilities
- Diagnostic functions

MICROWIRE/SPI Controller CoreStore

The MICROWIRE/SPI Controller is compatible with all MICROWIRE peripherals and SPI peripherals. It enables several devices to be connected on a three-wire system. At any given time, one device is the master and the others are slaves. The MICROWIRE/SPI Controller is capable of operating as either a master or a slave and in either 8-bit or 16-bit mode.

Smart Card Interface CoreStore

The Smart Card Interface provides a communication interface to a Smart Card, meeting all of the requirements defined in the ISO 7816-3 T=0 protocol and supporting the T=1 protocol through software. Features include:

- 16-byte transmit/receive (half-duplex) FIFO
- Software-configurable interrupts
- DMA support for transmit and receive

General Purpose I/O Contoller CoreStore

The General-Purpose I/O Controller provides a bidirectional port, with alternate function capablity, to an external off-chip interface. As an external interface, the General-Purpose I/O Controller is designed for direct connection to I/O pads. Features include:

- Programmable pin direction; each pin can function as an input or output port
- Internal weak pull-up, pull-down
- Direct low-impedance analog input
- Read back on all registers
- Each pin may be controlled by other modules through its software-selectable alternate function as an alternate source
- Selectable high drive current option

I2C Interface CoreStore

The I2C Interface provides a two-wire serial interface compatible with the ACCESS.bus physical layer, enabling easy integration of a wide range of low-cost memories and I/O devices such as EEPROMs, SRAMs, timers, A/D converters, D/A converters, clock chips, and peripheral drivers.

The I2C Interface is also compatible with Intel's System Management Bus (SMBus) and Philips' I2C bus. It can be configured as a bus master or slave, and can maintain bidirectional communications with both multiple master and slave devices.

The I2C Interface can be used with polling or interrupt.

DELIVERABLES

Each AMBA IP Library component is delivered in technology-independent RTL source code format. Components purchased from the IPextreme Core Store are delivered in encrypted source code format. Each product package includes:

- Synthesizable Verilog source code (encrypted if purchased from the Core Store)
- Integration testbench and tests
- Documentation
- Automatic configuration through the IPextreme IP Distribution and Support Portal
- Scripts for simulation and synthesis with support for commonly used EDA tools

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