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The Advanced Audio Interface (AAI) provides a full-duplex, serial, synchronous interface to codecs and similar serial devices. It is the same Advanced Audio Interface proven in high-volume devices from National Semiconductor and is available exclusively from IPextreme as synthesizable IP.

The host interface of the AAI complies with the AMBA 2.0 APB protocol. Control registers provide CPU control of operating mode, data word length, shift clock and frame sync generation, FIFO threshold levels, transmit/receive slot assignment in Network mode, and enabling/disabling interrupts. Status registers provide interrupt and FIFO status.

Transfer of audio data between the AAI and the host system can be either interrupt-driven or through DMA to reduce CPU utilization. When configured for interrupt-driven operation, the AAI buffers the audio data in 16-word receive and transmit FIFOs. When configured for DMA, the AAI buffers the audio data in registers.

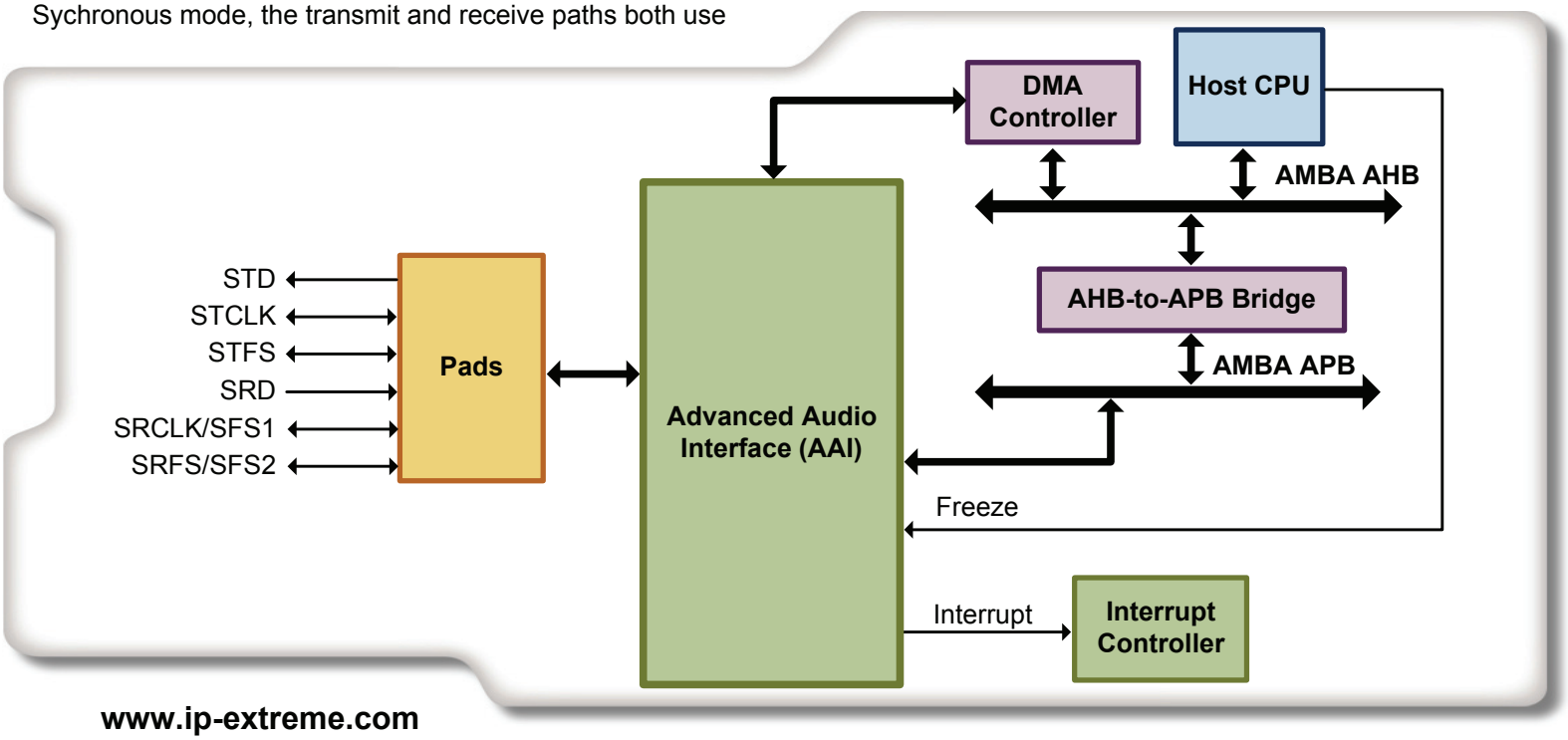
The transmit and receive paths can operate either asychronously or synchronously to each other. Each path uses a three-wire serial interface to the external codec: shift clock (STCLK/SRCLK), frame sync (STFS/SRFS), and data (STD/SRD).

In Asynchronous mode, the transmit and receive paths each use their respective shift clock and frame sync signals. In Sychronous mode, the transmit and receive paths both use the transmit shift clock and frame sync signals; the receive shift clock and frame sync signals then function as auxiliary frame sync signals (SFS1 and SFS2) to enable addressing of multiple codecs in Network mode.

To reduce chip-level pin count, the interface signals to the external codec can be shared with other on-chip functions through a General Purpose I/O (GPIO) Controller.

FEATURES

- Asynchronous or synchronous transmit/receive paths
- 8 or 16-bit word lengths
- In 16-bit mode, bits data 14–16 can be used for functions such as gain control if they are not used as audio data bits
- Normal mode or Network mode (up to 4 slots per frame)
- Active slot assignment for transmit/receive in Network mode
- IOM-2 mode for connection to an ISDN controller
- 16-word transmit/receive FIFOs for interrupt-driven operation
- Transmit/receive registers for DMA operation
- Internally or externally generated shift clock



FEATURES (CONTINUED)

- Primary and secondary clock reference sources for internally generated shift clock
- Programmable frame sync signal
  - Internally or externally generated
  - Normal or inverted
  - Short or long frame sync pulse
- Auxiliary frame sync signals available in Synchronous mode support addressing of multiple codes (Network mode)
- Loopback mode
- Freeze/suspend operation for system debug support
- Local clock gating for minimal power consumption

NORMAL/NETWORK MODE

In Normal mode, there is a single slot per frame. The AAI either transmits or receives a single data word in slot 0 if slot 0 is assigned to the AAI for transmit or receive. In Network mode, there up to four slots per frame. The AAI transmits or receives a single data word in each of its assigned transmit/receive slots. Each slot can be assigned to a separate DMA channel or can be interrupt-driven.

INTERFACES

- AMBA 2.0 APB host interface
  - 16-bit read/write data buses
  - 10-bit address bus
- Codec interface pins (STD, STCLK, STFS, SRD, SRCLK/SFS1, SRFS/SFS2) through chip I/O pads (optionally through a GPIO Controller)
- DMA interface
  - Four transmit DMA channels
  - Four receive DMA channels
- Clock interface
  - APB clock for registers, DMA, and interrupt functions
  - Shift clock inputs for extenally generated shift clocks
  - Primary and secondary clock reference inputs for internally generated shift clocks
- Interrupt interface (one interrupt signal)
- One asynchronous reset input
- Freeze/suspend interface
- DFT signals

GATE COUNT AND PERFORMANCE

Gate count and maximum frequency depend on synthesis tool and target technology. Example values for a typical 130-nm technology are:

- 13,900 (NAND2 equivalent) gates
- 100 MHz (APB clock)

DELIVERABLES

The AAI is available in Source and Encrypted products. The Source product is delivered in plain text Verilog source code. The Encrypted product, which is available in the Core Store, is delivered in encrypted source code. Both products include:

- Synthesizable Verilog source code (encrypted in the Encrypted product)
- Integration testbench and tests
- Documentation
- Scripts for simulation and synthesis with support for common EDA tools

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