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The Multi-Function Timer implements two independent 16-bit timer/counters, each of which offers a choice of clock sources and can be configured to operate in any of several modes. It is the same Multi-Function Timer proven in high-volume controllers from National Semiconductor and is available exclusively from IPextreme as synthesizable IP.

The operating mode of the Multi-Function Timer determines the function of each of the two timer/counters:

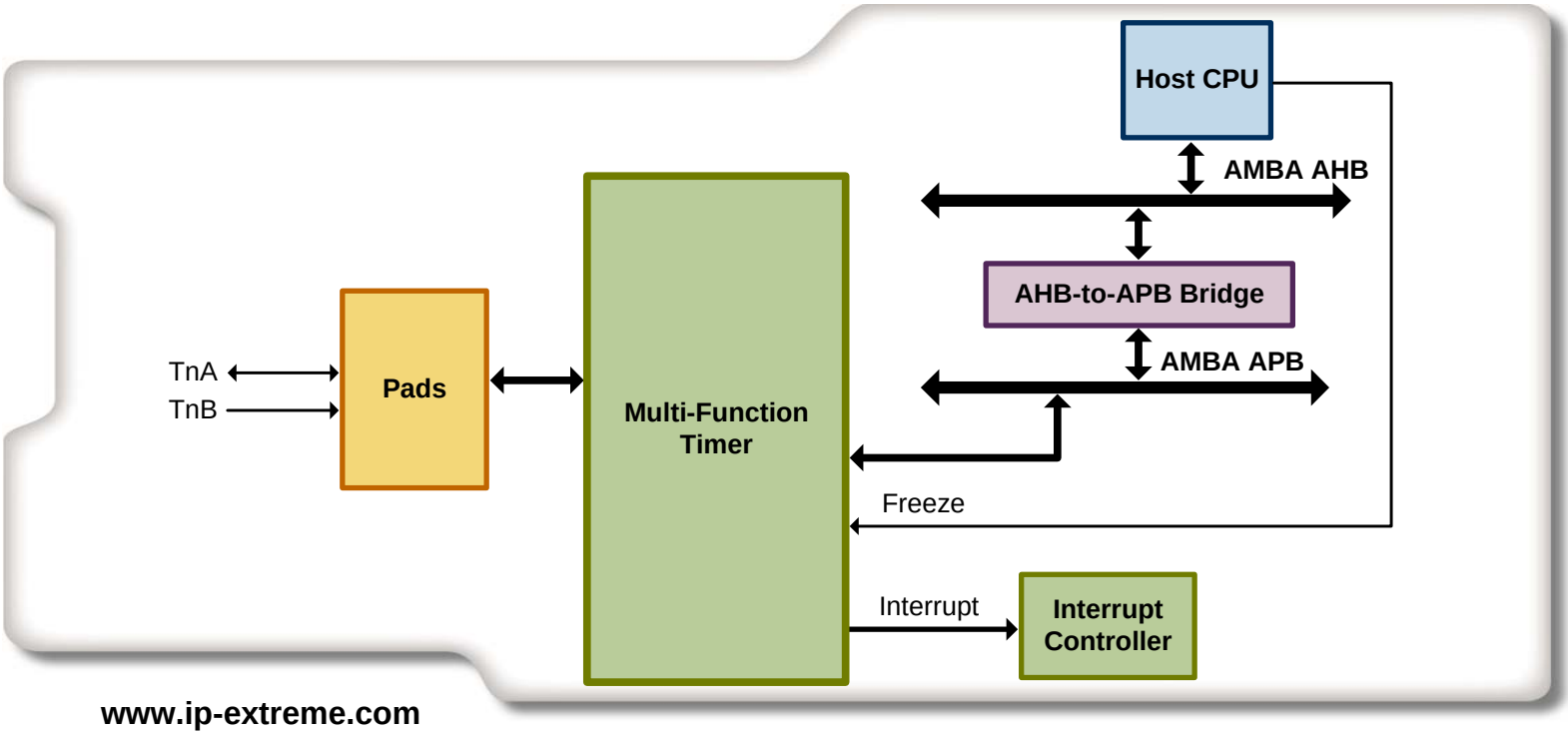
- Processor-independent pulse width modulation (PWM) mode generates pulses of a specified width and duty cycle, and provides a general-purpose timer/counter.
- Dual-input capture mode measures the elapsed time between occurrences of external events, and provides a general-purpose timer/counter.
- Dual independent timer mode generates system timing signals or counts occurrences of external events.
- Single-input capture and single timer mode provides one external event counter and one system timer.

The host interface of the Multi-Function Timer complies with the AMBA 2 APB protocol. Control registers within the Multi-Function Timer provide CPU control of timer mode, clock source selection and prescaling, signal polarity, and enabling/disabling/clearing interrupts. Status registers indicate timer/capture values and interrupt status.

The functions of the off-chip interface signals (TnA and TnB) depend on the current operating mode. To reduce chip-level pin count, TnA and TnB can be shared with other on-chip functions through a General Purpose I/O Controller.

FEATURES

- Two 16-bit programmable timer/counters
- Two 16-bit reload/capture registers that function either as reload registers or as capture registers, depending on the mode of operation
- Clock source selectors that allow each counter to operate in:
  - Pulse-accumulate mode
  - External event mode
  - Prescaled system clock mode
  - Slow clock input mode
- Two I/O pins (TnA and TnB) with programmable edge detection that operate as:
  - Capture inputs
  - Capture and preset inputs
  - External event (clock) inputs
  - PWM outputs



FEATURES (CONTINUED)

- An 8-bit fully programmable clock prescaler
- Pulse train operation for generation of single or multiple PWM pulses
- Two interrupts—one for each counter—that can be triggered by a:
  - Timer underflow
  - Timer reload
  - Input capture
- Debug support: Freeze or suspend Multi-Function Timer activity

INTERFACES

- AMBA 2 APB host interface
  - 16-bit read/write data buses
  - 10-bit address bus
- TnA/TnB pins through chip I/O pads (optionally through a General-Purpose I/O Controller)
- Clock interface
  - APB clock for registers, interrupt functions, and optionally as timer clock source
  - Slow clock input selectable as timer clock source
- Interrupt interface (one interrupt signal for each timer, plus combined interrupt)
- One asynchronous reset input
- Freeze/suspend interface
- DFT signals

HARDWARE CONFIGURATION OPTIONS

OPTION	RANGE	DEFAULT
Local clock gating for low-power operation	On or Off	Off

GATE COUNT AND PERFORMANCE

Gate count and maximum frequency depend on synthesis tool and target technology. Example values for a typical 130-nm technology are:

- 2000 (NAND2 equivalent) gates
- 100 MHz (APB clock)

DELIVERABLES

The Multi-Function Timer is available in Source and Encrypted products. The Source product is fully configurable and is delivered in plain text Verilog source code. The Encrypted product, which is available in the Core Store, offers limited configurability (default parameter values) and is delivered in encrypted source code. Both products include:

- Synthesizable Verilog source code (encrypted in the Encrypted product)
- Integration testbench and tests
- Documentation
- Automatic configuration through the IPextreme IP distribution and support portal
- Scripts for simulation and synthesis with support for common EDA tools

IPextreme

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