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The USART is a full-duplex synchronous/asynchronous receiver-transmitter proven in high-volume devices from National Semiconductor and available exclusively from IPextreme as synthesizable IP.

The USART supports a wide range of software programmable baud rates and data formats and operates in either Synchronous or Asynchronous (UART) mode. It implements automatic parity generation and several error detection schemes. The USART is capable of detecting a wakeup pattern to selectively enable the receiver and implements flow control logic for hardware handshaking.

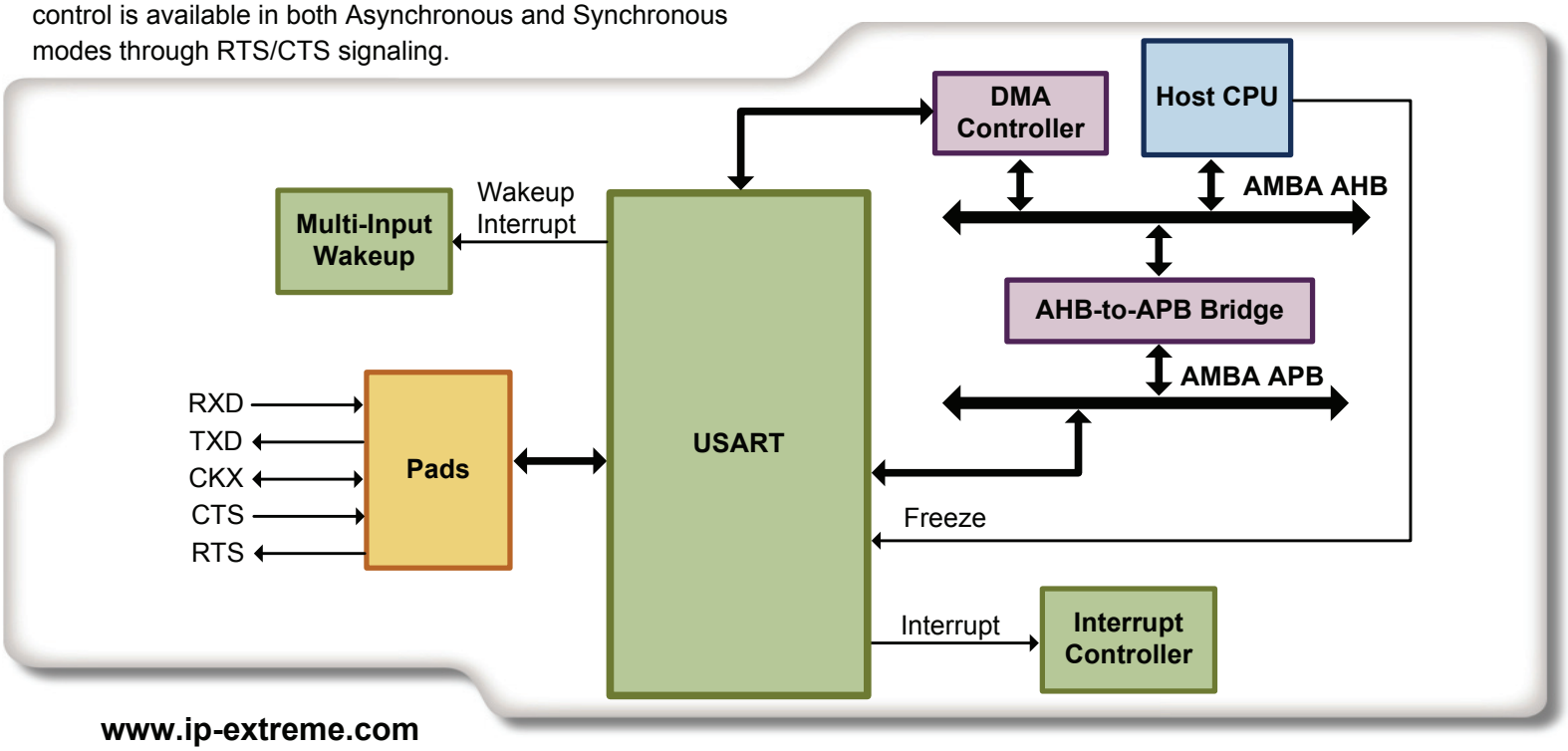
The host interface of the USART complies with the AMBA 2.0 APB protocol. Control registers within the USART provide CPU control of baud rate, frame format, wakeup pattern detection, operating mode, and enabling/disabling interrupts. Status registers provide interrupt and error status. In addition, there are registers that hold the transmit/receive data.

In Asynchronous (UART) mode, the USART communicates with other devices using two signals: transmit (TDX) and receive (RDX). In Synchronous mode, the USART communicates with other devices using three signals: transmit (TDX), receive (RDX), and clock (CKX); data bits are transferred synchronously with the CKX signal. Flow control is available in both Asynchronous and Synchronous modes through RTS/CTS signaling.

To reduce chip-level pin count, the USART interface signals can be shared with other on-chip functions through a General Purpose I/O (GPIO) Controller.

FEATURES

- Full-duplex double-buffered receiver/transmitter
- Synchronous operation using the CKX clock pin
- CKX can be generated internally or externally
- Asynchronous (UART) operation
- Programmable baud rate between CLK/2 and CLK/32768 baud
- Programmable frame formats
  - 7, 8, or 9 data bits
  - 1 or 2 stop bits
  - Odd, even, mark, space, or no parity
- Hardware support of parity-bit generation during transmission and parity-bit check during reception
- Software-controlled break transmission and detection
- Interrupt on transmit buffer empty, receive buffer full, receive error, and delta clear-to-send (flow control mode) conditions, each with a separate interrupt enable
- Internal diagnostic capability



FEATURES (CONTINUED)

- Automatic error detection
  - Parity error
  - Framing error
  - Data overrun error
- 9-bit Attention mode
- DMA support for transmit and receive with separate enables
- Hardware flow control functions
  - Clear-to-send (CTS)
  - Request-to-send (RTS)
- Wakeup pattern detection according to ISO14230/KWP2000
- Debug support: Freeze/suspend USART activity

INTERFACES

- AMBA 2.0 APB host interface
  - 8-bit read/write data buses
  - 10-bit address bus
- USART pins (CKX, TXD, RXD, CTS, RTS) through chip I/O pads (optionally through a GPIO Controller)
- DMA interface
  - One transmit DMA channel
  - One receive DMA channel
- Clock interface
  - APB clock for registers, DMA, interrupt functions, and for baud rate generation in Asynchronous mode
  - Baud rate clock input for Synchronous mode with external baud rate generation
  - Baud rate clock output for Synchronous mode with internal baud rate generation
- Interrupt interface (four interrupts)
- One asynchronous reset input
- Freeze/suspend interface
- DFT signals

HARDWARE CONFIGURATION OPTIONS

OPTION	RANGE	DEFAULT
Local clock gating for low-power operation	On or Off	Off
Clock synchronization for FPGA implementation	On or Off	Off
Wakeup detection logic	Included or Excluded	Excluded

GATE COUNT AND PERFORMANCE

Gate count and maximum frequency depend on synthesis tool and target technology. Example values for a typical 130-nm technology are:

- 2300 (NAND2 equivalent) gates
- 100 MHz (APB clock)

DELIVERABLES

The USART is available in Source and Encrypted products. The Source product is fully configurable and is delivered in plain text Verilog source code. The Encrypted product, which is available in the Core Store, offers limited configurability (default parameter values) and is delivered in encrypted source code. Both products include:

- Synthesizable Verilog source code (encrypted in the Encrypted product)
- Integration testbench and tests
- Documentation
- Automatic configuration through the IPextreme IP distribution and support portal
- Scripts for simulation and synthesis with support for common EDA tools

IPextreme

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