National Semiconductor
The Sight & Sound of Information

Building on the success of its CompactRISC™ architecture in embedded applications, National Semiconductor® is deploying the CR16CPlus in its CP3000 Communications Processor devices. In addition, National Semiconductor is now licensing its CR16CPlus IP to SoC developers through IPextreme under the product name CR16CP.

The CR16CP is an advanced version of the 16-bit CompactRISC architecture, extending earlier CR16 family products by using the industry-standard AMBA™ AHB bus system, providing full 32-bit data memory space, and supporting Nexus 5001 compliant on-chip debug capabilities.

National Semiconductor's CompactRISC architecture was specifically designed for embedded systems and delivers excellent code density, low power consumption, and small die area with the ability to tightly integrate on-chip acceleration, I/O and memory functions. The CompactRISC architecture has firmly established itself by filling a previously unmet need—those applications that require significant embedded performance, but cannot afford the size and cost overhead of full 32-bit RISC implementations. The architecture is enhanced with valuable controller features, like a variable length instruction set and direct bit manipulation to make it even more effective for embedded applications.

CR16 implementations have been proven in many National Semiconductor standard parts, such as their recent CP3000 Communications Processor family, which have proven valuable in a broad range of high-volume consumer communications applications. Other high volume applications for the CR16 include automotive airbag, telematics, infotainment and lighting systems, Bluetooth devices, wireless systems like European DECT phones, and personal computer peripherals and I/O.

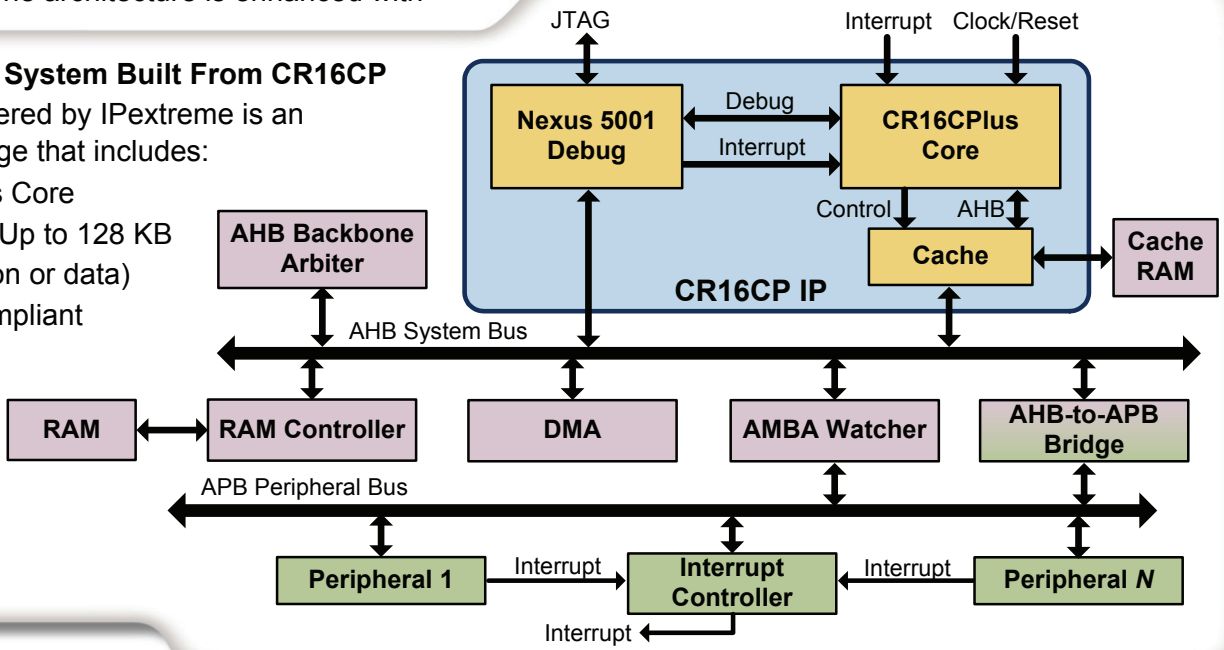
CR16CP FEATURES

The CR16CP implements a 16-bit embedded RISC controller with a Von-Neumann bus architecture. Instructions fetches and data transfers are performed through the AHB. A load-store unit decouples data transfers through the AHB and allows the CPU to continue program execution while the data is being transferred from/to memory (when there are no data dependencies).

Figure 1: Example System Built From CR16CP

The CR16CP IP offered by IPextreme is an integrated IP package that includes:

- The CR16CPlus Core
- Cache support: Up to 128 KB cache (instruction or data)
- Nexus 5001-compliant debug support



Controller Features

- 3-stage pipeline: Instruction Fetch (IF), Instruction Decode (ID), Execution (EX)
- Variable instruction length (16, 32, or 48 bits)
- Backward compatible with National Semiconductor CR16A and CR16B products
- Supervisor and User Modes for operating system (OS) support
- Single-cycle multiply (16x8)
- Low power achieved through compact design and dynamic clock gating

Registers

- 16 internal general purpose registers (GPRs)
- GPRS are 16 or 32 bits (two 16-bit GPRs can be concatenated to form a 32 bit GPR)
- 4 address registers
- Processor status register
- Configuration register
- Up to 11 debug control registers—depending on the number of debug channels (8 or 16)

Memory Organization

- 16 MB code memory (linear address space)
- 4 GB of data memory (linear address space)
- Supports data accesses on any alignment
- Instructions always 16-bit word aligned

Exceptions

- Non-maskable interrupt (NMI)
- Maskable interrupts (from up to 112 sources, managed by external interrupt controller)
- Traps

Stacks

- Interrupt Stack
- Supervisor Program Stack
- User Program Stack

ON-CHIP DEBUG SUPPORT

- Nexus 5001-compliant on-chip debug with 4-pin JTAG (IEEE149.1) for Nexus 5001 Class 1 support
- Up to 16 hardware breakpoints/watchpoints
- Instruction single-step
- Non-intrusive measurement of execution time (clock cycles) between two watchpoints
- Optional “freeze” of peripherals while CPU stopped in Debug Mode

CACHE SUPPORT

- Data or instruction cache supported
- Configurable cache size: 512 bytes–128 KB
- N-way set associative (N = 2, 4, or 8)
- L lines per way (L = 16, 32, 64, 128, or 256)
- W words per line (W = 4, 8, or 16)
- Cache can be locked and invalidated

IP DELIVERABLES

- Synthesizable Verilog source code
- Integration testbench
- Documentation
- IPextreme XPack packaging technology for design configuration, simulation, and synthesis with support for common EDA tools

PERIPHERAL LIBRARY

IPextreme also offers a rich set of AMBA peripherals ideal for use with the CR16CP. For more information, contact info@ip-extreme.com.

DEVELOPMENT TOOLS

Toolchain

National Semiconductor The Sight & Sound of Information — National CompactRISC CR16 Toolset

IAR SYSTEMS — IAR Systems CR16C Embedded Workbench

Debugger

iSYSTEM — iSYSTEM iC300, iONE, winIDEA

IPextreme

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