IEEE 1149.7 DTS Adapter

IPextreme

IEEE 1149.7 Debug/Test System (DTS) Adapter

PRODUCT BROCHURE

The DTS Adapter from IPextreme enables an existing IEEE 1149.1 debug test system (DTS) to take advantage of the advanced debug/test capabilities available with today's IEEE 1149.7-enabled semiconductor devices. Offered as a standalone product or as a companion product to our Compact JTAG IP for target systems, the DTS Adapter functions as a JTAG-to-Compact JTAG translator for the debug test system (DTS), supporting debug/test of IEEE 1149.7-compliant target systems.

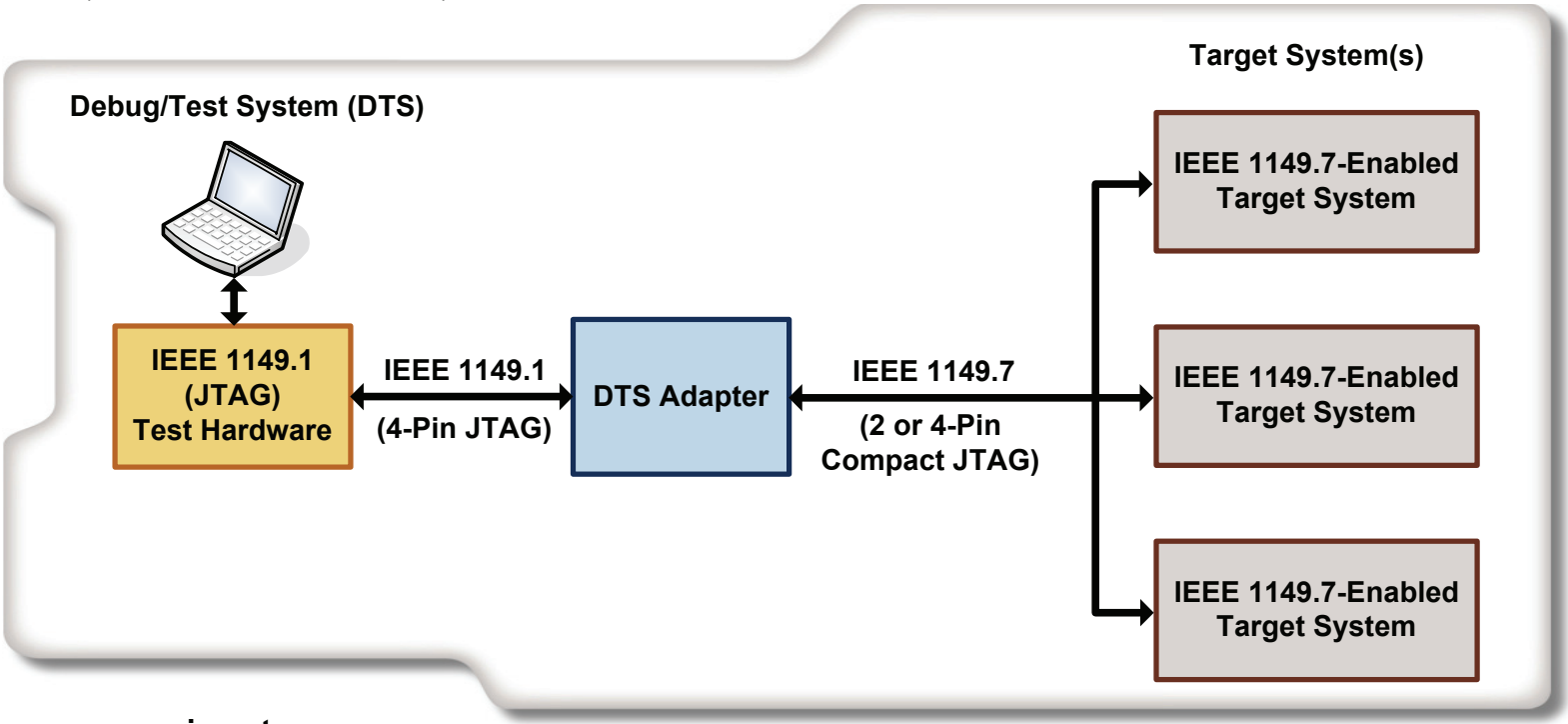
Easily implemented in FPGA or ASIC, the DTS Adapter provides the signal conversion and signal generation needed for existing IEEE 1149.1 (JTAG) test hardware to support IEEE 1149.7 features such as 2-pin operation, online/offline operation, Star topologies, and Scan Topology Training. With the DTS Adapter inserted into your existing IEEE 1149.1 debug/test hardware chain, you only need to upgrade your debug/test software to take full advantage of the advanced test/debug capabilities offered by IEEE 1149.7 enabled semiconductor devices.

DTS ADAPTER FEATURES

- IEEE 1149.1 interface to existing test/debug hardware
- IEEE 1149.7 interface to target system(s)
- Supports all IEEE 1149.7 scan formats
- Supports all IEEE 1149.7 scan topologies
- Automatic translation between IEEE 1149.1 and IEEE 1149.7 signalling for IEEE 1149.7 2-pin scan formats (MScan, OScan0-7, SScan0-3)
- Operation is transparent to IEEE 1149.1 test hardware, except for special functions that require programming the DTS Adapter
- Generation of IEEE 1149.7 Escape Sequences as commanded by test/debug software
- Control of TDI and TDO for IEEE 1149.7 Scan Topology Training
- Programmable control and data segments for IEEE 1149.7 segmented scan formats
- Proven interoperability with IPextreme Compact JTAG IP
- Safe connection/disconnection of target system(s)—DTS Adapter output signals are disabled (high-impedance) until enabled by DTS software
- Easily implemented in FPGA or ASIC
- Also useful in simulation as an IEEE 1149.7 stimulus generator

BENEFITS

- Extend the life of IEEE 1149.1 debug/test hardware for IEEE 1149.7 debug/test applications
- Take advantage of advanced IEEE 1194.7 debug/test features before IEEE 1149.7-enabled test hardware becomes widely available
- Accelerate design verification by using DTS Adapter as an IEEE 1149.7 bus transactor in simulation



DTS ADAPTER APPLICATIONS

IEEE 1149.7 offers several enhancements to the ubiquitous IEEE 1149.1 boundary scan technology, most notably:

- 2-pin operation
- Optimized scan formats to reduce protocol overhead and improve scan time
- Shorter scan paths through Star topologies and enhanced bypass capabilities
- Support for multiple TAP controllers on a single chip
- Support for reset and selection/deselection of target systems through the use of IEEE 1149.7 Escape Sequences

While most IEEE 1149.7 debug/test operations can be achieved through upgrades to IEEE 1149.1-based test software, there are some IEEE 1149.7 functions that require TCK/TMS/TDI/TDO pin-level control that most existing IEEE 1149.1 test hardware does not directly support. For example:

- In most existing IEEE 1149.1 test hardware, TMS is a uni-directional (output) signal sent to the target system. To support IEEE 1149.7 2-pin operation, TMS must be a bi-directional signal (named TMSC when operating in IEEE 1149.7 2-pin modes).
- IEEE 1149.7 Escape Sequences (used to reset target system test logic and to command target systems to the online or offline state) require the DTS hardware to hold the TCK pin at a high level, while toggling the TMS pin a specific number of times. Most existing IEEE 1149.1 test hardware does not provide the required pin-level control of TCK and TMS.
- IEEE 1149.7 Scan Topology Training, the procedure by which the DTS and target systems discover the test system topology (Series, Star-4, or Star-2), requires the DTS hardware to drive TDI and TDO with specific values. For most existing IEEE 1149.1 test hardware, TDO is an input-only pin and TDI may not have the necessary controllability.

Debug/test sytems that use IEEE 1149.1 test hardware to debug/test IEEE 1149.7-enabled devices are therefore ideal applications for the DTS Adapter. The DTS Adapter overcomes the limitations of IEEE 1149.1 test hardware with respect to IEEE 1149.7 functions in the following ways:

- The DTS Adapter supports bi-directional signalling on TMSC and automatically assembles/disassembles IEEE 1149.7 scan packets on TMSC whenever the DTS software selects a 2-pin scan format.
- When DTS software needs to generate an IEEE 1149.7 Escape Sequence, it commands the DTS Adapter to generate the Escape Sequence of the required type and the required time. The DTS Adapter then automatically generates the required signalling on TCK and TMS.
- For Scan Topology Training, the DTS commands the DTS Adapter to drive the required values on TDI and TDO.

For functions that require the DTS to explictly control the DTS Adapter—for example, enabling the target system interface, generating Escape Sequences, and controlling TDI and TDO for Scan Topology Training—the DTS writes the required commands to the DTS Adapter control registers directly through the IEEE 1149.1 interface. There is no additional or proprietary interface needed to program the DTS Adapter.

DTS ADAPTER DELIVERABLES

- Synthesizable Verilog source code
- Integration testbench and tests
- Documentation
- Scripts for simulation and synthesis with support for common EDA tools

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