M8051EW+

IPextreme

Mentor Graphics® Fast 8-Bit Microcontroller

PRODUCT BROCHURE

The M8051EW+ is the Mentor Graphics M8051W/EW high-performance version of the popular 8051 8-bit microcontroller. The M8051EW+ requires just 2 clocks per machine cycle instead of the 12 clocks per machine cycle required by industry standard 8051 devices. This allows the M8051EW+ to execute instructions six times faster than standard 8051 devices running at the same clock rate. Or, the M8051EW+ can run at one sixth the clock rate of a standard 8051 device and achieve equivalent performance at a fraction of the power consumption.

The 'On-Chip Instrumentation' (OCI) debug unit supplied with the Mentor Graphics M8051EW is available as a hardware configuration option with the M8051EW+. When used with the FS2 System Navigator for Mentor Graphics M8051EW Cores, the OCI debug unit supports advanced debug operations (start/stop/ single-step, breakpoints, and trace) through an IEEE 1149.1 (JTAG) interface. Because inclusion of the OCI debug unit is an M8051EW+ configuration option, you can include the OCI debug unit for prototyping and software development and exclude it from your production chips.

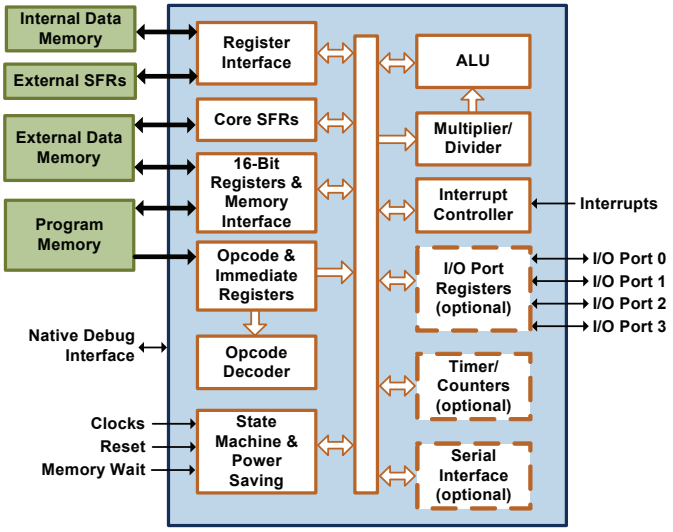
The M8051EW+ is a microcode-free design that is software compatible with industry standard 8051 devices, supporting both standard 8051 features and additional features corresponding to Intel 8051, 8031, 80C51BH, 80C31BH, and 87C51 devices and equivalent 8052 devices. The M8051EW+ is supported by several 3rd-party assemblers and C compilers including the 8051 Development Tools from Keil Software.

The M8051EW+ supports up to 1 MB of Program Memory and 1 MB of External Data Memory and can be configured to work with either synchronous or asynchronous memories, using either separate Program and External Data Memory interfaces or a single multiplexed memory interface. Support for slow memories is available through wait states.

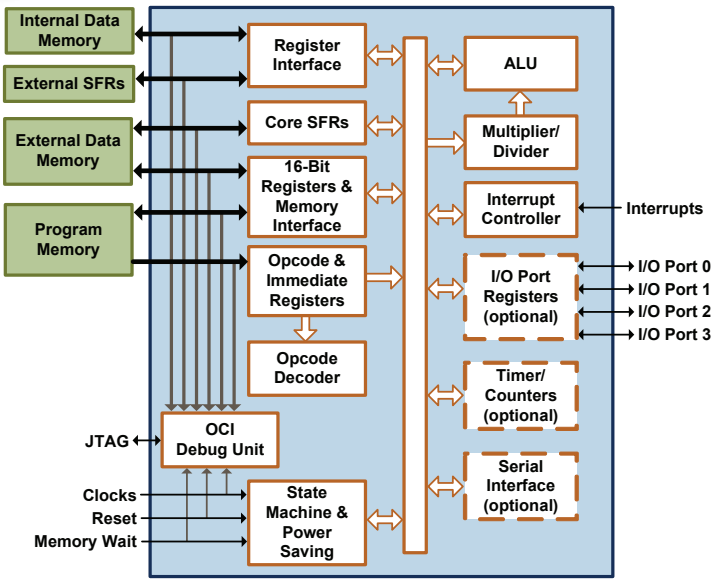
FEATURES

- 2 clocks per machine cycle
- Optional OCI debug unit
- Software compatible with Intel 8051, 8031, 87C51, and 8052 equivalents
- Up to 1 MB of External Data Memory
- Up to 1 MB of Program Memory
- Up to 256 bytes of Internal Data Memory
- Support for synchronous or asynchronous memories
- Wait state support for slow Program and External Data Memories
- M8051EW+-specific instruction (MOVC @(DPTR++), A) available for downloading program code to RAM
- Intel-compatible I/O Ports (optional)
- 2 or 3 16-bit timer/counters (optional)
- Full-duplex serial port (optional)
- 25-source, 2 or 4-level interrupt controller with choice of interrupt handling schemes

M8051EW+ without OCI



M8051EW+ with OCI



- 1, 2, 4, or 8 data pointers
- Support for up to 118 user-defined external special function registers (ESFRs), 11 of which may be bit-addressable
- Low-power support through Power-Down and Idle modes
- Fully synthesizable, scan ready design

DEDICATED MEMORY INTERFACES

The M8051EW+ uses dedicated interfaces for memory access instead of using I/O ports like standard 8051 devices. Therefore, all 32 of the M8051EW+ I/O pins are available for general-purpose I/O.

Internal Data Memory access (up to 256 bytes addressable) is through a dedicated interface to a user-implemented dual-port RAM. Through a configuration option, you can select either a synchronous or asynchronous Internal Data Memory interface.

External Data Memory (RAM) and Program Memory (ROM or RAM) can either use separate memory interfaces or share a single multiplexed memory interface. Both interfaces can be configured to support either synchronous or asynchronous memories. Up to 1 MB of External Data Memory and up to 1 MB of Program Memory are addressable using either a built-in memory extension scheme or standard code banking techniques supported by many 8051 assemblers and C compilers.

DEBUG SUPPORT

The M8051EW+ features an optional OCI debug unit with an IEEE 1149.1 (JTAG) interface to the external debug hardware. The OCI debug unit is intended to be used with the MIPS Technologies System Navigator for Mentor Graphics M8051EW Cores (formerly the In-Target System Analyzer (ISA) from First Silicon Solutions (FS2)) to provide a wide range of debugging features including breakpoints, reconstruction of execution history, and capture of Data Memory, Program Memory, and SFR accesses.

Excluding the OCI debug unit creates a smaller M8051EW+ design that still supports basic debug operations (start/stop/single-step) through a native debug interface.

LOW-POWER SUPPORT

The M8051EW+ uses separate clocks for the CPU, state machine, and peripherals to allow independent shutdown of the associated blocks in different power-down modes. In Idle mode, the clock to the CPU is stopped while the timer/counters, serial port, and interrupt controller continue to run using a half-speed clock. In Power-Down mode, all clocks are stopped.

ECOSYSTEM

Several widely used 8051 development tools are available from both commercial and open source providers. Providers offering tools that specifically support the M8051EW+ include Keil Software, IAR Systems, and MIPS Technologies. To compile the test programs used in the M8051EW+ integration testbenches, IPextreme uses both the 8051 Development Tools from Keil Software and the Small Device C Compiler (SDCC) available from http://sdcc.sourceforge.net.

GATE COUNTS

M8051EW+ gate count depends on configuration options, synthesis tool, and target technology. Example values at 100 MHz for a typical 90-nm technology are:

- 4K gates (NAND2 equivalent) for a minimum configuration (OCI, timers, serial port, and I/O Ports excluded)
- 8K gates for 8051 equivalent configuration with no OCI
- 8.5K gates for 8052 equivalent configuration with no OCI
- 14.5K gates for maximum configuration (including fully-configured OCI)

DELIVERABLES

- Verilog or VHDL source code
- Integration testbenches and tests
- Documentation
- Scripts for simulation and synthesis with support for common EDA tools

SUPPORT

IPextreme provides expert support for integration and use of the M8051EW+. Also available are M8051EW+ training and an FPGA-based demonstration platform that shows an example of how to implement the M8051EW+ in an FPGA and debug software using the System Navigator for Mentor Graphics M8051EW Cores.

IPextreme

IPextreme, Inc.
54 N. Central Ave.
Suite 204
Campbell, CA 95008
800-289-6412 (toll-free)
408-608-0421 (fax)
www.ip-extreme.com