



The Versatile Timer Unit from National Semiconductor contains four fully independent 16-bit timer subsystems. Each timer subsystem can operate either in dual 8-bit PWM configuration, as a single 16-bit PWM timer, or as a 16-bit counter with two input capture channels.

Each timer subsystem contains an 8-bit clock prescaler, a 16-bit up-counter, and two 16-bit registers. Each timer subsystem controls two I/O pins that either function as PWM outputs or capture inputs, depending on the associated timer subsystem's mode of operation:

- ▶ In 16-bit PWM mode, the TIOx pins function as PWM outputs.
- ▶ In dual 8-bit PWM mode, the 16-bit counter functions a two independent 8-bit counters. The TIOx pins function as PWM outputs.
- ▶ In capture mode, the TIOx pins function as capture inputs.
- ▶ In low-power mode, the clock is stopped. Read operations to the timer subsystem return the current register value; write operations are ignored.

There are four system-level interrupt requests, one for each timer subsystem. Each system-level interrupt request is controlled by four interrupt-pending flags, each of which offers a separate enable/disable bit.

CoreStore

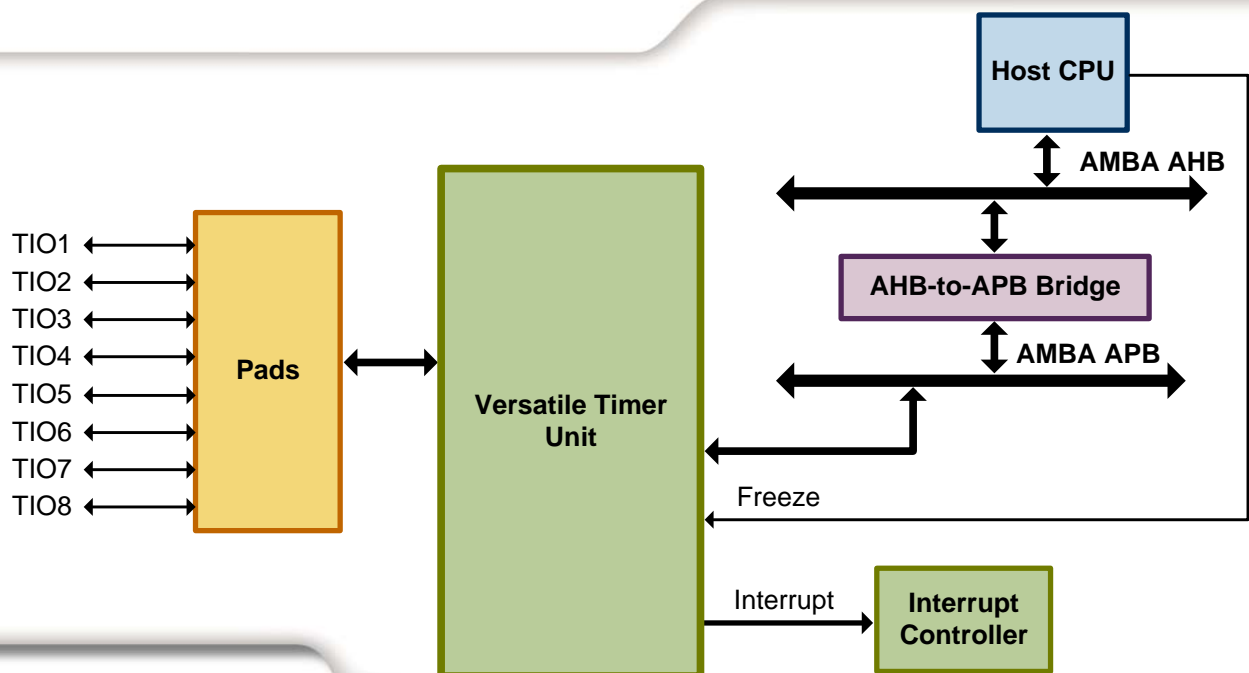
Famous IP • Available Online

The host interface of the Versatile Timer Unit complies with the AMBA 2 APB protocol. Control registers within the Versatile Timer Unit provide CPU control of timer mode, I/O pin functions and polarity, clock prescaling, PWM period and duty cycle, enabling/disabling/clearing interrupts, and starting/stopping the counters. Status registers indicate timer/capture values and interrupt status.

There are eight off-chip interface signals, TIO1–TIO8, two for each timer subsystem. To reduce chip-level pin count, the TIO1–TIO8 pins can be shared with other on-chip functions through a General Purpose I/O Controller.

FEATURES

- ▶ Software-configurable to offer up to:
 - Eight fully independent 8-bit PWM channels
 - Four fully independent 16-bit PWM channels
 - Eight 16-bit input capture channels
- ▶ Four timer subsystems, each of which contains:
 - One 16-bit counter
 - Two 16-bit capture/compare registers
 - One 8-bit fully programmable clock prescaler



FEATURES (CONTINUED)

- ▶ Each timer subsystem can operate in the following modes:
 - Low-power mode (all clocks are stopped)
 - Dual 8-bit PWM mode
 - 16-bit PWM mode
 - Dual 16-bit input capture mode
- ▶ Eight I/O pins, each of which can function either as:
 - PWM output with programmable output polarity, or
 - Capture input with programmable event detection and timer reset
- ▶ Flexible interrupt scheme with:
 - Four separate interrupt requests
 - 16 interrupt sources, each with a separate interrupt-pending flag and interrupt-enable bit
- ▶ Debug support: Freeze or suspend Versatile Timer Unit activity

INTERFACES

- AMBA 2 APB host interface
 - 16-bit read/write data buses
 - 10-bit address bus
- TIOx pins through chip I/O pads (optionally through a General Purpose I/O Controller)
- Clock interface – APB clock for registers, interrupt functions, and timer clock source
- Interrupt interface (one interrupt signal for each timer subsystem, plus combined interrupt)
- One asynchronous reset input
- Freeze/suspend interface
- DFT signals

HARDWARE CONFIGURATION OPTIONS

OPTION	RANGE	DEFAULT
Local clock gating for low-power operation	On or Off	Off

GATE COUNT AND PERFORMANCE

Gate count and maximum frequency depend on synthesis tool and target technology. Example values for a typical 130-nm technology are:

- 7000 (NAND2 equivalent) gates
- 100 MHz (APB clock)

DELIVERABLES

The Versatile Timer Unit is available in Source and Encrypted products. The Source product is fully configurable and is delivered in plain text Verilog source code. The Encrypted product, which is available in the Core Store, offers limited configurability (default parameter values) and is delivered in encrypted source code. Both products include:

- Synthesizable Verilog source code (encrypted in the Encrypted product)
- Integration testbench and tests
- Documentation
- Automatic configuration through the IPExtreme IP distribution and support portal
- Scripts for simulation and synthesis with support for common EDA tools

IPextreme

IPextreme, Inc.

307 Orchard City Drive

Suite 202

Campbell, CA 95008

800-289-6412 (toll-free)

408-608-0421 (fax)

www.ip-extreme.com

© Copyright 2008, IPextreme. All rights reserved. IPextreme is a registered trademark and XPack is a trademark of IPextreme, Inc. National Semiconductor is a registered trademark of National Semiconductor Corporation. All other trademarks are the property of their respective owners.

CoreStore

Visit our IP marketplace featuring famous IP from leading semiconductor companies.



www.ip-extreme.com/corestore