CFV2SPPC1

IPextreme

Freescale™ ColdFire® V2 Core & SPP C1

PRODUCT BROCHURE

The ColdFire V2 Core & Standard Product Platform C1 (CFV2SPPC1) combines the ColdFire V2 Core with an AMBA 2 AHB Crossbar Switch and Peripheral Bus Bridge, and a small set of commonly needed peripherals to create a bare-bones ColdFire V2 processor subsystem. Top-level AHB and APB interfaces make it easy for you to add your own AHB masters and slaves and APB peripherals and create your own custom ColdFire V2 device. With the CFV2SPPC1, you get:

- A fully synthesizable implementation of the popular ColdFire architecture
- Reliability—from processor and subsystem IP already deployed in millions of embedded systems worldwide
- Rapid time-to-market—in just a few hours you can be developing software on your own FPGA implementation of the CFV2SPPC1

COLDFIRE V2 CORE

The ColdFire V2 Core is a low-power, low-area, 32-bit processor core with single-cycle-access local SRAM and ROM, and a direct-mapped cache that can be configured as instruction cache, data cache, or split instruction/data cache. The ColdFire V2 Core delivers over 250 DMIPS of performance at 240 MHz and includes an enhanced MAC (EMAC) unit for DSP-like functions and faster execution of multiply instructions.

Like all ColdFire architecture processors, the ColdFire V2 Core features a variable-length instruction set for maximum code density, industry-standard AMBA 2 AHB system bus interface for rapid system integration, and a wide selection of development tools, operating systems, drivers, and libraries from both commercial and open source providers.

STANDARD PERIPHERALS AND INTERCONNECT

The CFV2SPPC1 includes the ColdFire V2 Core, plus the AHB/APB infrastructure and fully-integrated peripherals shown in Figure 1. The AHB Crossbar Switch provides the system interconnect, supporting simultaneous transfers between multiple AHB masters and slaves, including externally-connected AHB masters and slaves.

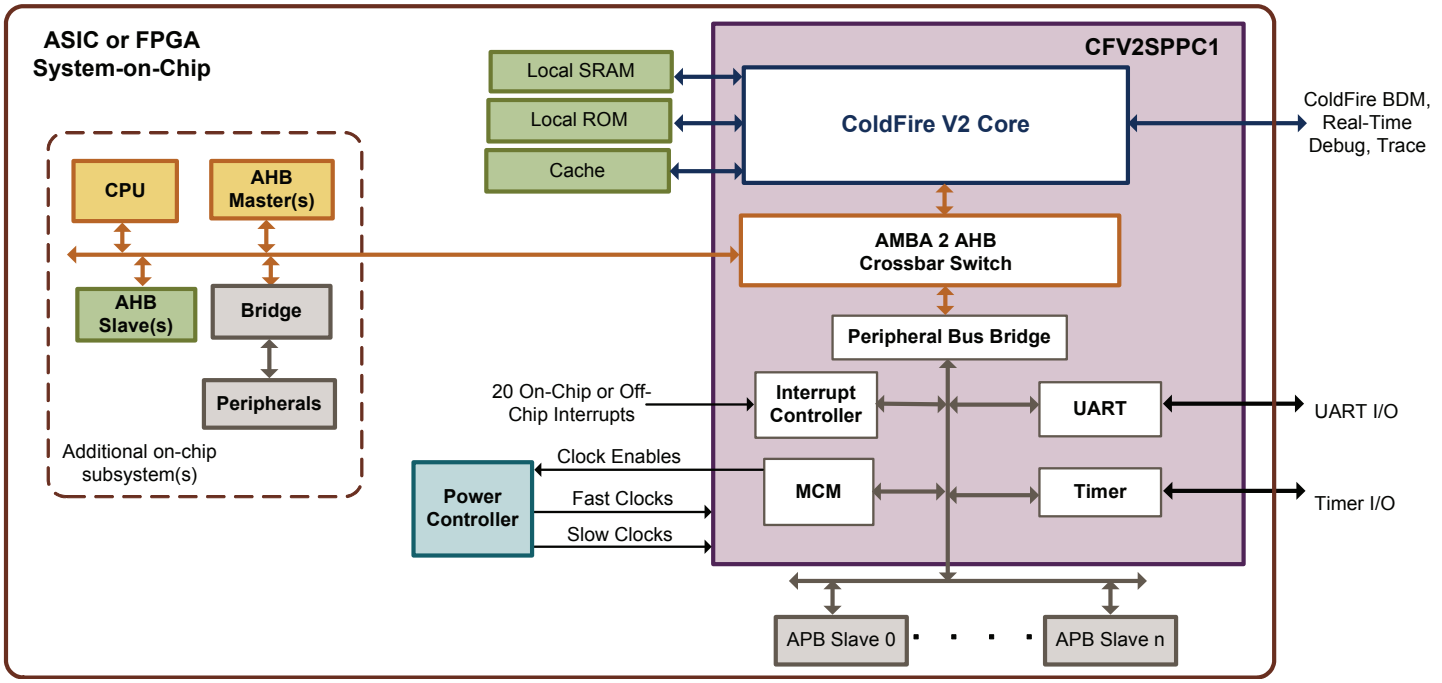
Variations of the CFV2SPPC1 with different combinations of on-board peripherals are also available. For example, you can add more peripherals, such as a Fast Ethernet Controller, or omit peripherals that you don't need to reduce system gate count.

PERIPHERALS FEATURES

On-board peripherals and their features include:

- Interrupt Controller
  - 64 programmable interrupt sources, 20 of which are available for external interrupts
  - Unique vector for each interrupt source
  - Support for low-power mode wake-up
- UART
  - Programmable clock source, data formats, and modes (normal/loopback)
  - Error detection
  - Four maskable interrupt conditions
- Timer
  - Programmable clock source
  - Programmable prescaler
  - Programmable interrupt or DMA request upon timer event

Figure 1: Example SoC Using CFV2SPPC1



- Miscellaneous Control Module (MCM)
  - Software watchdog timer
  - Reset status, low-power mode control, and core fault status registers

POWER SAVING FEATURES

The CFV2SPPC1 features software-controlled shutdown of selected clocks to support a variety of chip-level low-power modes:

- Independent shutdown of selected peripheral clocks
- Shutdown of the ColdFire V2 Core CPU clock in response to a ColdFire STOP instruction

DEBUG SUPPORT

The CFV2SPPC1 supports ColdFire Debug Architecture Revision B+, including:

- Background Debug Mode (BDM)
- Real-Time Trace (RTT)
- Real-Time Debug (RTD)

DEVELOPMENT SUPPORT

The ColdFire architecture is supported by a vast assortment of development systems/tools and run-time software including libraries, stacks, drivers, and operating systems from providers such as Freescale, Green Hills Software, Wind River Systems, CodeSourcery, and many more. For example, the Sourcery G++ tool suite from www.codesourcery.com supports ColdFire V2 targets and can be used to develop new code or to retarget ColdFire V1 programs to ColdFire V2 devices. A free version of the GNU compiler supporting ColdFire V2 targets is also available from www.gnu.org.

Freescale offers development boards, software, and CodeWarrior Development Tools (including a free version supporting the ColdFire V2 architecture). In addition, there are several operating systems supporting the ColdFire V2 architecture, including uClinux and several RTOS's, such as the MQX RTOS from Embedded Access, Inc.

GATE COUNT/MAXIMUM FREQUENCY

The CFV2SPPC1 gate count depends on synthesis tool and target technology. Approximate gate count for a typical 90-nm technology is 85K gates. The maximum CPU frequency for the same target technology is approximately 200 MHz. In 65-nm technology, the maximum frequency is 240 MHz.

The CFV2SPPC1 achieves over 85 MHz in most FPGA devices and uses approximately 13,000 LUTs in an Altera Stratix III device. For a Stratix III EP3SL200F1152C2, that is just over 8% utilization.

DELIVERABLES

- Verilog source code
- Integration testbench and tests
- Documentation
- Scripts for simulation and synthesis with commonly-used EDA tools

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