MP2VDSD

IPextreme

MPEG2 Video Decoder IP Core

PRODUCT BROCHURE

PRODUCT DESCRIPTION

The MP2VDSD is a standard-definition MPEG-2 video decoder compliant with the Main Profile @ Main Level (MP@ML) functionality specified by the ISO/IEC 13818-1 and ISO/IEC 13818-2 standards. The MP2VDSD also supports MPEG1 constrained parameter set bitstreams and MPEG1 bitstreams that are not constrained parameter set bitstreams as long as the parameter values do not exceed the corresponding MPEG2 MP@ML values. The MP2VDSD meets the constraints of the ATSC/Grand Alliance and DVB format specifications regarding Main Level.

The MP2VDSD is well designed for multimedia system-on-chip (SoC) products such as the example SoC shown in the figure below, which also includes (S)DRAM and controller, audio decoder, pixel engine, and host processor modules.

The MP2VDSD can be started on a picture basis or for an entire stream, meaning it can decode all layers of an MPEG video bitstream down to and including the picture layer.

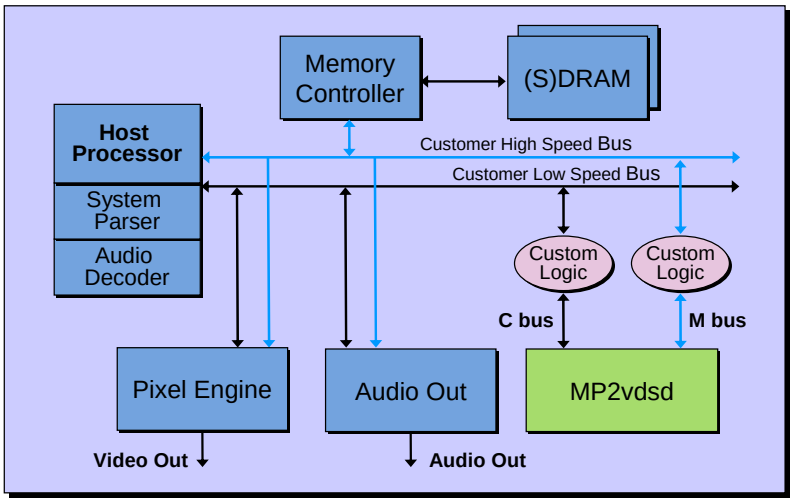
FEATURES

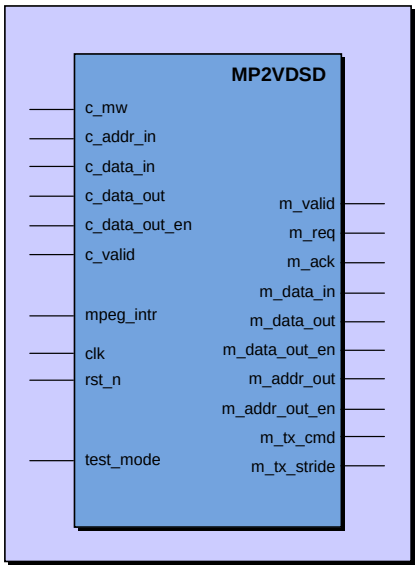
- Supports ISO/IEC 1172 (MPEG1) and ISO/IEC 13818 (MPEG2) bitstreams
- Decodes MPEG2 MP@ML
- Supports 15 Mbps input bit rate
- Supports 24, 25, and 29.97 MHz frame rates
- Supports either 525 lines at 60 Hz or 625 lines at 50 Hz SD television system
- Supports frame sizes 720x480 at 30 frames/s or 720x576 up to 25 frames/s
- Supports progressive and interlaced source material (for interlaced material, both field and frame coding are implemented)
- Easily controlled by commands through a control bus interface to start tasks or stall the MP2VDSD
- Controllable for letter box, pan & scan, and 3:2 pull down support
- Easily integrated into system-on-chip using shared memory
- Error detection and error recovery
- User Data extraction
- Supports ES video streams
- Minimal CPU intrusion, required only between picture data

APPLICATIONS

- DVB/ATSC decoders for SDTV
- DVD/VCD/SVCD
- Digital set-top box

System Block & Interface Diagrams





TECHNICAL DATA

- System clock frequency greater than 40 MHz (for real time decoding of MPEG2 bitstreams at MP@ML)
- Approximately 13 Kbits of internal SRAM
- Less than 2 MB of external shared memory depending on the picture resolution

Figure 2 shows the internal structure of the MP2VDSD. The MP2VDSD is controllable by an external module such as a microprocessor through its control bus (C bus) interface. The MP2VDSD mapped registers include control, command, and status information (parameters extracted while parsing the video bitstreams).

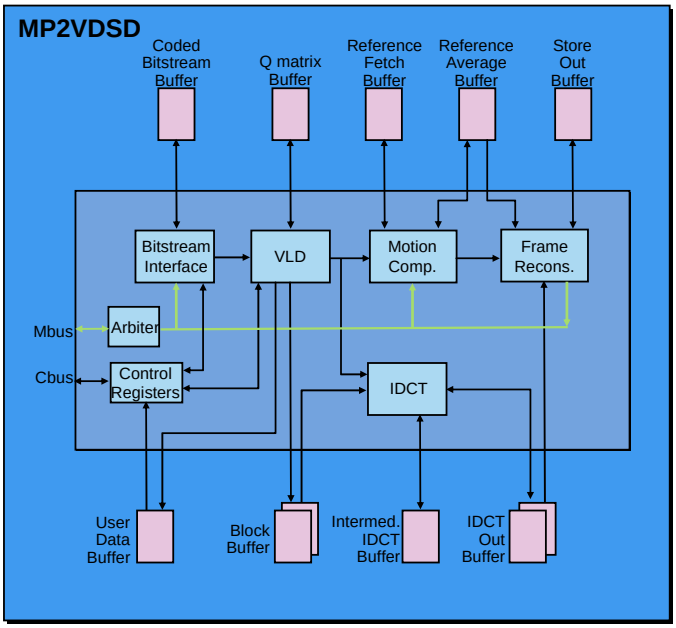


Figure 2: Functional Block Diagram

The host processor controls and reads status from the MP2VDSD through the mapped registers. The MP2VDSD, in turn:

- Receives parsing commands and control information written to the mapped registers
- Processes the video bitstreams or remains stalled accordingly
- Reports decoding status by updating its internal status mapped registers
- Sends an interrupt when the processing of the commands is completed or errors are encountered

This offers various levels of controllability allowing easy integration of the MP2VDSD into systems of various requirements.

The MP2VDSD assumes that the video input bitstreams are stored in the bitstream circular buffer in the shared memory by a host processor or other external module. Likewise, the MP2VDSD assumes that the decoded pictures are read by an external pixel engine and presented as a video stream. The pixel engine is in charge of letter box, pan & scan, 3:2 pull down, up and down scaling, filtering, and aspect ratio conversion (4/3 and 16/9). The pixel engine can be controlled by reading the MP2VDSD status registers, which provide adequate information for presentation and display modes according to the decoded bitstream.

THE CUSTOMER EXPERIENCE

The IPextreme® engineering team has been creating quality IP for a decade, such as the first fully synthesizable ARM processor, the Infineon C166S, MPEG decoders, and Bluetooth. Our engineers understand integration challenges and so rework and package the design for maximum ease of use. They will typically limit parameters to those most important, simplify interfaces, bundle software, supply suites that verify connectivity, and generally transfer just the necessary knowledge from the original designers.

All the IP we ship is packaged in our patent pending XPack , which maximizes ease of use by letting the integration engineers configure complex IP through an intelligent user interface that outputs the configuration and constraints files for common tools from Cadence, Mentor, and Synopsys. During the preparation and packaging of the IP our engineers learn enough about it to offer excellent support. IPextreme takes advantage of professional commercial IP delivery software systems and our engineers stick with the customer to ensure they successfully integrate IP purchased from us. See our website for more information on XPack.

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