ColdFire Family

IPextreme

Freescale™ ColdFire® Architecture IP

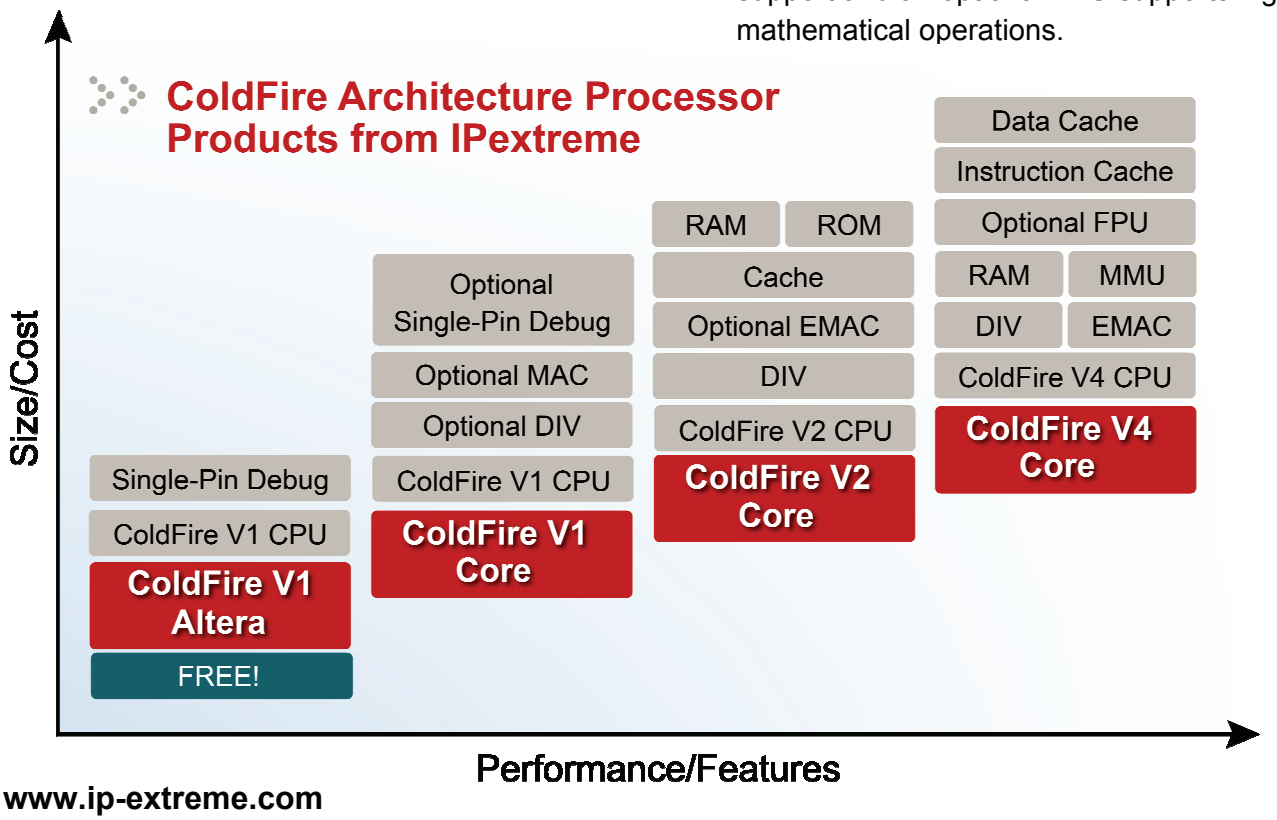
PRODUCT BROCHURE

IPextreme offers production-proven ColdFire architecture cores at a wide range of price/performance profiles for applications ranging from low-cost 8-bit to 32-bit migration to the high-performance 32-bit embedded systems. With features and performance comparable to Cortex-M series processors from ARM, Ltd., ColdFire cores from IPextreme enable embedded systems designers to:

- Select the 32-bit processor architecture best suited to their design requirements and preferred software development tools
- Choose the ColdFire V1, V2, or V4 architecture implementation that best matches their project's cost/area/power/performance objectives
- Build a complete subsystem around a selected ColdFire core using the same peripheral IP blocks implemented in Freescale ColdFire devices and supported by industry-proven software drivers
- Jump-start application software design with an industry-proven operating system adapted to the selected ColdFire core and subsystem peripherals

ColdFire architecture processors available from IPextreme include:

- ColdFire V1 Core – For low-cost/low-power applications and designs migrating from 8-bit to 32-bit processor architectures, the ColdFire V1 Core can achieve 276 DMIPS of performance and can use as few as 19K gates in a 65-nm process. The ColdFire V1 Core is available either as a fully synthesizable IP core or as a (free-of-charge) encrypted core for Altera Cyclone III FPGAs.
- ColdFire V2 Core – Using the same 4-stage CPU pipeline as the ColdFire V1 Core, the ColdFire V2 Core features more efficient system bus utilization through tightly-coupled local RAM, ROM, and cache. The enhanced MAC (EMAC) unit accelerates execution of DSP algorithms, enabling the ColdFire V2 Core to complete a 32x32 matrix multiply operation using fewer than ½ the CPU clock cycles required by a Cortex-M3 processor.
- ColdFire V4 Core – With up to 631 DMIPS of performance, the ColdFire V4 Core is suited to the more demanding embedded applications. A fully-integrated MMU provides full operating system support and an optional FPU supports high-precision mathematical operations.



COMMON INSTRUCTION SET

All three of the ColdFire cores implement the ColdFire Instruction Set Architecture (ISA) with additional instructions to support the special arithmetic hardware (DIV, MAC, EMAC, FPU) available with the synthesizable ColdFire cores. ColdFire instructions are variable in length (16, 32, or 48 bits) to maximize code density, enabling a smaller code memory footprint with no performance penalty.

COMMON HARDWARE INTERFACES

All of the ColdFire architecture cores from IPextreme are fully synthesizable, testable, and feature straightforward industry-standard interfaces for rapid, error-free integration into any ASIC or FPGA design:

- AMBA 2 AHB system bus interface (Altera AVALON bus for the V1 ColdFire Altera product)
- Standard synchronous local memory interfaces
- Simple clock and reset implementation
- ColdFire Background Debug Mode (BDM) debug interface supported by several development tool providers

BEST-IN-CLASS ECOSYSTEM

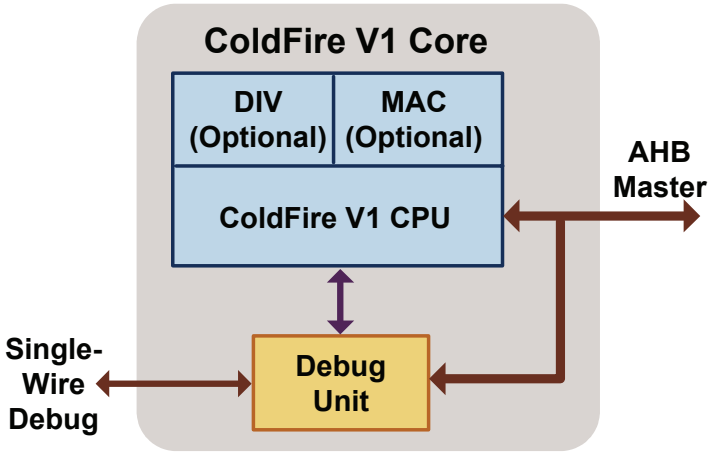
Compilers/ Assemblers/ Debuggers/IDE	Freescale, Green Hills, Wind River, CodeSourcery, Express Logic, FORTH, GNU, P&E, IAR, iSYSTEM, Netburner, Lauterbach
BDM Cables	Freescale, Green Hills, Wind River, Express Logic, P&E, IAR, iSYSTEM
Development Boards	Freescale, P&E, Netburner, IAR, Intec Automation
Drivers and Libraries	Freescale, Embedded Access, Express Logic, Green Hills, InterNiche, CodeSourcery,
Operating Systems	Express Logic, Embedded Access, Wind River, Micro Digital, Blunk Microsystems, RTEMS, CMX Systems, Quadros, Segger, Linux, uClinux

The entire ColdFire Family is supported by a world-class ecosystem of development platforms and toolchains developed and improved over the 15+ year history of the 68K/ColdFire architecture. Also available are operating systems and software stacks/drivers/middleware for a variety of connectivity/networking, file system, security, and graphics applications.

Products are available at a variety of price points ranging from free/complimentary tools offered by open source and commercial providers to highly-integrated premium tools suites.

COLDFIRE V1 CORE

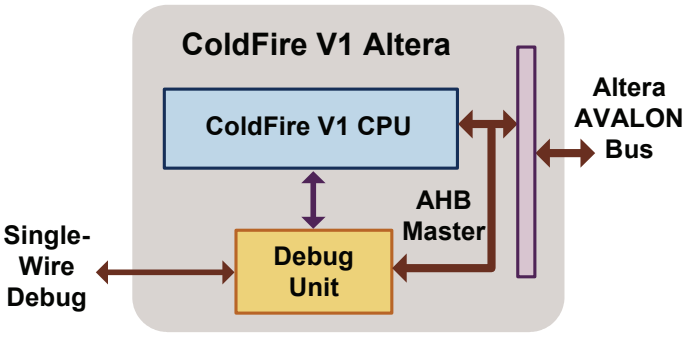
The ColdFire V1 Core is a fully synthesizable ColdFire V1 solution for ASIC or FPGA implementation. The ColdFire V1 Core features the ColdFire V1 CPU with optional hardware divider (DIV) and MAC units. Debug support including BDM, trace, and Real-Time Debug (RTD) is through a single-wire debug interface.



COLDFIRE V1 ALTERA

Available free-of-charge to integrate into Altera Cyclone III FPGAs, the ColdFire V1 Altera product features the ColdFire V1 CPU and the same debug features and single-pin debug interface as the ColdFire V1 Core. The ColdFire V1 Altera product is delivered as encrypted RTL for use with Altera Cyclone III FPGAs and has no associated IP licensing or royalty fees.

For the ColdFire V1 Altera product, the ColdFire V1 AHB system bus is adapted to Altera's AVALON bus. The ColdFire V1 Altera product is fully with the Altera Qsys and Quartus II tools.

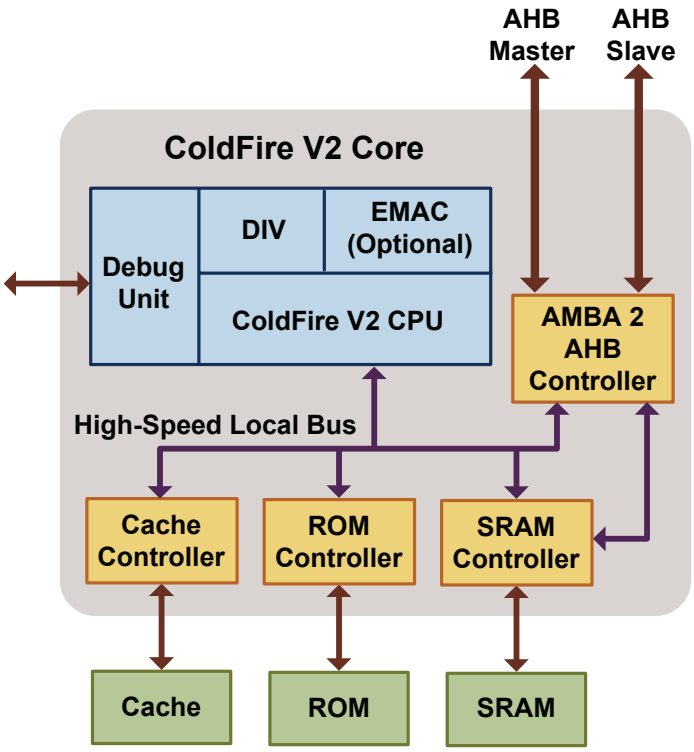


COLDFIRE V2 CORE

The ColdFire V1 and V2 Cores use the same 4-stage processor pipeline, consisting of a 2-stage instruction fetch pipeline and a 2-stage operand execution pipeline, separated by a FIFO instruction buffer.

The ColdFire V2 Core offers higher performance through tightly-coupled, zero-wait-state local memories (RAM, ROM, and cache of user-defined sizes) and the ability to run the CPU at 1x, 2x, 3x, or 4x the system bus (AHB) frequency. An AHB slave port allows external AHB masters to access the local RAM.

Through pin-strapping options, you can select either local SRAM, local ROM, or system memory as the boot device.



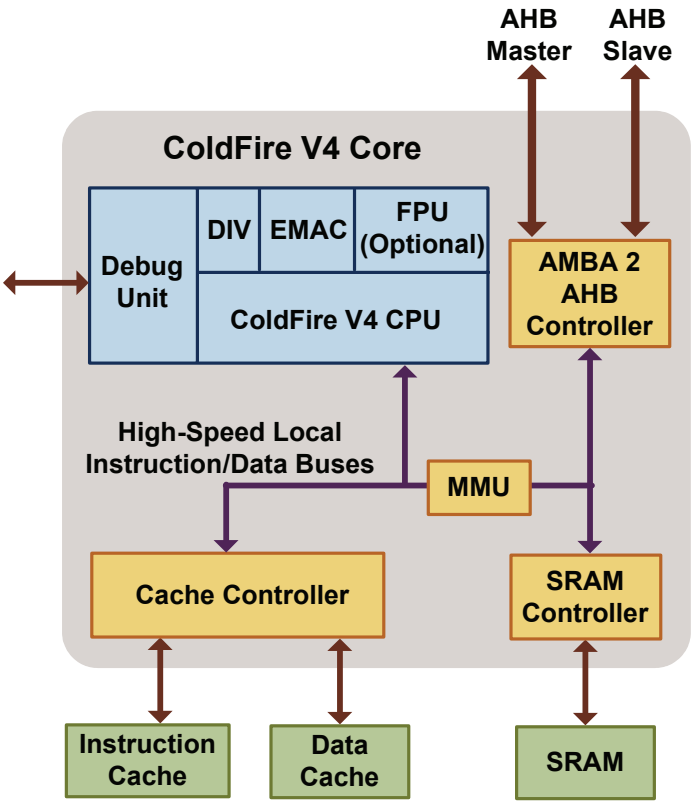
An included hardware divide (DIV) unit and optional enhanced MAC (EMAC) unit accelerate execution of multiply/divide operations and provide support for additional EMAC instructions, reducing the need for a co-processor in DSP-intensive applications.

Debug support is through a three-wire serial interface for BDM and RTD with an additional 8-bit parallel interface for real-time trace (RTT).

COLDFIRE V4 CORE

The ColdFire V4 Core is a high-performance implementation of the ColdFire architecture with a 9-stage CPU pipeline and Harvard local bus structure for accesses to independent instruction and data caches and tightly-coupled local SRAM. The 9-stage pipeline supports dual-issue of certain heavily used instruction constructs (such as MOVE) for limited superscalar operation.

With 1.54 DMIPS/MHz of performance and a maximum frequency of 410 MHz in a 65-nm process, the ColdFire V4 Core offers up to 631 DMIPS, more DMIPS than any Cortex-M series processor. Like the ColdFire V2 Core, the ColdFire V4 CPU can run at 1x, 2x, 3x, or 4x the system bus frequency.



SUMMARY OF COLDFIRE V1, V2, V4 FEATURES

Feature	ColdFire V1 Altera	ColdFire V1 Core	ColdFire V2 Core	ColdFire V4 Core
DMIPS/MHz	1.15	1.15	1.05	1.54
Special Arithmetic Hardware (and supported ISA extensions)	None	Optional DIV Optional MAC	DIV Optional EMAC	DIV, EMAC Optional FPU
Local RAM/ROM	—	—	RAM & ROM	RAM
Cache	—	—	Single direct-mapped cache up to 32 KB; used for instruction, data, or both instruction and data	Independent instruction/data caches up to 32 KB each; four-way set-associative
MMU	—	—	—	Yes
Supported implementations	Cyclone III FPGA	FPGA or ASIC	FPGA or ASIC	FPGA or ASIC
Supported CPU/system bus clock ratios	1:1	1:1	1:1, 2:1, 3:1, 4:1	1:1, 2:1, 3:1, 4:1
System Bus Interface	Altera AVALON Bus (24-bit address, 32-bit data)	AMBA 2 AHB (24-bit address, 32-bit data)	AMBA 2 AHB (32-bit address, 32-bit data)	AMBA 2 AHB (32-bit address, 32-bit data)
Debug Support	Single-pin BDM, trace, RTD	Optional single-pin BDM, trace, RTD, on-chip trace buffer	BDM, RTT, RTD	BDM, RTT, RTD, on-chip trace buffer

The ColdFire V4 Core also includes an MMU and optional FPU. Debug support is through the same BDM interface as the ColdFire V2 Core and includes BDM, RTT, RTD, plus an on-chip 128-entry trace buffer for low-cost trace through the three-wire BDM serial interface.

DELIVERABLES

Each of the synthesizable ColdFire V1, V2, and V4 products is delivered in technology-independent RTL source code format (Verilog) and also includes an integration testbench, example test/demonstration programs, documentation, and scripts for simulation and synthesis with commonly-used EDA tools supporting both ASIC and FPGA flows.

The ColdFire V1 Altera product is delivered as encrypted RTL for implementation in Cyclone III FPGAs and is fully compatible with Altera's Qsys and Quartus II tools.

EVALUATE COLDFIRE FOR YOUR NEXT DESIGN

For product details and pricing information, or to evaluate one or more ColdFire cores for your next SoC design, contact IPextreme at info@ip-extreme.com.

IPextreme

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