CFV4SPPC1

IPextreme

Freescale™ ColdFire® V4 Core & SPP C1

PRODUCT BROCHURE

The ColdFire V4 Core & Standard Product Platform (SPP) C1 (CFV4SPPC1) combines the ColdFire V4 Core with industry-proven platform peripherals to form a complete high-performance microcontroller subsystem supported by a vast ecosystem of development tools and runtime software. With the CFV4SPPC1, you get:

- Performance—over 500 DMIPS at 345 MHz
- Reliability—from processor and peripheral IP already deployed in millions of embedded systems worldwide
- Rapid time-to-market—in just a few hours you can be developing software on your own FPGA implementation of the CFV4SPPC1

COLDFIRE V4 PERFORMANCE

The ColdFire V4 Core is a high-performance implementation of the ColdFire architecture with 1.54 DMIPS/MHz instruction throughput and high-speed Harvard local buses with tightly-coupled instruction and data caches and local SRAM. The ColdFire V4 Core also features an MMU for full operating system support plus special arithmetic hardware including a divider and enhanced MAC (EMAC) for faster execution of DSP algorithms, and an FPU for single and double-precision floating-point calculations.

Like all ColdFire architecture processors, the ColdFire V4 Core features a variable-length instruction set for maximum code density, industry-standard AMBA 2 AHB system bus interface for rapid system integration, and a wide selection of development tools, operating systems, drivers, and libraries from both commercial and open source providers.

STANDARD PERIPHERALS AND INTERCONNECT

The CFV4SPPC1 includes ColdFire V4 Core, plus the fully-integrated peripherals shown in Figure 1, implementing functions commonly needed for embedded systems including interrupt control, DMA, timers, and various serial interfaces. An AMBA 2 AHB Crossbar Switch provides the system interconnect, supporting simultaneous AHB transfers between multiple masters and slaves, including externally-connected AHB masters and slaves.

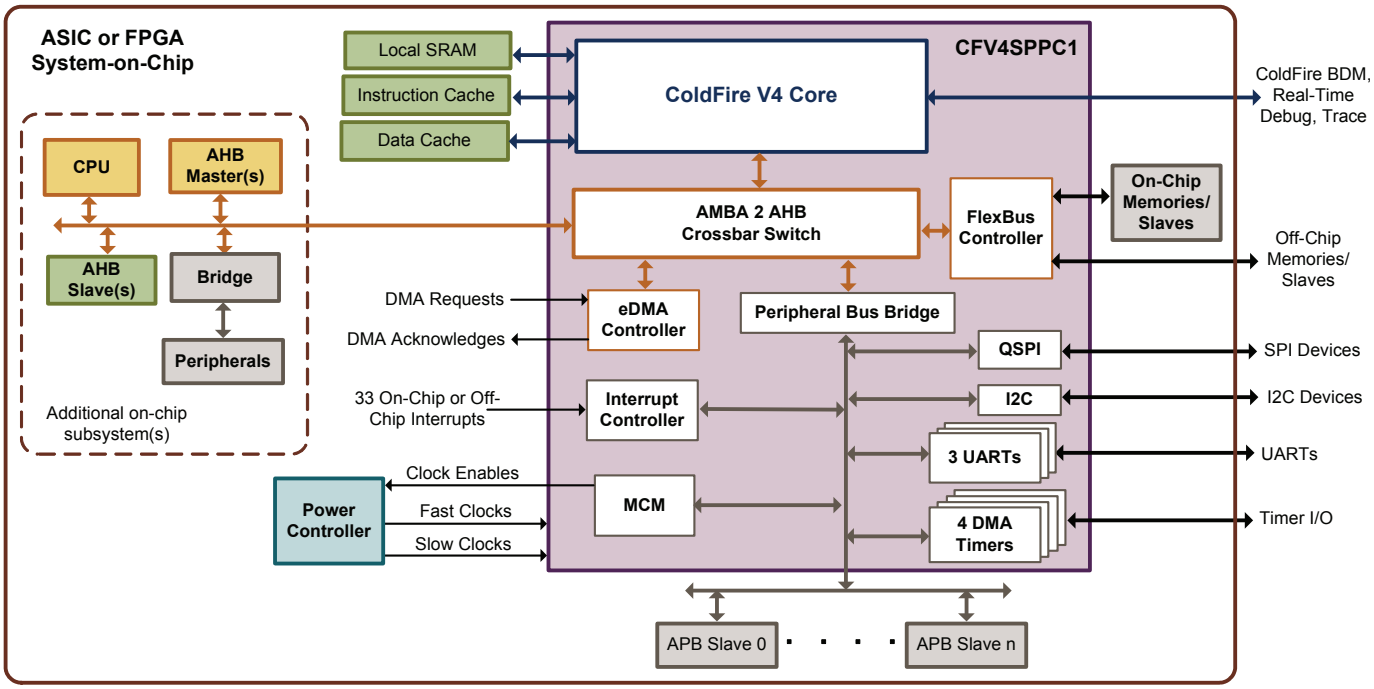
Variations of the CFV4SPPC1 with different combinations of on-board peripherals are also available. For example, you can add one or two Ethernet Controllers or you can choose to omit one or more of peripherals to reduce system gate count.

PERIPHERALS FEATURES

On-board peripherals and their features include:

- FlexBus Controller
  - Connects up to 6 on-chip or off-chip memories/devices
  - Independently programmable transfer characteristics for each device (wait states, address setup/hold)
- Enhanced DMA (eDMA) Controller
  - 16 independently programmable DMA channels
  - Programmable channel arbitration modes
  - Support for channel linking and scatter/gather operation
- Interrupt Controller
  - 64 programmable interrupt sources, 33 of which are available for external interrupts
  - Unique vector for each interrupt source
  - Support for low-power mode wake-up

Figure 1: Example SoC Using CFV4SPPC1



- Queued SPI (QSPI) module
  - Programmable queue for up to 16 SPI transfers
  - Four chip-select lines for up to 16 devices
  - Programmable baud rate, before-and-after transfer delays, clock phase and polarity
- I2C interface module
  - Support for the original Philips I2C bus protocol
  - Support for baud rates up to 3.4 Mbps
- 3 UARTS
  - Programmable clock source, data formats, and modes (normal/loopback)
  - Error detection
  - Four maskable interrupt conditions
- 4 DMA Timer modules
  - Programmable clock source
  - Programmable prescaler
  - Programmable interrupt or DMA request upon timer event
- Miscellaneous Control Module (MCM)
  - Software watchdog timer
  - Reset status, low-power mode control, and core fault status registers

POWER SAVING FEATURES

The CFV4SPPC1 features software-controlled shutdown of selected clocks to support a variety of chip-level low-power modes:

- Independent shutdown of selected peripheral clocks
- Shutdown of the ColdFire V4 Core CPU clock in response to a ColdFire STOP instruction; the ColdFire V4 Core local SRAM Controller clock may optionally be kept running in STOP mode to support access to local SRAM from external AHB masters

DEBUG SUPPORT

The CFV4SPPC1 supports ColdFire Debug Architecture Revision D+, including:

- Background Debug Mode (BDM)
- Real-Time Trace (RTT)
- Real-Time Debug (RTD)
- On-chip, 128-entry trace buffer for low-cost trace over BDM

DEVELOPMENT SUPPORT

The ColdFire architecture is supported by a vast assortment of development systems/tools and run-time software including libraries, stacks, drivers, and operating systems from providers such as Freescale, Green Hills Software, Wind River Systems, CodeSourcery, and many more. For example, the Sourcery G++ tool suite from www.codesourcery.com supports ColdFire V4 targets and can be used to develop new code or to retarget ColdFire V1/V2 programs to ColdFire V4 devices. A free version of the GNU compiler supporting ColdFire V4 targets is also available from www.gnu.org.

Freescale offers development boards, software, and CodeWarrior Development Tools (including a free version supporting the ColdFire V4 architecture). In addition, there are several operating systems supporting the ColdFire V4 architecture, including Linux/uClinux and several RTOS's, such as the MQX RTOS from Embedded Access, Inc.

GATE COUNT/MAXIMUM FREQUENCY

The CFV4SPPC1 gate count depends on synthesis tool and target technology. Approximate gate count for a typical 90-nm technology is 370K gates. The maximum CPU frequency for the same target technology is approximately 345 MHz.

The CFV4SPPC1 achieves over 100 MHz in most FPGA devices and uses approximately 47,000 LUTs in an Altera Stratix III device. For a Stratix III EP3SL200F1152C2, that is less than 30% utilization.

DELIVERABLES

- Verilog source code
- Integration testbench and tests
- Documentation
- Scripts for simulation and synthesis with commonly-used EDA tools

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