MICROWIRE/SPI

IPextreme

National Semiconductor® MICROWIRE/SPI Controller

PRODUCT BROCHURE

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The MICROWIRE/SPI Controller is a synchronous serial communication controller compatible with all MICROWIRE peripherals and SPI peripherals. It is the same MICROWIRE/SPI Controller proven in high-volume controllers from National Semiconductor and is available exclusively from IPextreme as synthesizable IP.

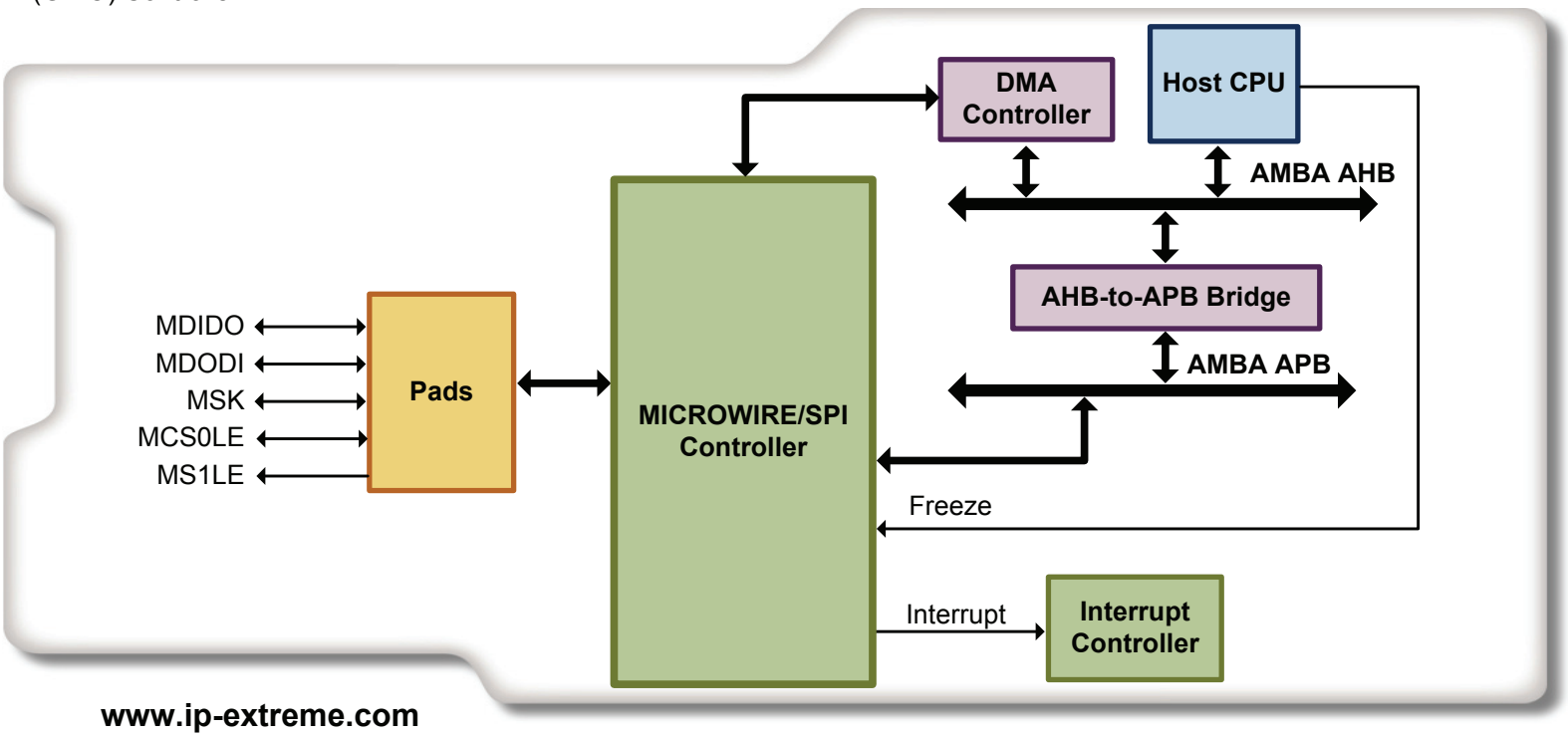
Originally developed to reduce the number of connections and, therefore, the cost of communicating with peripherals, the MICROWIRE/SPI protocol allows several devices to be connected on one three-wire system. At any given time, one device operates as the master while all other devices operate as slaves. The three-wire system includes two bidirectional serial transmit/receive signals (MDIDO: master mode data in/slave mode data out; and MDODI: master mode data out/slave mode data in). The serial clock (MSK) is driven by the current master.

The MICROWIRE/SPI Controller also implements slave select signals (MSC0LE and MS1LE at the chip-level I/O) to efficiently enable the target slave device. MSC0LE is a slave select output signal in master mode and a slave select input signal in slave mode; MS1LE is a slave select output signal used only in master mode. To reduce chip-level pin count, the MICROWIRE/SPI interface signals can be shared with other on-chip functions through a General Purpose I/O (GPIO) Controller.

The host interface of the MICROWIRE/SPI Controller complies with the AMBA 2.0 APB protocol. Control registers within the MICROWIRE/SPI Controller provide CPU control of master or slave mode, 8 or 16-bit data transfers, clock mode, shift clock frequency in master mode, slave select signal polarity, and enabling/disabling interrupts. Status registers indicate shift register busy, read buffer full, and receive overrun. In addition, there are registers that hold the transmit/receive data.

FEATURES

- Supports master and slave operation
- 8 or 16-bit transfers
- 16-bit read buffer
- Programmable shift clock frequency in master mode
- One slave select input for slave mode
- Two slave select outputs for master mode
- Programmable echo back operation in slave mode
- Flags for busy, read buffer full, and receive overrun with separate interrupt enables
- DMA support for transmit and receive with separate enables



FEATURES (CONTINUED)

- Programmable clock modes
  - Normal mode: Shift transmit data out on MSK rising edge; sample receive data on MSK falling edge
  - Alternate mode: Shift transmit data out on MSK falling edge; sample receive data on MSK rising edge
- MSK can be high or low when idle
- Debug support: Freeze or suspend MICROWIRE/SPI Controller activity

INTERFACES

- AMBA 2.0 APB host interface
  - 16-bit read/write data buses
  - 10-bit address bus
- MICROWIRE/SPI pins (MDIDO, MDODI, MSK, MSC0LE, and MS1LE) through chip I/O pads (optionally through a GPIO Controller)
- DMA interface
  - One transmit DMA channel
  - One receive DMA channel
- Clock interface
  - APB clock for registers, DMA, interrupt functions, and for shift clock generation in master mode
  - Shift clock input for slave mode
- Interrupt interface (one interrupt signal)
- One asynchronous reset input
- Freeze/suspend interface
- DFT signals

HARDWARE CONFIGURATION OPTIONS

OPTION	RANGE	DEFAULT
Local clock gating for low-power operation	On or Off	Off
Clock synchronization for FPGA implementation	On or Off	Off

GATE COUNT AND PERFORMANCE

Gate count and maximum frequency depend on synthesis tool and target technology. Example values for a typical 130-nm technology are:

- 1500 (NAND2 equivalent) gates
- 100 MHz (APB clock)

DELIVERABLES

The MICROWIRE/SPI Controller is available in Source and Encrypted products. The Source product is fully configurable and is delivered in plain text Verilog source code. The Encrypted product, which is available in the Core Store, offers limited configurability (default parameter values) and is delivered in encrypted source code. Both products include:

- Synthesizable Verilog source code (encrypted in the Encrypted product)
- Integration testbench and tests
- Documentation
- Automatic configuration through the IPextreme IP distribution and support portal
- Scripts for simulation and synthesis with support for common EDA tools

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IPextreme

IPextreme, Inc.
307 Orchard City Drive
Suite 202
Campbell, CA 95008
800-289-6412 (toll-free)
408-608-0421 (fax)

www.ip-extreme.com

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