Motorola has developed and patented its Multiple Reference Clock Generator (MRCG) IP to meet the needs of SoCs that require real-time generation and control of multiple clocks running at different frequencies. The MRCG offers several advantages over traditional clock generation technologies such as phase locked loop (PLL) and direct digital synthesis (DDS). Deployed and proven in Motorola products, the MRCG is now available to SoC developers through IPextreme.

HOW IT WORKS

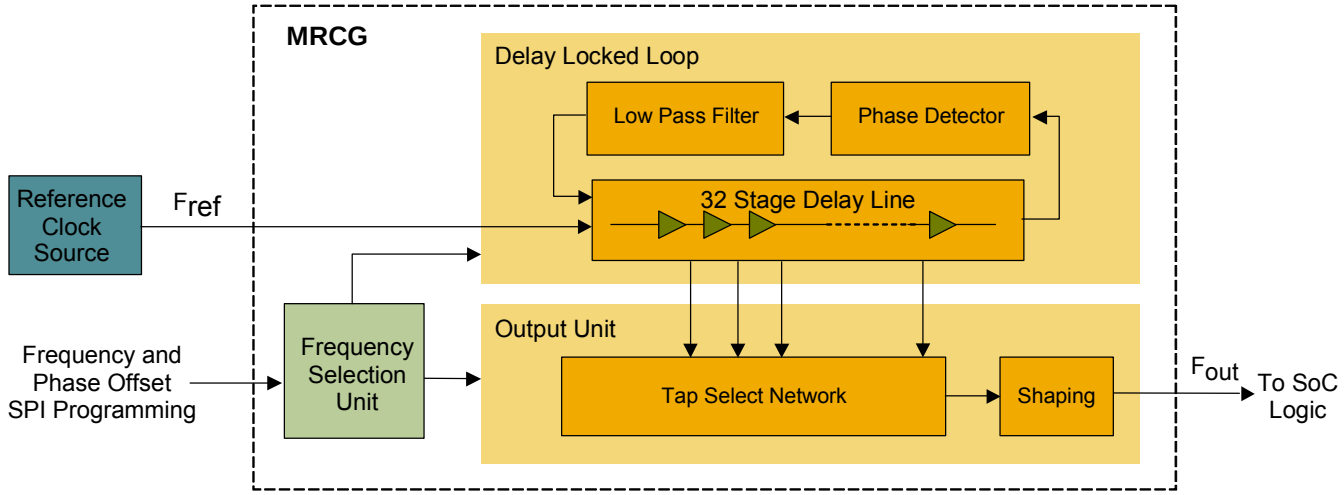
The MRCG uses digital and mixed-signal technology, portable to any semiconductor process, to create multiple clock signals from a single reference clock source. Each generated output clock is a synthesized two-state digital output signal with a transition time determined by a digital-to-phase converter. Each digital-to-phase converter consists of a Tap Select Network, which selects the appropriate phase at the appropriate time from a common Delay Locked Loop (DLL).

The Frequency Selection Unit provides programmable control of output frequency and phase offset by controlling the Tap Select Network. The mixed-signal Shaping block conditions the output clock signal.

The MRCG is scalable to support multiple output clocks. Each output clock requires one instance of the Frequency Selection Unit and Output Unit.

FEATURES AND BENEFITS

- Generates multiple output clocks, each with a programmable frequency and phase offset, from a single reference clock source
- Wideband operation—2 MHz to 1 GHz in 90-nm technology; higher frequencies are achievable in smaller technologies
- Output clock frequencies and phase offsets are programmable in real time through a serial programming interface (SPI)
- Can disable/enable or reconfigure any output clock in real time
- Deterministic behavior—output clock is stable 7 clock cycles after enabling the clock or re-programming to a new frequency or phase offset
- Area and maximum frequency of the MRCG scale with the target technology



ADVANTAGES OVER PLL

The MRCG overcomes several limitations of PLL-based clock generation.

Wide Array of Available Frequencies

With a traditional PLL, clocks derived from the PLL voltage-controlled oscillator (VCO) source through a digital clock divider must be an integer dividend of the 20% band limited PLL frequency. For example, clocks derived from a 100-MHz PLL must be 50 MHz, 25 MHz, 12.5 MHz, and so on. You need a higher-frequency PLL to get a more granular choice of output frequencies.

With the MRCG, the output frequency can be any relation to the source clock frequency (integer or non-integer ratio).

Easy Migration Path to Faster Technologies

With a PLL, if you need additional clock frequencies, you may need to redesign or replace the PLL in your next design. With the MRCG, you can just add instances of the Frequency Selection Unit and Output Unit blocks, with no impact on performance.

And, with the MRCG, you can use the same reference clock and MRCG IP when you migrate your design to a faster technology and just reprogram the MRCG to generate faster clocks for the SoC logic.

Deterministic Clock Stabilization Time

PLLs need time to stabilize upon power-up and the stabilization time may not always be deterministic, which requires some designs to disable their input clocks for the worst-case stabilization time after PLL power-up. With the MRCG, you can individually program the turn-on time of the output clocks and, once the PLL is stable, changes to output clock characteristics—including re-enabling a disabled clock—require exactly seven clock cycles.

Low Jitter

The MRCG contributes marginal jitter due to quantization error; the majority of jitter is determined by the clock signal source. The phase noise of the MRCG clock output signal is aligned to the phase noise of the clock signal source.

Smaller Area, Lower Power

For designs with multiple clocks, using the MRCG results in smaller area and lower power compared to using a separate PLL for each clock.

Even if you generate two or more clocks from a single PLL, the MRCG uses less power and area than a PLL solution to generate the same clocks. The power and area savings increase with the number of clocks generated.

ADVANTAGES OVER DDS

Clock generation through DAC-based DDS technology provides high bandwidth, but consumes more power than PLL-based solutions. In addition, the maximum clock frequency is limited to ½ the reference clock frequency. The MRCG provides high bandwidth, lower power, and a maximum clock frequency equal to the reference clock frequency.

MRCG IMPLEMENTATION

The MRCG is realized through a combination of fully synthesizable digital IP and reusable mixed-signal IP, both of which are available from IPextreme.Adaptation of the IP to your target design and technology is also available as a design service from IPextreme.

A CLOSER LOOK AT THE MRCG

For a closer look at MRCG technology, download the MRCG White Paper from www.ip-extreme.com/whitepapers.

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