National Semiconductor® General Purpose I/O Controller

PRODUCT BROCHURE

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The General Purpose I/O Controller provides sharable connections to chip I/O pads, supporting either 16 or 32 I/O channels. Each channel connects a chip I/O pad to either:

- Data input/output registers within the General Purpose I/O Controller (general-purpose I/O function), or
- One of two selectable peripheral devices (alternate functions A and B)

For example, a single chip-level I/O pin can be shared, under software control, between general-purpose I/O and up to two on-chip peripheral devices such as a USART and/or other component from the National Semiconductor IP Library for AMBA Interconnect.

The General Purpose I/O Controller provides control and data signals to each I/O pad to select data direction (through separate input and output enables), send or receive I/O signal data, and control the I/O pad for weak pull-up, weak pull-down, and high drive.

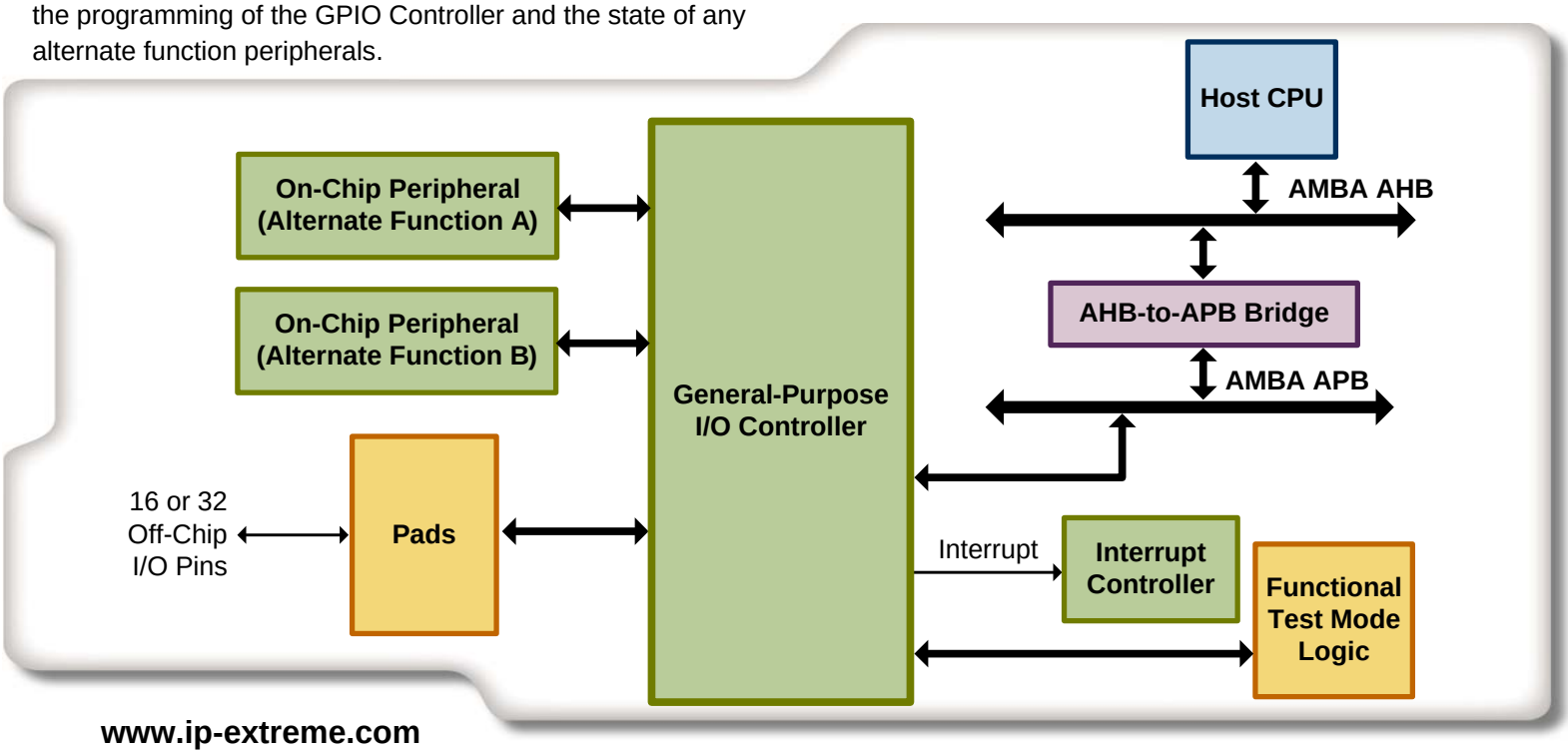
Each input pin can be enabled to provide level-sensitive interrupt capabability, with programmable polarity. The interrupt output signal from the General Purpose I/O Controller is the logic OR of all interrupt-enabled inputs.

A functional test feature enables the I/O pins to be controlled and driven by user-implemented test logic, independent of the programming of the GPIO Controller and the state of any alternate function peripherals.

The host interface of the General Purpose I/O Controller complies with the AMBA 2 APB protocol. Control registers within the General Purpose I/O Controller enable per-channel control of general-purpose I/O or alternate function mode, alternate function source selection (A or B), pull-up/pull-down and high drive signalling, and interrupt functionality. Data in/out registers hold the pin input/output data for general-purpose I/O.

FEATURES

- 16 or 32 I/O channels; each channel corresponds to one off-chip interface pin connected to the General Purpose I/O Controller through an I/O pad
- Programmable pin direction
- Internal weak pull-up, pull-down
- Direct, low-impedance analog input
- Read-back on all registers
- Each pin may be controlled by other modules through its software-selectable alternate function and alternate source
- Selectable high drive current option
- Functional test mode to directly control the pad interface signals from user-implemented test logic



INTERFACES

- AMBA 2 APB host interface
  - 16 or 32-bit read/write data buses (depending on number of I/O channels)
  - 10-bit address bus
- Pads interface to I/O pads
- Peripherals interface to on-chip peripherals for alternate functions
- Functional test mode interface
- Clock interface—APB clock
- Interrupt signal
- One asynchronous reset input
- DFT signals

HARDWARE CONFIGURATION OPTIONS

OPTION	RANGE	DEFAULT
Local clock gating for low-power operation	On or Off	Off
Number of I/O channels	16 or 32	32
Reset values of selected registers	0x0000–0xFFFF (16 I/O channels) or 0x0000_0000–0xFFFF_FFFF (32 I/O channels)	0x0000 (16 I/O channels) or 0x0000_0000 (32 I/O channels)

GATE COUNT AND PERFORMANCE

Gate count and maximum frequency depend on synthesis tool and target technology. Example values for a typical 130-nm technology are:

- 2000 (NAND2 equivalent) gates for 16 I/O channels
- 4000 (NAND2 equivalent) gates for 32 I/O channels
- 100 MHz (APB clock)

DELIVERABLES

The General Purpose I/O Controller is available in Source and Encrypted products. The Source product is fully configurable and is delivered in plain text Verilog source code. The Encrypted product, which is available in the Core Store, offers limited configurability (default parameter values) and is delivered in encrypted source code. Both products include:

- Synthesizable Verilog source code (encrypted in the Encrypted product)
- Integration testbench and tests
- Documentation
- Automatic configuration through the IPextreme IP distribution and support portal
- Scripts for simulation and synthesis with support for common EDA tools

IPextreme

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