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The Smart Card Interface provides a communication interface to a Smart Card, meeting all of the requirements defined in the ISO 7816-3 T=0 protocol and supporting the T=1 protocol through software.

The Smart Card Interface uses a single 16-byte FIFO for both transmit and receive. Data transfer to and from the host system is triggered through programmable FIFO thresholds and can be interrupt-driven or executed through DMA for reduced CPU utilization.

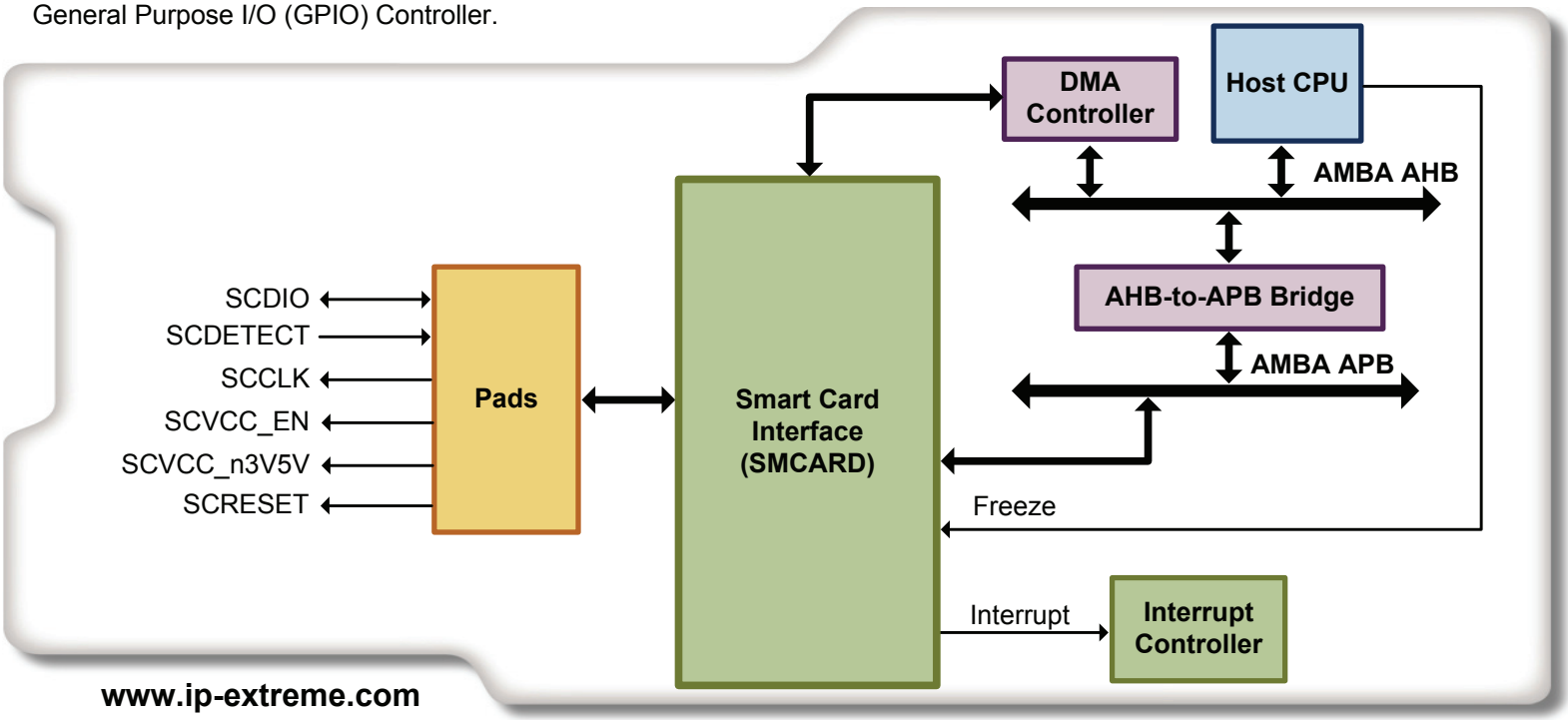
The host interface complies with the AMBA 2 APB protocol. Host-accessible control registers provide CPU control of FIFO threshold levels, Smart Card protocol, clock generation, timeout periods, device activation, and enabling/disabling interrupts and DMA. Status registers provide FIFO, interrupt, and error status. An internal state machine switches the Smart Card Interface between various modes in response to hardware and software events.

The connection to the off-chip Smart Card is through chip I/O pads and includes a bidirectional serial data signal (SCDIO), a card detect input signal (SCDETECT), a Smart Card clock output (SCCLK), output signals for Vcc control (SCVCC_EN and SCVCC_n3V5V), and Smart Card reset output (SCRESET).

To reduce chip-level pin count, the Smart Card Interface signals can be shared with other on-chip functions through a General Purpose I/O (GPIO) Controller.

FEATURES

- Compatible with the ISO 7816-3:1997(E) standard
- Support for asynchronous Smart Cards with asynchronous reset
- Support for asynchronous protocol T=0 in hardware and T=1 in software
- Single 16-byte FIFO used for transmit and receive
- Software-configurable interrupts
- Automatic character repetition for protocol T=0
- Automatic convention detection
- Programmable module clock prescaler
- Programmable card clock and baud rate generator
- Programmable card clock and data line buffer (Sustained Tri-state or Push-Pull)
- Programmable debounce counters for card insertion and removal detection
- Clock STOP HIGH and clock STOP LOW for Smart Card power-down mode
- Automatic execution of activation and (emergency) deactivation sequences
- DMA support for transmit and receive
- Debug support: Freeze/suspend Smart Card Interface



INTERFACES

- AMBA 2 APB host interface
  - 8-bit read/write data buses
  - 10-bit address bus
- Smart Card pins (SCDIO, SCCLK, SCRESET, SCDETECT, SCVCC_EN, SCVCC_n3V5v) through chip I/O pads (optionally through a GPIO Controller)
- DMA interface—one DMA channel shared for transmit and receive
- Clock interface—single APB input clock for registers, DMA, interrupt functions, and SCCLK generation
- Interrupt interface (one interrupt)
- One asynchronous reset input
- Freeze/suspend interface
- DFT signals

HARDWARE CONFIGURATION OPTIONS

OPTION	RANGE	DEFAULT
Local clock gating for low-power operation	On or Off	Off

GATE COUNT AND PERFORMANCE

Gate count and maximum frequency depend on synthesis tool and target technology. Example values for a typical 130-nm technology are:

- 6300 (NAND2 equivalent) gates
- 100 MHz (APB clock)

DELIVERABLES

The Smart Card Interface is available in Source and Encrypted products. The Source product is fully configurable and is delivered in plain text Verilog source code. The Encrypted product, which is available in the Core Store, offers limited configurability (default parameter values) and is delivered in encrypted source code. Both products include:

- Synthesizable Verilog source code (encrypted in the Encrypted product)
- Integration testbench and tests
- Documentation
- Automatic configuration through the IPextreme IP Distribution and Support Portal
- Scripts for simulation and synthesis with support for common EDA tools

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