National Semiconductor
The Sight & Sound of Information

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The Timer and Watchdog from National Semiconductor generates clocks and interrupts that can be used to time periodic functions in a system. It also provides watchdog protection for software execution.

A programmable down-counter provides the timer function. The timer clock source is derived from a slow clock input signal that is processed by a configurable clock prescaler. Upon reaching zero, the timer generates an interrupt and, if programmed to do so, restarts counting from the programmed start value.

The watchdog function generates a watchdog error if the watchdog service occurs too early, too late, or upon a data mismatch. Watchdog error signals can be used to initiate a system recovery; for example, a non-maskable interrupt or system reset.

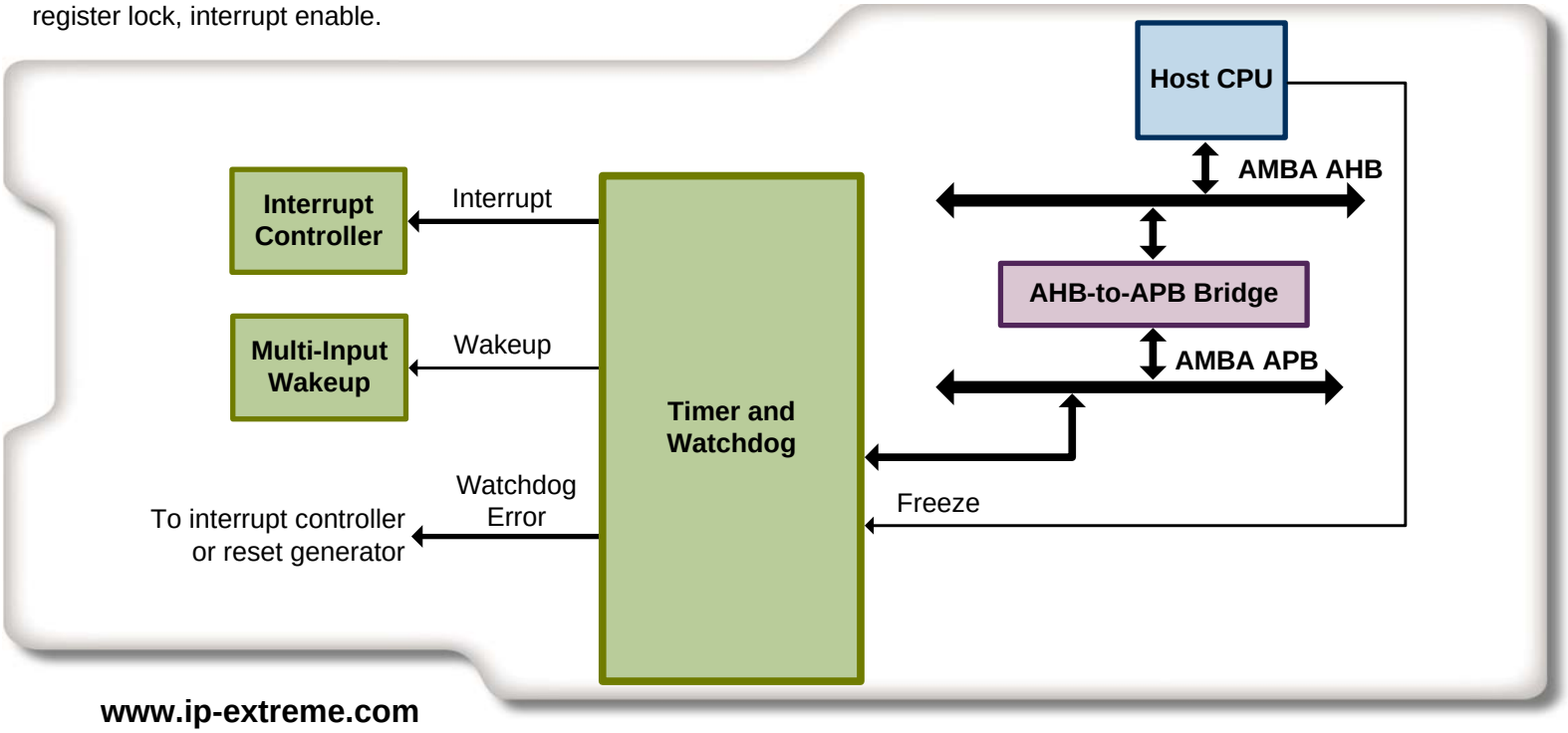
A register lock feature provides protection against erroneous software action. After setting the Timer and Watchdog configuration, software can lock selected registers to prevent write access. Once a section of the Timer and Watchdog is locked, only a system reset can release it.

The host interface of the Timer and Watchdog complies with the AMBA 2 APB protocol. Control registers within the Timer and Watchdog provide CPU control of clock prescaler, timer preset, timer restart, data match value for watchdog service, register lock, interrupt enable.

Status registers indicate terminal count status and, in functional test mode, the current timer and watchdog counter values.

FEATURES

- Slow input clock, typically 32.768 kHz
- 5-bit programmable prescaler counter
- 16-bit programmable periodic interrupt timer
- 8-bit watchdog counter
- Watchdog input clock selector
- Configuration lock option for fully protected watchdog
- Data matching mechanism for watchdog service
- Detection of the following failures:
  - Watchdog service performed too early
  - Watchdog service performed too late
  - Wrong data used in a watchdog service
- Debug support: Freeze or suspend Timer and Watchdog activity



INTERFACES

- AMBA 2 APB host interface
  - 16-bit read/write data buses
  - 10-bit address bus
- Clock interface
  - APB clock for registers and wakeup signal generation
  - Slow clock input for timer
- Interrupt and wakeup signals
- Watchdog error signals to interrupt controller or reset generator
- One asynchronous reset input
- Freeze/suspend interface
- Input signal to indicate functional test mode
- DFT signals

HARDWARE CONFIGURATION OPTIONS

OPTION	RANGE	DEFAULT
Local clock gating for low-power operation	On or Off	Off

GATE COUNT AND PERFORMANCE

Gate count and maximum frequency depend on synthesis tool and target technology. Example values for a typical 130-nm technology are:

- 2000 (NAND2 equivalent) gates
- 100 MHz (APB clock)

DELIVERABLES

The Timer and Watchdog is available in Source and Encrypted products. The Source product is fully configurable and is delivered in plain text Verilog source code. The Encrypted product, which is available in the Core Store, offers limited configurability (default parameter values) and is delivered in encrypted source code. Both products include:

- Synthesizable Verilog source code (encrypted in the Encrypted product)
- Integration testbench and tests
- Documentation
- Automatic configuration through the IPextreme IP distribution and support portal
- Scripts for simulation and synthesis with support for common EDA tools

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