CFV2SPP5208

IPextreme

Freescale™ ColdFire® V2 Core & SPP 5208

PRODUCT BROCHURE

The ColdFire V2 Core & Standard Product Platform 5208 (CFV2SPP5208) combines the ColdFire V2 Core with industry-proven platform peripherals to form a complete low-cost, low-power microcontroller subsystem supported by a vast ecosystem of development tools and runtime software. The CFV2SPP5208 is the same ColdFire V2 processor core and platform/peripheral IP implemented in Freescale's MCF5208 devices. With the CFV2SPP5208, you get:

- A fully synthesizable implementation of the popular ColdFire architecture
- Reliability—from processor and peripheral IP already deployed in millions of embedded systems worldwide
- Rapid time-to-market—in just a few hours you can be developing software on your own FPGA implementation of the CFV2SPP5208

COLDFIRE V2 CORE

The ColdFire V2 Core is a low-power, low-area, 32-bit processor core with single-cycle-access local SRAM and a direct-mapped cache that can be configured as instruction cache, data cache, or split instruction/data cache. The ColdFire V2 Core delivers over 250 DMIPS of performance at 240 MHz and includes an enhanced MAC unit for DSP-like functions and faster execution of multiply instructions.

Like all ColdFire architecture processors, the ColdFire V2 Core features a variable-length instruction set for maximum code density, industry-standard AMBA 2 AHB system bus interface for rapid system integration, and a wide selection of development tools, operating systems, drivers, and libraries from both commercial and open source providers.

STANDARD PERIPHERALS AND INTERCONNECT

The CFV2SPP5208 includes the ColdFire V2 Core, plus the fully-integrated peripherals shown in Figure 1, providing commonly needed functions such as Ethernet, interrupt control, DMA, timers, and various serial interfaces. An AMBA 2 AHB Crossbar Switch provides the system interconnect, supporting simultaneous transfers between multiple AHB masters and slaves, including externally-connected AHB masters and slaves.

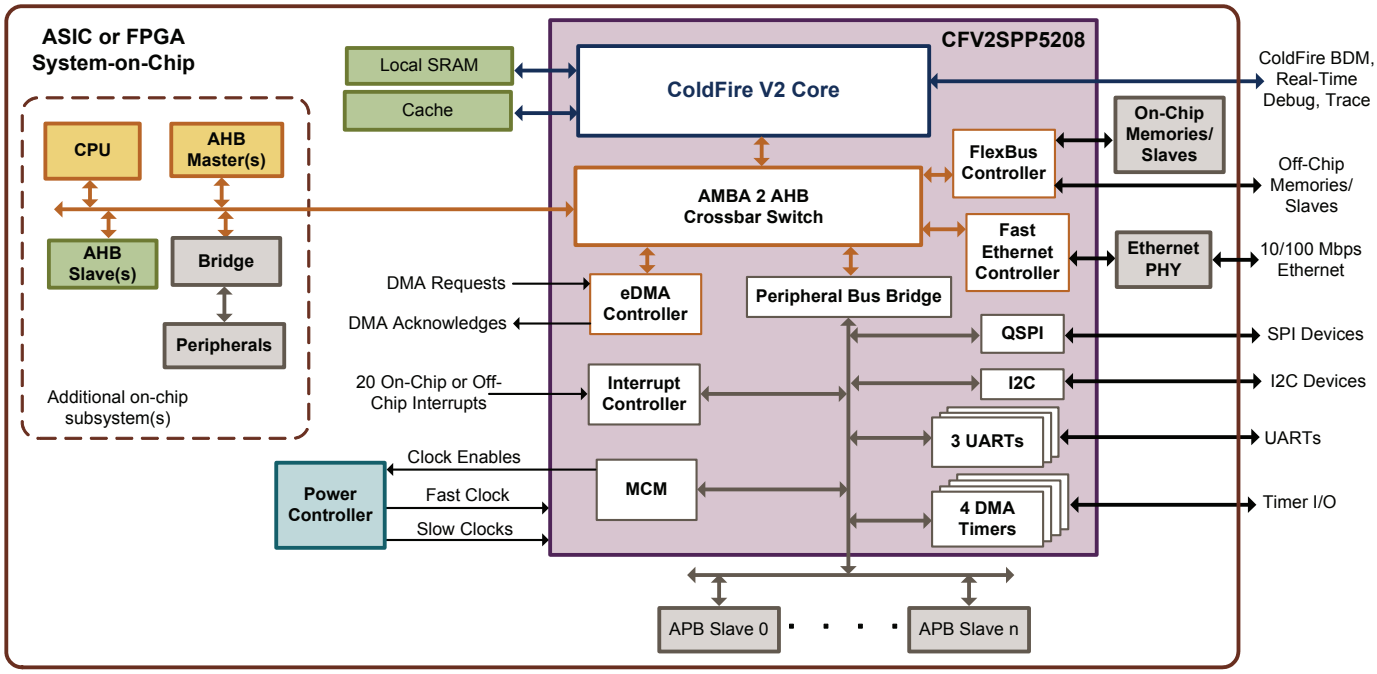
Variations of the CFV2SPP5208 with different combinations of on-board peripherals are also available. For example, you can add more peripherals, such as another Fast Ethernet Controller, or omit peripherals that you don't need to reduce system gate count.

PERIPHERALS FEATURES

On-board peripherals and their features include:

- FlexBus Controller
  - Connects up to 6 on-chip or off-chip memories/devices
  - Independently programmable transfer characteristics for each device (wait states, address setup/hold)
- Enhanced DMA (eDMA) Controller
  - 16 independently programmable DMA channels
  - Programmable channel arbitration modes
  - Support for channel linking and scatter/gather operation
- Fast Ethernet Controller
  - 10/100 Mbps Ethernet support
  - Half and full-duplex modes
  - Media Independent Interface (MII) or 7-wire interface to Ethernet PHY

Figure 1: Example SoC Using CFV2SPP5208



- Interrupt Controller
  - 64 programmable interrupt sources, 20 of which are available for external interrupts
  - Unique vector for each interrupt source
  - Support for low-power mode wake-up
- Queued SPI (QSPI) module
  - Programmable queue for up to 16 SPI transfers
  - Four chip-select lines for up to 16 devices
  - Programmable baud rate, before-and-after transfer delays, clock phase and polarity
- I2C interface module
  - Support for the original Philips I2C bus protocol
  - Support for baud rates up to 3.4 Mbps
- 3 UARTS
  - Programmable clock source, data formats, and modes (normal/loopback)
  - Error detection
  - Four maskable interrupt conditions
- 4 DMA Timer modules
  - Programmable clock source
  - Programmable prescaler
  - Programmable interrupt or DMA request upon timer event
- Miscellaneous Control Module (MCM)
  - Software watchdog timer
  - Reset status, low-power mode control, and core fault status registers

POWER SAVING FEATURES

The CFV2SPP5208 features software-controlled shutdown of selected clocks to support a variety of chip-level low-power modes:

- Independent shutdown of selected peripheral clocks
- Shutdown of the ColdFire V2 Core CPU clock in response to a ColdFire STOP instruction

DEBUG SUPPORT

The CFV2SPP5208 supports ColdFire Debug Architecture Revision B+, including:

- Background Debug Mode (BDM)
- Real-Time Trace (RTT)
- Real-Time Debug (RTD)

DEVELOPMENT SUPPORT

The ColdFire architecture is supported by a vast assortment of development systems/tools and run-time software including libraries, stacks, drivers, and operating systems from providers such as Freescale, Green Hills Software, Wind River Systems, CodeSourcery, and many more. For example, the Sourcery G++ tool suite from www.codesourcery.com supports ColdFire V2 targets and can be used to develop new code or to retarget ColdFire V1 programs to ColdFire V2 devices. A free version of the GNU compiler supporting ColdFire V2 targets is also available from www.gnu.org.

Freescale offers development boards, software, and CodeWarrior Development Tools (including a free version supporting the ColdFire V2 architecture). In addition, there are several operating systems supporting the ColdFire V2 architecture, including uClinux and several RTOS's, such as the MQX RTOS from Embedded Access, Inc.

GATE COUNT/MAXIMUM FREQUENCY

The CFV2SPP5208 gate count depends on synthesis tool and target technology. Approximate gate count for a typical 90-nm technology is 157K gates. The maximum CPU frequency for the same target technology is approximately 200 MHz. In 65-nm technology, the maximum frequency is 240 MHz.

The CFV2SPP5208 achieves over 85 MHz in most FPGA devices and uses approximately 24,000 LUTs in an Altera Stratix III device. For a Stratix III EP3SL200F1152C2, that is only 15% utilization.

DELIVERABLES

- Verilog source code
- Integration testbench and tests
- Documentation
- Scripts for simulation and synthesis with commonly-used EDA tools

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