### FRCC2100

## **IPextreme**

### Freescale FlexRay Communications Controller Core

#### ⇒ PRODUCT BROCHURE





#### **PRODUCT DESCRIPTION**

To deliver the safety, comfort, and entertainment features consumers are demanding, modern vehicles have become rolling data centers.

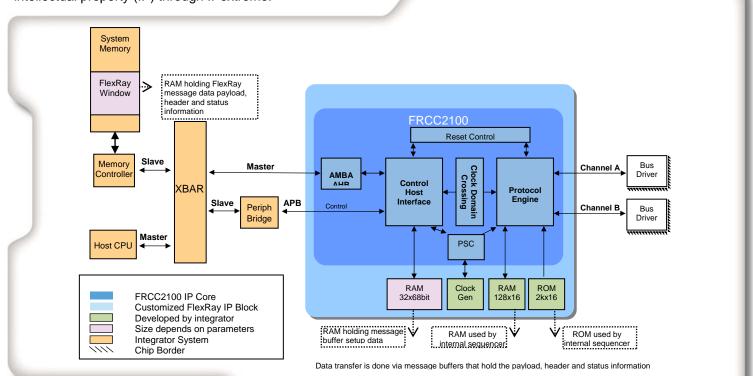
With backing the leading car manufacturers and their electronics suppliers, FlexRay is becoming the next widely implemented vehicle network standard. FlexRay delivers previously exclusive functionality, being fast and flexible without giving up the reliability or deterministic behavior required by safety critical applications such as brake-by-wire or future steer-bywire.

Freescale Semiconductor is a founding and core member of the FlexRay Consortium and the world's largest supplier of automotive chips. Freescale was the first company to produce a FlexRay silicon sample. Freescale's FlexRay standard parts are used today within the first volume manufactured vehicle employing FlexRay technology in an automotive application.

Now the same FlexRay Communications Controller design proven in those chips is available as licensable intellectual property (IP) through IPextreme.

#### **KEY FEATURES**

- Low power consumption through extensive clock gating
- Developed by Freescale alongside the FlexRay Specification development with the FlexRay Consortium
- Modular design allows tailoring to SOC designer's end product
- Proven in Freescale standard devices (MFR42xx,43xx, MPC55xx), first car with FlexRay
- 100% synthesizable Verilog code, Protocol Engine intensively tested by major IDMs
- TÜV conformance tested IP (Specification V2.1A)
- Low power, small area
- Supported by Flexray software tool providers for application software, operating system, FlexRay stack, and driver software
- Integration support from IPextreme
- Training facilitated by Freescale and 3rd parties



#### **FRCC2100 DESIGN FEATURES**

- Modular design
  - PE cleanly separated from CHI
  - Memories external to core
- Data transfer is done through message buffers that hold the payload, header, and status information
- Single 10-Mbit/s channel for affordability, dual independent channels for 20-Mbit/s, or redundant 10-Mbit/s channels for reliability
- Support for lower data rates (2.5, 5 and 8 Mbit/s)
- Maskable interrupt signals
- Reports on clock synchronization
- AMBA interface to host CPU and system memory
- Low power consumption through extensive clock gating (optional, may be implemented external to the IP block)
- CHI clock independent of PE clock through Clock Domain Crossing
- Configurable:
  - Maximum number of message buffers hardware configuration option (4-252)
  - Message buffer setup programmable at runtime
  - Two independent receive FIFOs, each with up to 255 entries and flexible filtering
  - Four configurable slot error counters

#### THE FRCC2100 ECOSYSTEM

Application core	Software component	Software component	Software component	Software component	Software component
AUTOSAR Runtime Environment (RTE)					
AUTOSAR OS	Development Error Tracer	Generic Network Management	AUTOSAR COM	Diagnostic Communication Manager	XCP Protocol Layer
	Communication Manager		PDU Router		1/2D 7 .
	ECU State Manager	FlexRay Network Management		FlexRay Transport Protocol	XCP Transport Layer on FlexRay
	Diagnostic Event Manager	FlexRay Interface			
		FlexRay Driver			Transceiver Driver

FRCC2100 is supported by most FlexRay software providers for application, operating system, FlexRay stack, and driver software. The FRCC2100 can be connected to FlexRay-compliant physical bus drivers.

#### FRCC2100 PROTOTYPING/EVALUATION

MFR4310 FlexRay Starter Kit



- 2 x FlexRay nodes based on MFR4310 IP and two HCS12X development boards
- CodeWarrior Development Tool CD containing demo application, FlexRay monitoring software and low level drivers (unified driver, written in C) as well as one application example

#### **FRCC2100 IP DELIVERABLES**

- Verilog RTL code of FlexRay module
- Self-checking integration testbench
- Packaged with IPextreme XPack
- Web based self-checking configuration Xpack Web to specify options and timing
- Automatically generation of synthesis scripts and constraints
- Supports all major EDA flows
  - Support for Incisive and VCS-MX simulation flows
  - Support for Design Compiler and RTL Compiler
- FRCC2100 User Guide
- Integration Guide
- XPack Guide
- IP integration and product support

# **IPextreme**

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