Compact JTAG

IPextreme

IEEE 1149.7 Compact JTAG Interface

PRODUCT BROCHURE

The Compact JTAG IP from IPextreme provides an IEEE 1149.7-compliant Test Access Port (TAP), enabling you to take advantage of IEEE 1149.7 features such as:

- 2-pin access to your on-chip IEEE 1149.1 test infrastructure
- Reduced scan times through shorter scan paths
- Efficient use of the 2-pin interface for both test and debug

The Compact JTAG IP supports all mandatory and optional features of IEEE Std. 1149.7-2009 and is the cornerstone of the emerging Compact JTAG ecosystem—implemented in chips from Texas Instruments and other major semiconductor manufacturers and the reference design used by leading development system providers.

IEEE STD 1149.7-2009

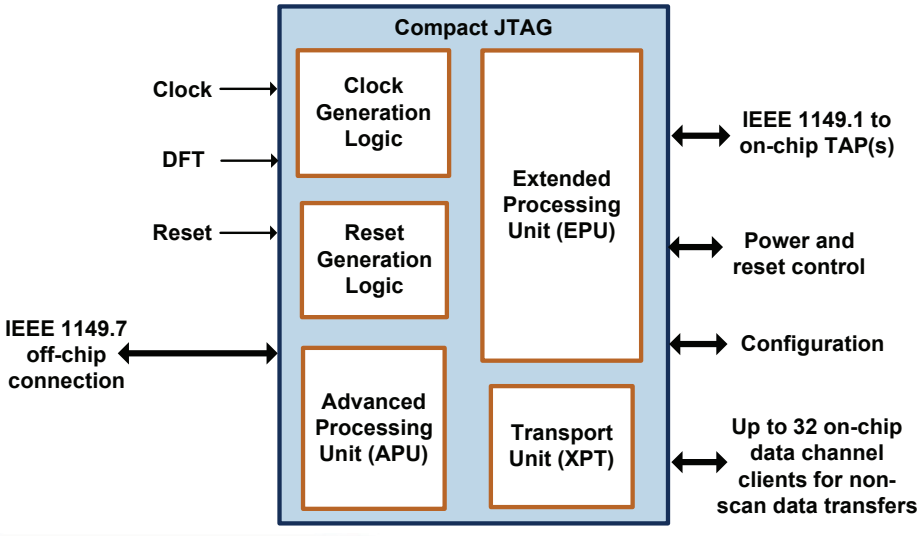
IEEE Std. 1149.7-2009 defines a next-generation Test Access Port (TAP), known as TAP.7, which extends IEEE 1149.1 TAP (TAP.1) functionality in several ways. Whereas IEEE 1149.1 was original developed as a solution for testing board-level interconnect, IEEE 1149.7 offers additional features to support increased chip integration, power management, application debug, and device programming. IEEE 1149.7 features are grouped into six classes, each of which is a superset of all the lower classes:

- Class T0 maintains strict compliance to IEEE 1149.1 while also providing support for multiple IEEE 1149.1 TAPs on a single chip
- Class T1 adds support for the IEEE 1149.7 command protocol, generation of functional and test resets, and power control
- Class T2 adds the capability to bypass a chip's system test logic, resulting in a 1-bit path for Instruction Register (IR) and Data Register (DR) scans
- Class T3 adds support for connecting TAP.7 controllers in a 4-wire star topology (TAP.7 controllers connected in parallel)
- Class T4 adds support for 2-pin operation (all signalling done using only TMS(C) and TCK(C)), which means that TDO and TDI can be removed or used for other functions
- Class T5 adds support for up to two data channels for non-scan data transfers, with each data channel supporting up to sixteen on-chip data transfer clients

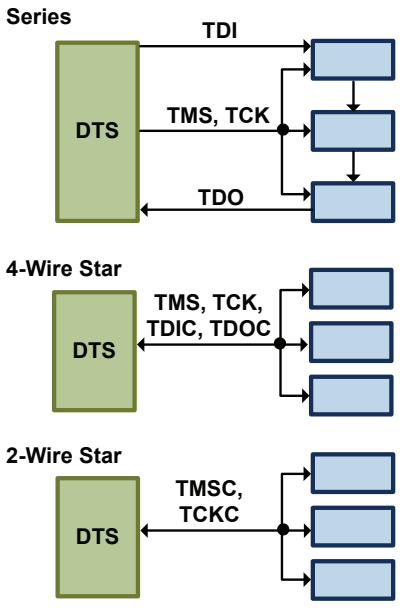
COMPACT JTAG IP FEATURES

- Supports IEEE 1149.7 classes T0–T5
- Supports all mandatory and optional scan formats: JScan0–3, MScan, OScan0–7, and SScan0–3
- Supports all IEEE 1149.7 mandatory and optional features, commands, and registers
- Firewall provides robust hot-connect protection by disabling TCK to on-chip test logic until the Debug Test System (DTS) deactivates hot-connect protection

Compact JTAG On-Chip Interconnect



IEEE 1149.7 Scan Topologies



- Partitioned along IEEE 1149.7-specified functional boundaries:
  - Reset and Selection Unit (RSU) for class T0 optional features (contained within the APU)
  - Extended Processing Unit (EPU) for extended (class T1–T3) operation
  - Advanced Processing Unit (APU) for advanced (class T4 and T5) operation
  - Separate blocks for clock and reset signal conditioning
  - Data channel (class T5) logic is optional and is, therefore, isolated into a separate top-level module

CONFIGURATION OPTIONS

Through hardware parameters, you can select the following optional features of the Compact JTAG IP:

- Power-down support. If you choose to include power-down support, the Compact JTAG IP supports all IEEE 1149.7 power-down modes and the power-down mode restore feature. Power-down support requires a 32-kHz clock for the power-down timer.
- Data channel (class T5) support:
  - Transport function with 1 or 2 physical data channels (PDCs), each supporting up to 16 data channel clients
  - Transport function with 0 PDCs (no data channel support; however, the Compact JTAG IP remains online if the DTS initiates the transport protocol to a different target sharing the same DTS connection)
  - No transport function or data channel support (Compact JTAG IP functions a class T4 TAP)

INTERFACES

- Compact JTAG (IEEE 1149.7) interface to off-chip DTS
- JTAG (IEEE 1149.1) interface to on-chip test logic
- Power control/status interface to on-chip logic
- Functional/test reset interface to on-chip logic
- Configuration interface for node ID, JTAG device ID, decouple-at-startup, Controller ID, and TDI/TDO pin functions
- Data channel interface for optional data channels
- 32-kHz clock (optional, used for power-down mode support)
- Power-on reset
- DFT signals to control clock and reset for scan testing of the Compact JTAG logic

INTEGRATING THE COMPACT JTAG IP

The off-chip interface of the Compact JTAG IP includes all required and optional IEEE 1149.7 interface signals, plus the associated enable and pullup control signals for the chip-level I/O pads. You can choose to connect TCK(C), TMS(C), TDI(C), and TDO(C) to support both IEEE 1149.1 and IEEE 1149.7 debug/test environments or connect only TCKC and TMSC to support only IEEE 1149.7 two-pin operation. For further flexibility, you can connect TDI(C) and TDO(C) and, at run-time, select either their respective IEEE 1149.7 functions or user-defined functions.

The Compact JTAG IP also supports nTRST and return TCK (RTCK), each of which is optional and uses an additional chip-level I/O pin. RTCK is not a standard IEEE 1149.7 signal, but is provided to support non-standard implementations where TCK is adapted to an on-chip functional clock.

The interface to on-chip test logic is an IEEE 1149.1-compliant TAP interface for connection to a chip-level TAP controller and, optionally, multiple embedded TAP controllers. The 4-bit TAP state of the Compact JTAG IP is available for the on-chip test logic to use instead of implementing an additional JTAG state machine. The on-chip data channel client interface functions as defined in IEEE Std. 1149.7-2009.

The size of the Compact JTAG IP class T4 configuration is approximately 2500 gates in a typical 90-nm process. Class T5 with full data channel support adds approximately 1300 gates.

COMPACT JTAG IP DELIVERABLES

- Synthesizable Verilog source code
- Integration testbench and tests
- Documentation
- Scripts for simulation and synthesis with support for common EDA tools

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