



The RAM Controller (RAMC) provides connectivity between an AMBA 2 AHB and a synchronous RAM (SRAM). It features single-cycle, pipelined access to 32-bit SRAM and supports 8, 16, and 32-bit data accesses. It is the same RAM Controller IP proven in high-volume devices from National Semiconductor.

The host interface of the RAMC complies with the AMBA 2 AHB protocol. The AHB data bus width is 32 bits, while the AHB address bus width is configurable (3–32 bits). The RAMC does not generate wait states on the AHB; each data phase is one clock cycle.

The RAMC connects to a synchronous RAM through a generic RAM interface. The RAM must support byte-write operation and can be implemented either as a single 32-bit RAM or as four 8-bit RAMs.

The RAMC does not pass the 2 least significant bits of the AHB address (HADDR[1:0]) to the RAM address output. Therefore, byte-addresses on the AHB address bus become 32-bit word addresses at the RAM interface. For write accesses, the RAMC automatically generates the correct RAM byte write enables according to the values of AHB signals HADDR[1:0] and HSIZE[2:0].

For read accesses, the RAMC always reads a 32-bit word and returns the full 32 bits on HRDATA[31:0].

If a read access occurs while a write access to the same address is pending, the RAMC returns the internally registered write data for the byte(s) that have not yet been written to the RAM.

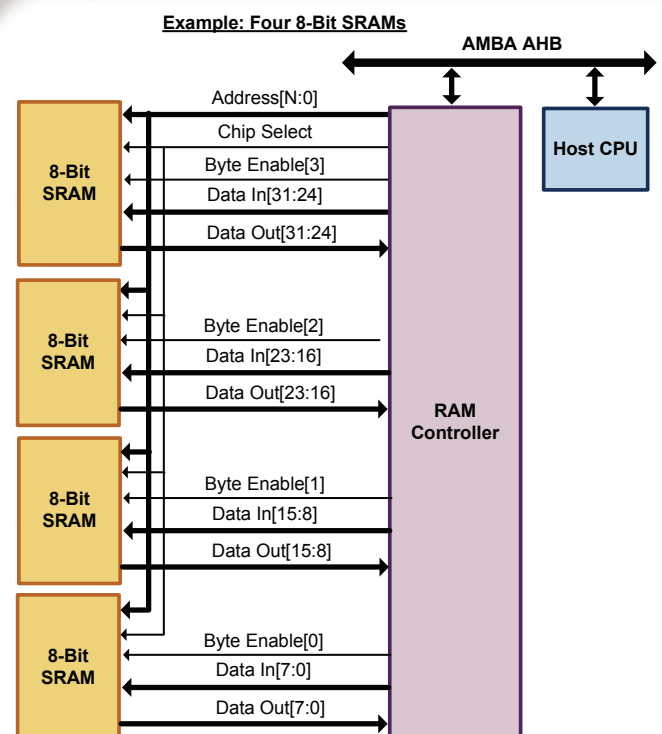
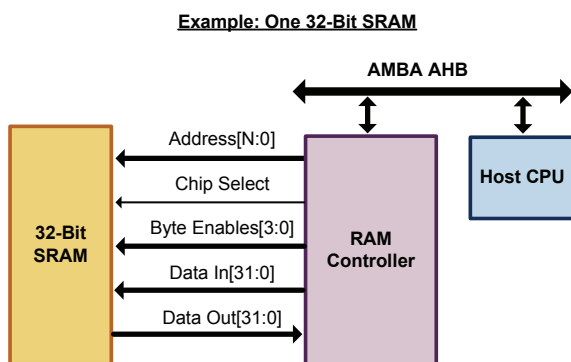
### FEATURES

- ▶ AMBA 2 AHB compliant host interface
- ▶ Single-cycle pipelined read/write accesses to 32-bit SRAM
- ▶ 8, 16, or 32-bit accesses
- ▶ Configurable address width
- ▶ SRAM can be implemented as single 32-bit RAM or four 8-bit RAMs
- ▶ Little endian data interface
- ▶ Local clock gating for minimal power consumption

### DELIVERABLES

The deliverables for the RAM Controller include:

- Synthesizable Verilog source code
- Documentation
- Scripts to synthesize the RAM Controller with common EDA tools





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