Sn/Pb SMT Application Notes

General

Soldering temperature profiles used must provide adequate temperature rise time and cool-down time to prevent damage due to thermal shock. These guidelines are emphasized because cracking or other damage caused by handling or thermal shock is not necessarily apparent under ordinary visual inspection techniques. The damage can be very small (micro-cracks) and can occur under the terminations where even high magnification cannot detect them. The problem is further complicated by the fact that these micro-cracks may not be initially detectable by standard electrical testing. Once initiated, the cracks can grow with time and cause latent failures. Attention to these details will aid in the successful use of the inherently reliable multilayer ceramic capacitor.

Ceramic capacitors larger then EIA size 1812 are known to be very susceptible to thermal shock damage due to their large ceramic mass. These large parts require more care during installation than smaller surface mount devices.

Solder Pre-Heat Cycle

Proper preheating is essential to prevent thermal shock cracking of the capacitor. The circuit assembly should be preheated as shown in the recommended profiles at a rate of 1.0 to 2.0°C per second to within approximately 100°C of the maximum soldering temperature. Temperature change should be distributed as evenly as possible throughout large capacitor bodies as applying heat or cold to a localized spot on the device may result in thermal gradients great enough to cause cracking.

SMT Soldering Temperatures

Solders typically utilized in SMT have melting points between 179°C and 188°C. Activation of rosin fluxes occurs at about 200°C. Based on these parameters, typical maximum reflow temperatures run between 210 to 230°C. Use of thermal profiling is advised for accurate characterization of circuit heat absorption and maximum component temperature conditions that occur during the soldering process.

Solder Reflow

Recommended temperature profiles for reflow soldering are shown in Figures 1 & 2. A maximum heating rate of 3°C/sec. (4°C/sec. for vapor phase) should not be exceeded between the pre-heat cycle and maximum soldering temperature.

Solder Wave

Wave soldering can be utilized, but the preheat requirements generally make this process very difficult to accomplish. Recommended temperature profile for wave soldering is shown in Figure 3. **Wave soldering is not recommended for ceramic MLCCs larger then 1210 size due to the incompatibility of the chip's mass with the steep temperature gradient typically present in this process.**

Figure 1: Solder Reflow Profile for MLCCs

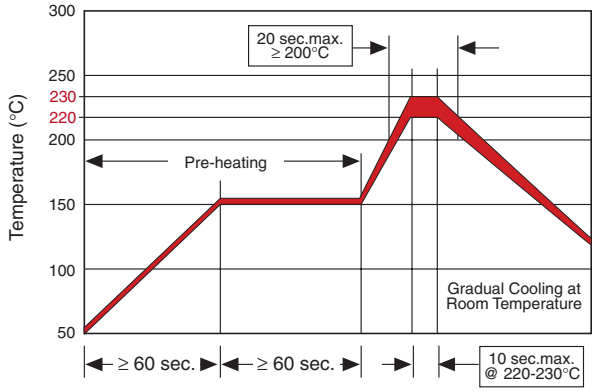


Figure 2: Vapor Phase Profile for MLCCs

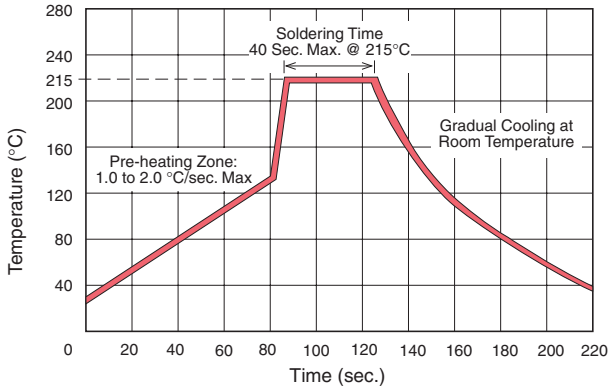
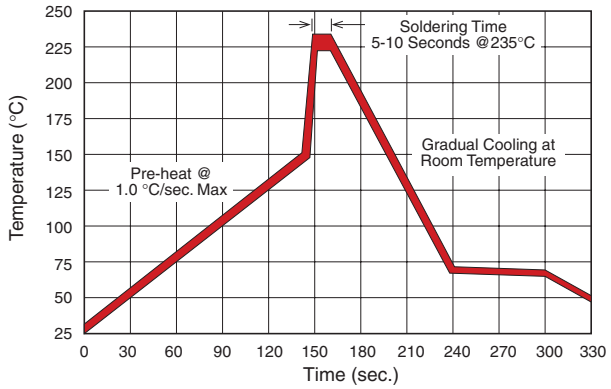


Figure 3: Wave Solder Profile for MLCCs



Soldering Iron

Ceramic capacitor attachment with a soldering iron is discouraged due to the inherent process control limitations. In the event that a soldering iron must be employed the following precautions are recommended.

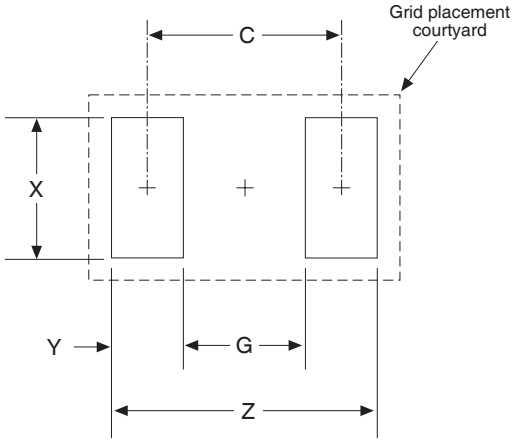
- Preheat circuit and capacitors to 150°C
- Never contact the capacitor with the iron tip
- 30 watt iron output (max)
- 280°C tip temperature (max)
- 3.0 mm tip diameter (max)
- Limit soldering time to 5 sec.

Cool Down Cycle

After the solder reflows properly the assembly should be allowed to cool gradually, again maintaining the thermal gradient of 2°C/sec. maximum at room ambient conditions. Attempts to speed this cooling process or immediate exposure of the circuit to cold cleaning solutions increase the possibility of thermal shock cracking of the ceramic capacitor.

IPC 7351 Land Pattern Guidelines

Appropriate pad design, solder application, and component orientation are all ingredients of a quality, defect-free soldering process. The Institute for Interconnecting and Packaging Electronic Circuits (IPC) has developed and published IPC 7351 "Surface Mount Design and Land Pattern Standard". This standard presents industry consensus on optimum dimensions based on empirical knowledge of fabricated land patterns. The standard also contains an excellent analysis of solder joints and their relation to component, PCB, and placement tolerances. A summary of the IPC land pattern design recommendations for solder reflow and solder wave processes are listed in table below. It is highly recommended that the PCB designer/SMT process engineer obtain the complete IPC 7351 standard (http://www.ipc.org)



Chip EIA	Size (mm)	Reflow Solder Z	G	X	Y(ref)	C(ref)	Solder Wave Z	G	X	Y(ref)	C(ref)
0402	1005	2.4	0.4	1.3	1.0	1.4					
0603	1608	2.8	0.6	1.0	1.1	1.7	3.18	0.68	0.80	1.25	1.93
0805	2012	3.2	0.6	1.5	1.3	1.9	3.70	0.70	1.10	1.50	2.20
1206	3216	4.4	1.2	1.8	1.6	2.8	4.90	1.50	1.40	1.70	3.20
1210	3225	4.4	1.2	2.7	1.6	2.8	4.90	1.50	2.00	1.70	3.20
1808	4520	5.8	2.5	2.7	1.7	4.2	Not Recommended				
1812	4532	5.8	2.0	3.4	1.9	3.9					
1825	4564	5.8	2.0	6.8	1.9	3.9					

Tomb Stoning / Chip Movement

Tomb-stoning or draw bridging is illustrated in figure 1. Tomb-stoning or other undesirable chip movements may result if unequal surface tension forces exist as the molten solder wets the MLCC terminations and mounting pads. This tendency can be minimized by insuring that all factors at both solder joints are equal, namely; pad size, solder mass, termination size, component position and heating. Tomb-stoning is easily avoided through proper design, material selection and proofing of the process.

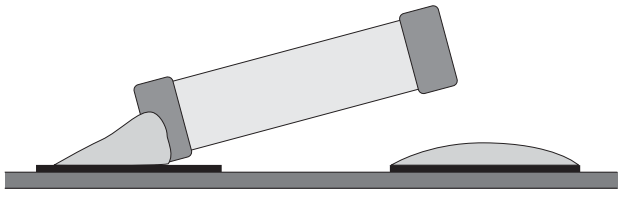


Figure 1