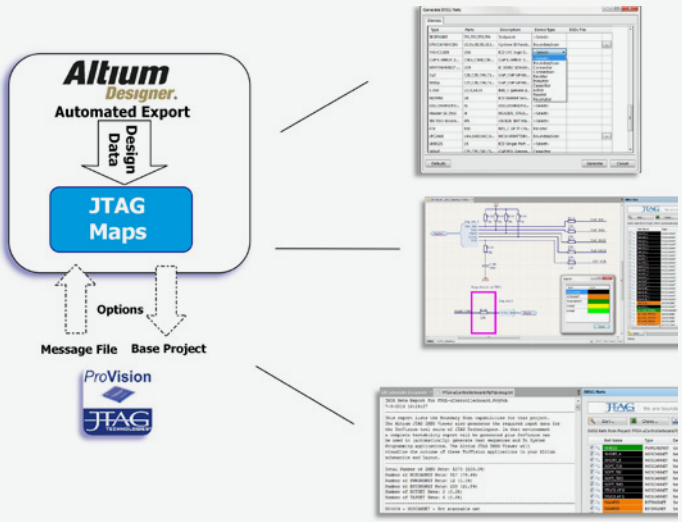
Factsheet

JTAG MAPS™ - AN EXTENSION TO ALTIUM

Analysis and display of boundary-scan coverage for Altium Designer



- Rapid view of JTAG nets mapped on your schematic
- Assists with the DfT process
- Shows base-level boundary-scan access
- Visualize both TAP nets and 'testable' nets
- Exports project data to JTAG Technologies tools
- Creates net access statistics table.

Introduction

A large number of today's designs feature JTAG/boundary-scan components that can provide valuable test resources during hardware debug, manufacturing test and even depot repair. JTAG Maps™ is a simple extension to Altium designer that allows the design engineer to very quickly assess the capabilities of the JTAG resources on a design - before committing to layout.

Highlighting the schematics

In the past, engineers often spent a great deal of time highlighting the boundary-scan nets of a design manually to assess the fault coverage from boundary-scan for their design. Today the free JTAG Maps for Altium application does this automatically, freeing up valuable time, allowing a more thorough DfT and speeding-up time to market.

With or without boundary-scan models

Boundary-scan device models (BSDLs) are the mainstay of any JTAG/boundary-scan process as they indicate precisely which pins can be controlled or observed by JTAG/boundary-scan. However, BSDL models are not always available in a timely manner. To overcome this potential problem JTAG Maps for Altium can be used without BSDL files also, so that you can still quickly get an overview of the potential boundary-scan coverage. Note that if available, a BSDL model will provide all bscan details of a device and hence the most accurate picture.

Order information
JTAG Maps for Altium - download from Altium extensions web portal
http://www.altium.com/products/extensions

Automatic chain detection

JTAG Maps for Altium will automatically detect the scan chain path (or paths) with no limits to the number of paths (also known as TAPs) in the design. The nets associated with the TAPs will be highlighted separately from the 'testable' nets using different colors.

While most users will want to simply use the quick coverage report that JTAG Maps for Altium can provide, it is also possible to import a more accurate picture. After creating a JTAG ProVision archive from your Altium project, data can be analysed further within JTAG ProVision. A simple txt-based message file containing full fault-coverage information can then be read back into JTAG Maps for display/highlighting.

Optional Developer Tools

Factsheet

JTAG MAPS™ - AN EXTENSION TO ALTIUM

Analysis and display of boundary-scan coverage for Altium Designer

For engineers wishing to apply JTAG/Boundary-scan tests directly onto their design JTAG Technologies offers two further options, JTAGLive and JTAG ProVision.

JTAGLive is a perfect getting started tool and offers a basic pin to pin testing feature (free Buzz) and the advanced Python-based scripting system (Script) for more involved sequential testing using loops branches and defined variables made up from pin groups.

JTAG ProVision meanwhile offers a fully automated ATPG system for pin to pin interconnects, memory clusters. logic blocks and more. ProVision also includes capabilities to perform in-system programming across a wide range of CPLDs, SPROM, Flash Devices and µProcessors with embedded memory.

JTAG Maps users looking for a demonstration or evaluation of these systems should contact their local sales office or email info@jtag.com

Figure 2

JTAG Maps set-up screens

Region or Country	Telephone	E-mail
• Europe or Rest of World	+31 (0)40 295 0870	info@jtag.nl
• United Kingdom & Ireland	+44 (0)1234 831212	sales@jtag.co.uk
• North America	Toll free - 877 FOR JTAG Western US - 949 454 9040	info@jtag.com
• China, Malaysia, Singapore, Thailand, Taiwan	+86 (021) 5831 1577	info@jtag.com.cn
• Germany	+49 (0)971 6991064	germany@jtag.com
• Finland	+358 (0)9 4730 2670	finland@jtag.com
• Sweden	+46 (0)8 754 6200	sweden@jtag.com

1800-Q4_2016_1003