

Optimising LED manufacturing

LED manufacturers seek new methods to reduce manufacturing costs and improve productivity in an increasingly demanding market. **Tom Pierson, Ranju Arya, Columbine Robinson of KLA-Tencor Corporation** discuss how epitaxy process control can result in improved MOCVD uptime and overall yield. Challenges that can be assisted with inline inspection techniques.

To meet the requirements of demanding new market applications such as LCD backlighting and general lighting, light emitting diode (LED) manufacturers must slash costs and boost fab productivity. Inline inspection will be critical in that effort, speeding the fab ramp process and increasing production yields. In the front end wafer semiconductor process, epitaxial layer defects in particular can account for as much as 50% of the total wafer level yield budget. The KLA-Tencor's Candela surface inspection system is designed for the inspection needs of the LED industry and can capture a wide variety of mission-critical substrate and epitaxial defects. Full implementation of inline inspection and statistical process control (SPC) could cut yield loss from epi defects in half while significantly increasing the metal-organic chemical vapour deposition (MOCVD) reactor uptime.

Inline inspection for LED process

LED performance is defined by optical characteristics such as efficiency, brightness, and colour quality, which depend on the composition and structure of the device layer. The industry currently uses photoluminescence, reflectance measurements, x-ray diffraction, and similar analytical techniques to monitor wavelength, film thickness uniformity, material composition, and other metrics tied to optical performance and parametric yield. In addition, the industry is seeing increasing adoption of automated inspection tools for monitoring and control of epitaxial defects. Epi defects are known to impact the electrical and optical properties of LED devices as well as limiting reliability and lifetime. Functional yields can vary from batch to batch – typical yields at full wafer test (FWT) can range from 60% to above 90% depending on chip design, material defects, and fabrication process

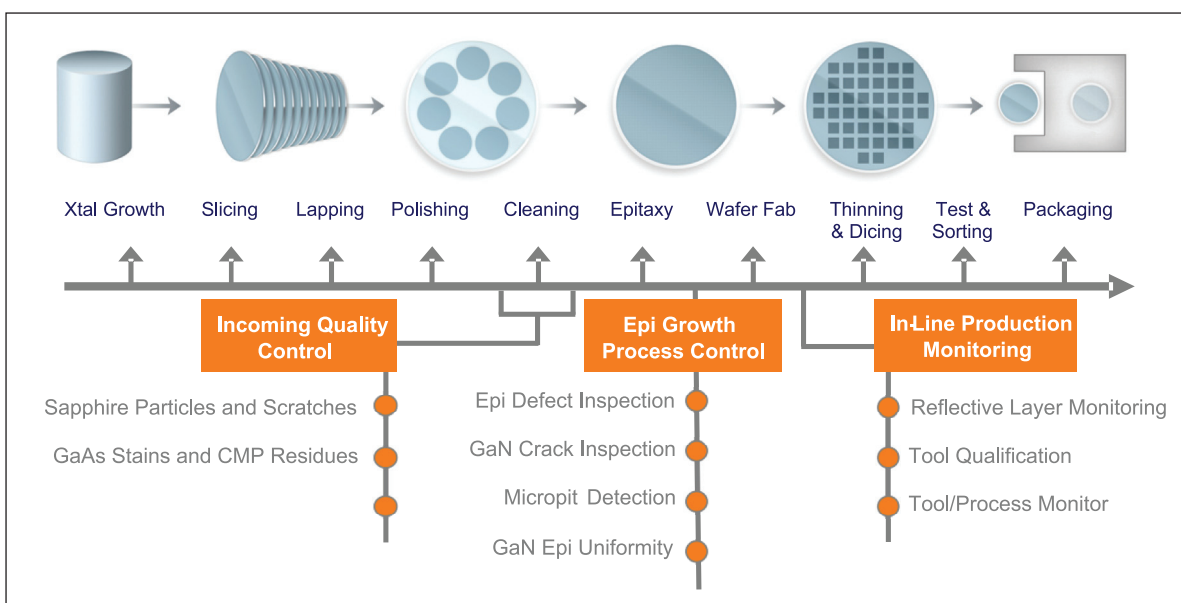


Figure 1: Key inspection points in the LED manufacturing process

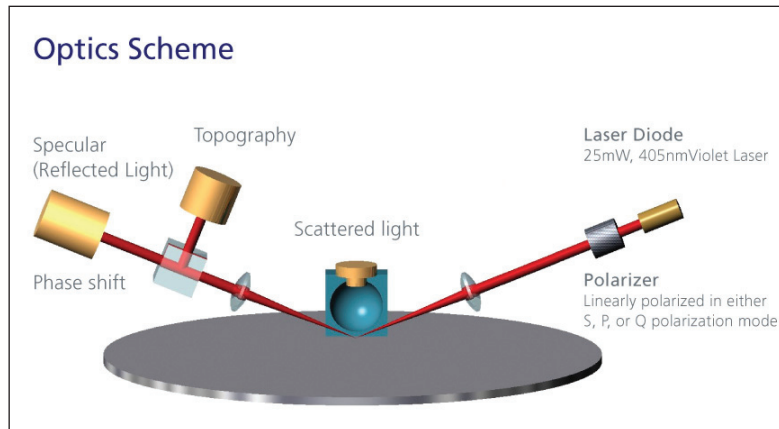


Figure 2: Candela design with multi-channel analysis to detect and classify a wide range of mission-critical defects

variations. Epitaxial layer defects in particular can account for as much as 50% of the total wafer level yield budget. Industry leaders who use automated inspection to monitor defect densities within wafer, wafer-to-wafer, and batch-to-batch estimate that optimal inspection practices can reduce the yield impact of material defects and offer significantly higher yields.

Key inspection points across the front-end process include before and after cleaning and final preparation of substrates, and after deposition of the epitaxial layer (Figure 1). If a yield crash occurs, having data from multiple inspection points greatly simplifies the root cause analysis and helps prevent misguided process adjustments. There is no need to alter MOCVD process parameters when the underlying problem can be traced to incoming substrate quality.

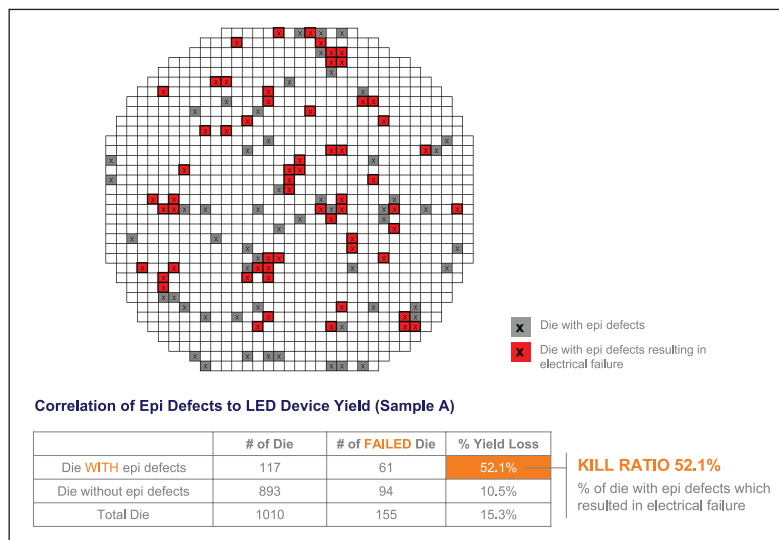


Figure 3: Correlation of epi defects to LED device yield

Epi defect correlation

KLA-Tencor's inline inspection system is designed specifically for the defect inspection requirements of the LED industry. The optical design uses multi-channel detection technology to measure the scatter, reflectivity, phase shift, and topographic variations across the transparent substrate surface (Figure 2). Multiple measurements are made enabling production grade throughput and 100% surface coverage.

After scanning, the analysis software extracts defects from the background signal, classifies them by defect type, and reports defect parameters and locations. For example, during inspection of polished sapphire substrates, the inspection recipe may include particles, scratches, pits, slurry residues and stains. Typical GaN-epitaxial layer defects include particles, scratches, micropits, microcracks, crescents, circles, hexagon bumps, and other topographic defects.

An analysis grid can be set to match the die dimensions, allowing correlations between individual defects and final wafer test results. For example, Figure 3 shows the influence of epi defects on device performance. In this study, the device die grid was overlaid on the Candela defect map and pass/fail criteria was set based on known killer defects (i.e. epi pits, crescents, hexagon bumps, and topography clusters). It is important to note that surface particles were omitted from the pass/fail criteria as surface particles are added and removed many times throughout processing.

After device fabrication, FWT electrical probe data was collected. Failed die were defined as those with a reverse leakage current greater than 1mA indicating a short of the device p-n junction. The corresponding yield map was overlaid with the Candela defect map to demonstrate the correlation between epi defects and LED device yield. Dies with known killer epi defects had a 52.1% failure rate (or kill ratio) at electrical testing, while dies without epi defects had only a 10.5% failure rate. Thus, dies with killer epi defects had a 5X greater probability of failure than those without defects.

Figure 4 shows the bar graph of the yield loss for the samples in this study. From the correlation investigation, total yield loss can be partitioned into "epi defect induced yield loss" and "other sources of yield loss." Other sources of yield loss include fabrication induced defects, particle and handling contamination, etc. The total yield loss after FWT for the three LED wafers analyzed was 15.3%, 17.5%, and 14.3% of which 6.0%, 7.2%, and 5.5%, respectively, could be attributed to epi defects. In this example, the epi defect induced yield loss represents roughly 40% of the total yield loss budget.

Best Known Methods (BKMs)

Manual inspection techniques are inadequate for full wafer coverage and do not provide detection and classification results in a quantitative and repeatable manner. At best, manual inspection techniques might detect a rise in defectivity due to a major process excursion, but they will miss a transient increase in the severity of specific killer defects such as pits or hexagon bumps. Such minor excursions, subtle increases in killer defect densities, are virtually undetectable through manual inspection techniques, but can account for a substantial fraction of total yield loss.

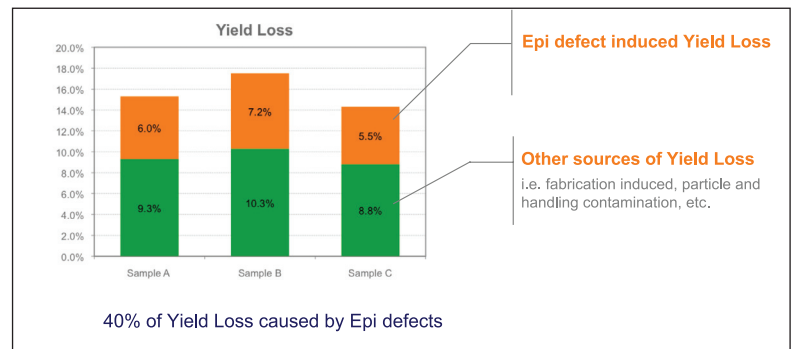
Figure 5 shows the value of automated inspection for early detection of an epi reactor excursion of epi pits known to short the device p-n junction. The upper portion of the figure illustrates a minor excursion which goes undetected by manual inspection. A typical fab cycle through FWT is two to three weeks. Thus, for a manufacturer running at 20,000 wafer starts per month (WSPM) the feedback loop does not occur until the wafers reach electrical FWT. In the case of a two-week fab cycle, a minor excursion would expose 10,000 wafers to increased defect densities and increased yield loss. The lower portion of Figure 5 illustrates how automated inspection isolates the defect excursion.

Corrective actions quickly reduce defectivity levels to within process control limits. Fewer wafers are exposed to killer defects, reducing incremental yield loss. Early detection of excursions through automated inspection translates to millions of dollars in savings each year for LED chip makers. The cost of the MOCVD epitaxial layer is also an important contributor to overall device cost. MOCVD equipment accounts for about 65% of the capital cost of an LED fab (source: Bank of America Merrill Lynch Global Research, 2009). Maximizing the uptime and productivity of these systems is critical. Leading LED manufacturers use Candela defect data to implement SPC monitoring on each MOCVD reactor, thereby providing a rapid control loop should the defect density of a given reactor exceed process control limits.

Substrate and epi-layer defects

Common defects on sapphire substrates include particles, pits, scratches and CMP process stains. Substrate pits are known to cause GaN epi defects. Sapphire substrate stains are a root cause of localized areas of GaN epi roughness, where underlying high densities of atomic crystal dislocations can short device p-n junctions. Figure 6 illustrates the cause-and-effect of substrate stains on subsequent GaN-epi growth.

Automated inspection of incoming substrates verifies substrate quality. With clear pass/fail criteria,



manufacturers can more readily set and enforce material quality specifications, raising both yield and overall device performance.

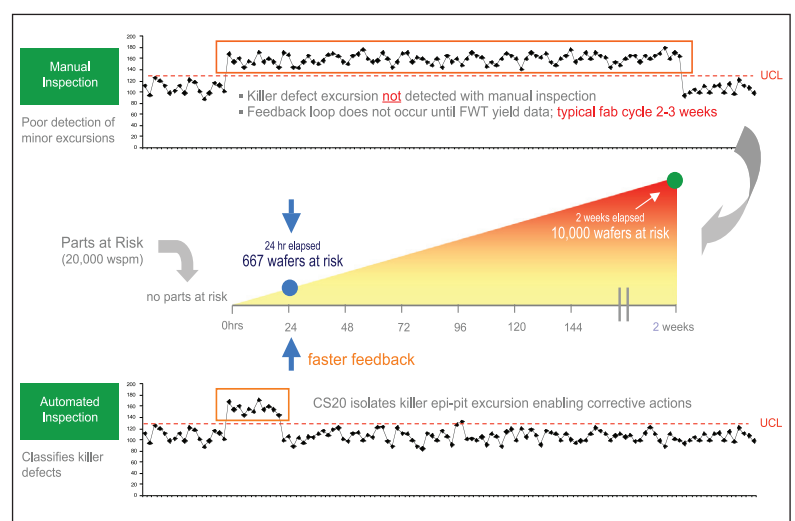
Figure 4:
Sample yield
Loss

MOCVD processes produce a variety of GaN epi defects; common yield-impacting defects include hexagonal pits and bumps, crescents, circles, and other topographic defects. In addition to such device killers, GaN epi cracks are also known to be a significant reliability killer. As LEDs make their way into higher-end applications such as LCD backlighting, automotive, and general lighting, field reliability and LED performance longevity are of critical importance.

GaN epi cracks can be extremely problematic to LED makers as these defects cannot be screened at FWT or final probe test and only later result in field failures and expensive recalls.

Figures 7.a and 7.b illustrate Candela inspection images for GaN epi morphology and epi crack defects. These defects can be readily detected and classified in the output defect map.

Figure 5:
The value of
automated
inspection for
early detection
of an epi
reactor
excursion of
epi pits



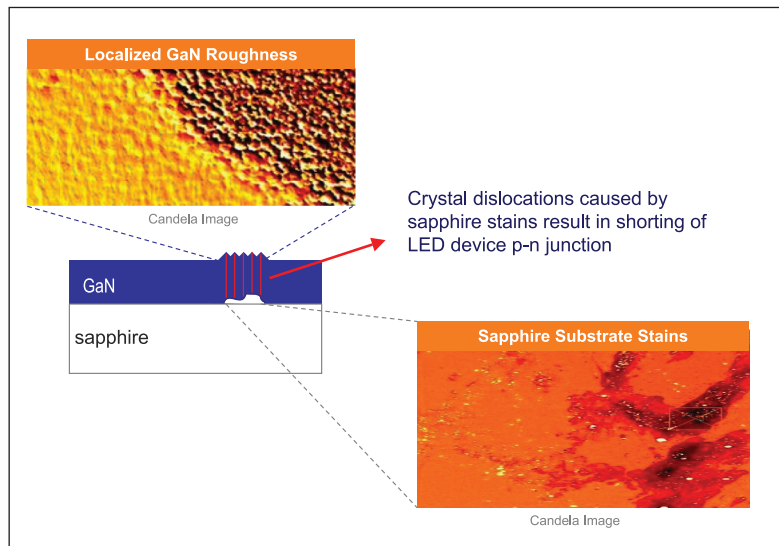


Figure 6:
Impact of
substrate stains
on GaN-epi

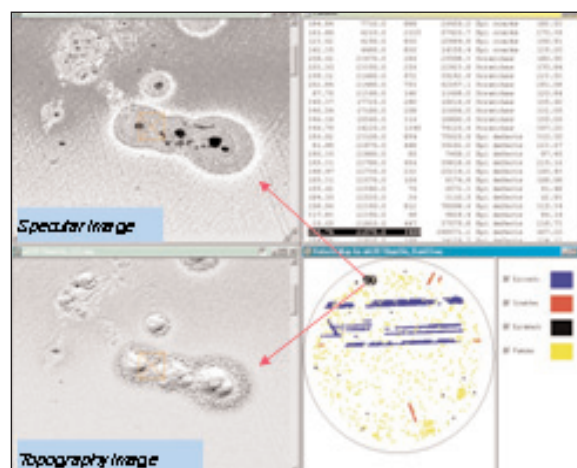
Improving yield

Inline inspection delivers ROI by helping to improve yield, minimize process excursions, and increase MOCVD uptime. Inline defect inspection, combined with SPC monitoring, provides a rapid feedback loop for tuning reactor growth parameters and correcting process problems. If these interventions keep epi defectivity within control limits there is less need for preventive maintenance procedures and their associated downtime.

Figure 8 illustrates a timeline representative of the evolution of process control improvements and benefits derived from automated inline inspection. The x-axis begins at time = 0, i.e. the point in time when an LED fab implements automated inspection with production SPC monitoring. Figure 8 summarizes the three key economic benefits derived from automated inspection with SPC:

1. Killer defect reduction from process improvement.

When production-grade automated inspection is first



Above left: Figure 7.a: Candela specular and topography images of typical epi topography defects

Above right: Figure 7.b: Candela specular and topography images of typical epi crack defects

implemented, defect levels are high with wide run-to-run tolerances. Quantitative and methodical inspection results provide engineers with the necessary data to design experiments aimed to reduce epi defectivity and improve production yields. On average, LED makers will achieve a 2-3% improvement in FWT yield within the first 6 months of ownership.

2. Fewer production lots exposed to yield loss from minor excursions.

Once baseline defect levels are established, control limits are put in place to monitor each MOCVD reactor. Defect inspection provides a feedback loop for corrective actions on MOCVD process parameters. Inspection sampling rates are typically 100% in order to address within-wafer, wafer-to-wafer, and run-to-run trends. Reduced exposure to minor excursions – which may last for weeks, or even months – is the most common economic gain realized by LED device manufacturers.

3. Prevention of minor excursions from becoming major excursions.

Defect inspection not only provides a feedback loop to minimize the impact of minor excursions, but also helps to prevent minor excursions from becoming major excursions thereby improving MOCVD uptime and overall productivity.

These three components of value are the key drivers for implementation of automated inline inspection. Reducing killer defect densities results in yield improvement while defect density SPC results in less exposure to minor excursions and increased MOCVD uptime. Leading LED manufacturers worldwide have demonstrated that the value derived from automated inspection translates to millions of dollars in savings each year.

Conclusions

Epi defects in the bottleneck MOCVD process are frequent yield killers and account for roughly half of the

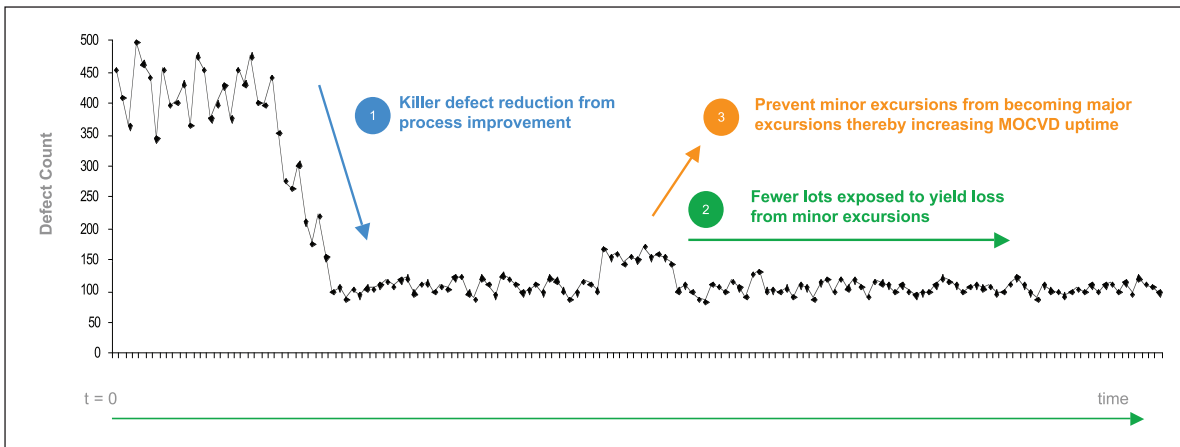


Figure 8: Key value drivers of automated inline inspection

total wafer level yield budget. Implementation of inline inspection and SPC monitoring of the MOCVD process could cut the yield loss from epi defects in half.

These yield and productivity (MOCVD uptime) enhancements are achieved through killer defect

reduction, early detection and prevention of minor and major excursion trends. KLA-Tencor's Candela surface inspection system allows comprehensive inspection and control of epi process and helps LED manufacturers realize this multi-million dollar yield opportunity.

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