



# Automated defect-data analysis allows comprehensive yield management in LED manufacturing

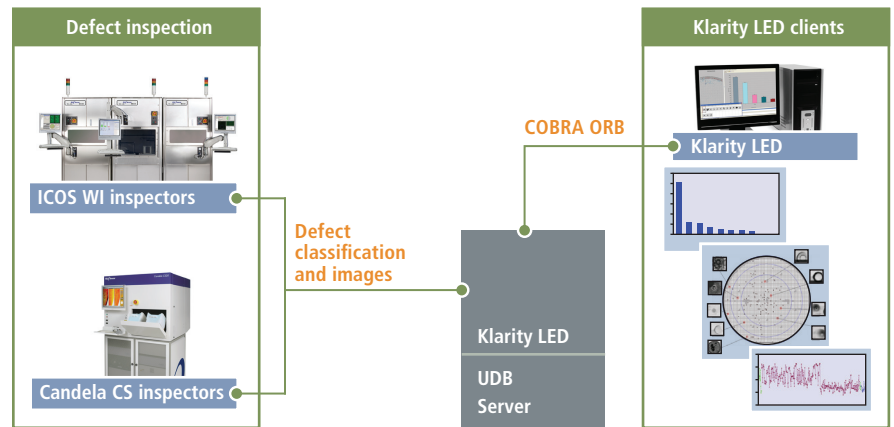
Automated, systematic analysis of defects during LED wafer manufacturing should reduce the time needed to identify and resolve the underlying problems, according to authors from **PHILIPS LUMILEDS** and **KLA-TENCOR**.

The LED manufacturing industry is facing a number of production challenges, driven by the evolution of higher-power and higher-performance LED devices along with the emergence of new high-end, high-volume applications such as solid-state lighting. At the same time, the parameters for acceptable devices are becoming more stringent, and the market is imposing higher production-volume requirements and price constraints.

Taken together, these driving forces are raising the bar significantly with regard to yield management in LED manufacturing. The current approach taken by LED manufacturers relies heavily on manual gathering, review and analysis of defect/yield data. As LED manufacturers see increased demand for their products and more competition in the market, the need for an automated, systematic defect-analysis methodology has become more apparent.

To address these escalating requirements, leading LED manufacturers such as Philips Lumileds Lighting are pioneering new automated-inspection methods based on technologies such as those from KLA-Tencor that have already proven successful through multi-generation deployments in the semiconductor industry.

This article examines an automated software solution for inline analysis of KLA-Tencor's ICOS WI-Series defect-inspection data using the same company's Klarity LED yield-



**FIG. 1.** Typical data flow for Klarity LED.

analysis solution. The objective is to use the graphical charting and quantitative analysis capabilities of Klarity LED to reveal a clearer understanding of defect trends, improve the analysis capabilities, and reduce the time needed to identify and resolve defect issues.

Automated analysis features within Klarity LED include the following: excursion monitoring and automated report generation; spatial signature analysis (SSA); and defect source analysis (DSA).

## Motivation

Defect reduction has always been an on-going effort at Lumileds. The defect group has been successful in driving defect-reduction programs to meet the target yield, but the methods currently employed require a substantial

effort from each member of the team.

The current method of defect analysis at Lumileds relies heavily on manually sorting and reviewing defect data from the inspection tools. In the event of an excursion, it usually takes from several hours to a day to review the defect data of the affected lots or wafers.

The data review is performed in the cleanroom via a tool-specific offline image-review station. This can be a tedious and time-consuming task. And once the "problem wafer" is identified, the engineer has to identify which layer caused the problem and which module/process is responsible. Thus, it may require days of analysis and process optimization before the issue can be resolved.

The engineer will typically spend about 2-3 days per week analyzing the defect-inspection data, identifying excursions and generating the weekly yield report. This report is then presented and discussed during the weekly yield meeting. Thus, the

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majority of the engineer’s work week can easily be consumed just to generate this weekly yield report.

**Data flow**

The data-flow concept for using Klarity LED software within a more comprehensive defect-analysis scenario is depicted in Fig. 1.

Wafer-inspection tools, namely ICOS WI for patterned LED wafers and Candela CS for un-patterned wafers, send defect data in the form of KLARF files to a centralized Klarity Unified Database (UDB). Each KLARF contains defect information, such as defect ID, defect location and defect size. Defect patch images from the inspection tools can be linked to individual defects via embedded pointers and uploaded to the UDB.

Klarity LED clients are installed on PCs (either in the office or clean-room), and are linked to the UDB via the existing network. Clients can perform queries to generate wafer-maps, control charts, defect Pareto charts and defect image galleries, etc.

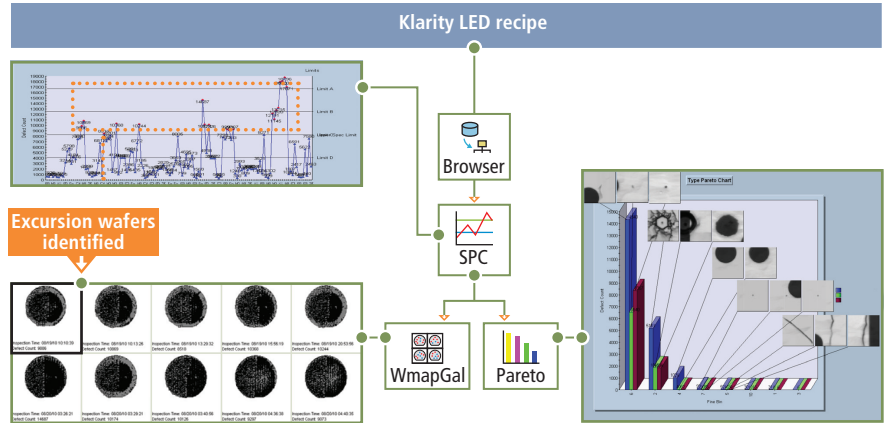
The desired outcome of this effort at Lumileds was to enable defect-control engineers to use Klarity LED features that would allow them to make more-informed factory-floor decisions. Some of the use cases and test strategies developed during the implementation phase are documented in the following sections.

**Use-case 1: Excursion detection using SPC charting**

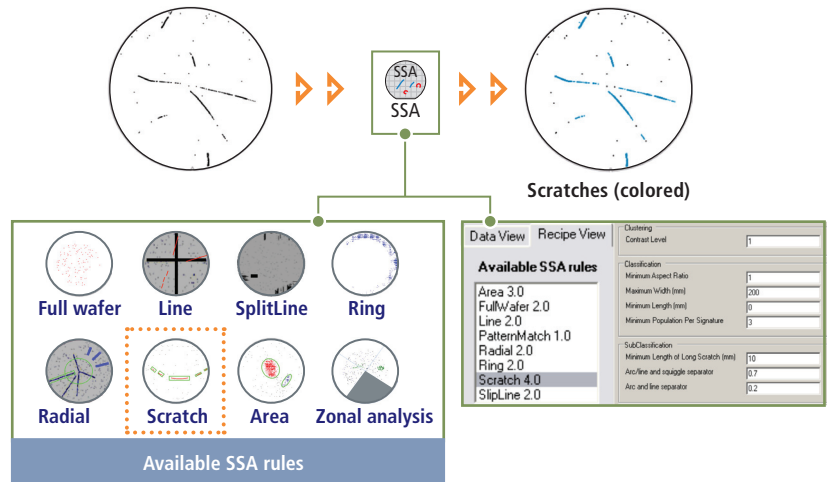
Lumileds monitors and detects line excursions through defect trend charting. Before the introduction of Klarity LED, operators on the production floor would manually input the inspection data and the defect engineers compiled this data on a weekly basis. Manual input of data is both time-consuming and highly prone to human error.

In the event of an excursion, the defect engineer often investigated the issue by going into the clean-room to review the wafer maps one by one on the inspection tool. The engineer often had to spend hours in the clean-room to review the data wafer by wafer or lot by lot, depending on the extent of the issue.

With the introduction of Klarity LED, defect-analysis recipes can be created to automatically generate statistical process control



**FIG. 2.** Excursion detection use case: Klarity LED recipe setup and resulting SPC charts, wafer-map gallery and defect type Pareto.



**FIG. 3.** Spatial signature analysis (SSA) flow.

(SPC) charts. These charts can then be used for defect trending and excursion detection. Trend charts can be generated for daily, weekly or monthly tracking of defect levels. The defect engineer can also set SPC limits and have Klarity LED automatically notify them should an excursion occur. These functions can all be done using simple and intuitive graphical recipes as shown in Fig. 2.

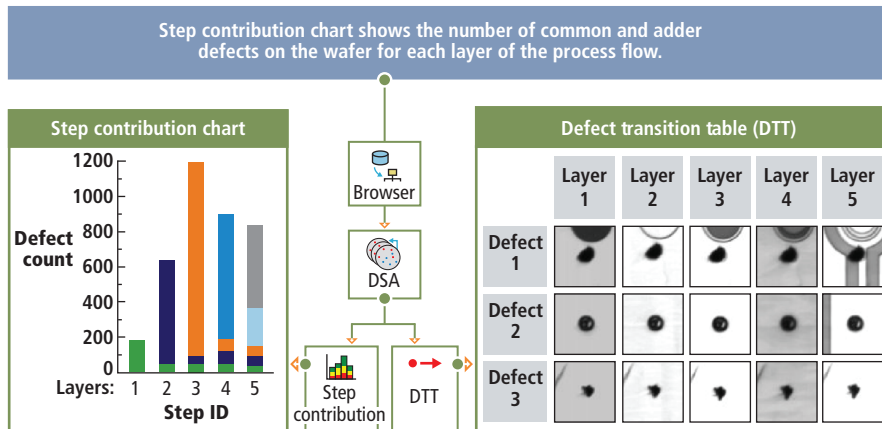
**Use-case 2: Using SSA to identify signatures on wafers**

Along with the ability to perform defect trending and monitoring, the ability to flag and identify wafers that exhibit certain pre-determined spatial signatures can be a powerful tool. The defect engineer can use this capability to monitor known, intermittent process issues or to help in identifying the

root cause of certain defect excursions.

Klarity LED incorporates spatial signature analysis (SSA) to quickly identify wafers with specific defect signatures. The user “trains” the SSA node by customizing rules via an SSA recipe editor and using sample wafer data having the signature of interest. Once done, the user will save the rule settings as an SSA recipe and incorporate this SSA recipe into the Klarity LED recipe for analysis as shown in Fig. 3.

In one case study, SSA was employed to quickly identify the source layer for a specific nuisance defect (non-yield-limiting defect). This nuisance defect is often referred to as a “fish-scale” defect. Fish-scale defects, if they occur in a massive amount, form either a “donut” or “ring” signature on the wafer, which is very unique. The lot-to-lot variation



**FIG. 4.** Example of a typical recipe with defect source analysis (DSA) and defect transition table (DTT) nodes.

for this defect type is quite high, leading to false excursion events. After implementation, the true yield-limiting lot-to-lot variation could be identified.

In another case study, it was observed that on some wafers there was high defectivity due to defect clusters at the edge of the wafer. Using the zonal-analysis feature of Klarity LED, Lumileds was able to quickly quantify the location of these specific clusters. Trend charts were set up to monitor occurrence of the edge signatures. Wafers with signatures were singled out using SSA and SPC to determine the locations with a high concentration of edge clusters. With this information the defect engineer could perform additional

analysis to further narrow-in on the root cause of the excursion using the DSA capability discussed in the next section.

### Use-case 3: Using DSA to determine root cause

One of the key elements of defect reduction is to determine which layer/process step is producing the defects. Knowing this, the engineer can then go on to determine the root cause of the problem and make the right decision to rectify the problem.

Defect source analysis (DSA) is a powerful tool to help the defect engineer narrow the search for the source of problem. It enables the engineer to trace the transition of defects

on a wafer as the wafer moves from one layer to the next layer in the process flow, clearly identifying which defects are common to multiple inspections and which are newly added (so-called adders).

The DSA function is further enhanced via a defect transition table (DTT) feature. The DTT allows the user to track how a defect's morphology changes from layer to layer along the process flow, as seen in Fig. 4.

### Conclusions and results

Klarity LED has demonstrated the ability to significantly improve the efficiency of systematic defect-analysis capabilities to support a high-volume LED production environment. Incorporating various options to sort, filter, display and analyze defect-inspection data produced many meaningful interpretations for the user.

The bottom line is a significant improvement in both the timeliness of data and the accuracy of analysis to support improved yields at increasingly-higher production volumes.

Based on the results of the above-described use cases, it is anticipated that further deployments and extensions to KLA-Tencor's Klarity LED will play a key role as Philips Lumileds Lighting continues to enhance its LED production capabilities and to introduce new leading-edge LED devices.