# Accelerate Yield: Design Based Inspection

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KLA-Tencor
Accelerating Yield

The maximum sensitivity of advanced patterned wafer inspectors can produce sizable inspection results, with $10^5$ to $10^6$ defects detected per wafer during the process development stage. Because engineers base yield decisions on these defect results, they must be able to isolate the most critical defects for more thorough review, classification and analysis. While techniques such as nuisance filtering and automatic defect binning are useful for refining the defect population, emerging methods should be considered for extracting the most yield-relevant defects from these large defect sets, including the identification of systematic defects that often cause significant yield loss in advanced processes. Design based inspection is a promising set of novel techniques that links design data and defect inspection data, effectively improving the quality of the yield information produced by patterned wafer inspectors.

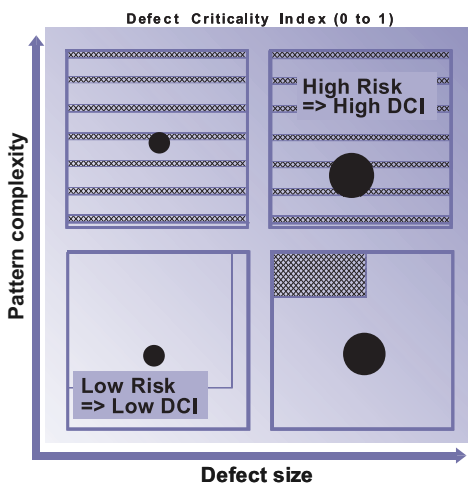


**Figure 1.** Assigning a Defect Criticality Index to each defect, according to design layout information and defect patch image, helps increase the percentage of yield-critical defects in a SEM review sample.

One component of design based inspection is the Defect Criticality Index (DCI). The DCI is calculated for each defect using the GDS clip (design layout) information associated with the neighborhood of the defect and defect attributes such as size and brightness. It is assigned to each defect during wafer inspection, and ranges in value from 0 to 1. Defects having an index near 0, such as a small defect on a sparse background, tend not to be yield-relevant. Defects having an index approaching 1.0, such as a large defect within complex background pattern, tend to have a high probability of affecting yield. The DCI method is particularly useful when used for review sample shaping. While conventional methods typically send a random sample of defects for review, a new methodology preferentially selects defects with a high DCI for SEM review and classification. This technique increases the ratio of defects of interest (DOI) in the review sample and filters out defects with a low probability of affecting yield, resulting in a more actionable defect Pareto. Preliminary results have shown that this new methodology improves the fraction of DOI in the review sample by as much as a factor of five.

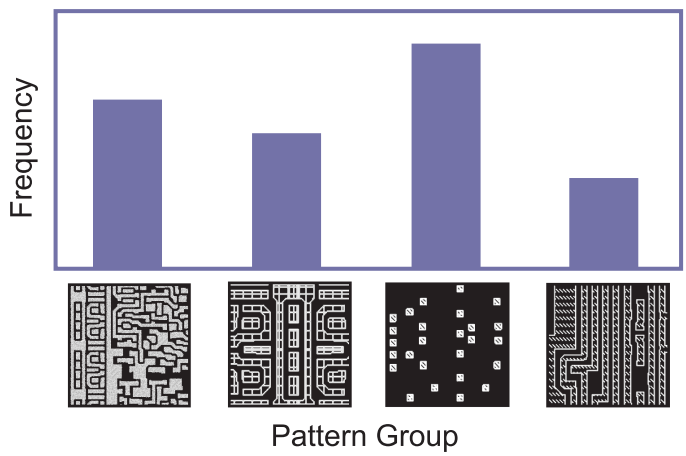


**Figure 2.** Design Based Binning is a novel methodology which groups defects based on design layout and defect patch image information, producing a pattern-based defect Pareto.

Another element of design based inspection is an innovative binning methodology called Design Based Binning (DBB). DBB uses defect patch image and chip design information to sort defects and create a pattern-based Pareto. Every defect is mapped to its GDS coordinate; the corresponding pattern background is extracted; then, the defects are binned based on pattern matching, patch image and design attributes such as line width and line space. DBB can provide designers with critical information, helping to shorten their early development cycle. For example, the design layout can be optimized using information from DBB which identifies and quantifies the printability of various features, such as line widths. DBB also can be used to find pattern failures that are *spatially random*, but *structurally systematic* – information useful for OPC and design/layout improvements which would not be detected using on-wafer reticle verification techniques such as PWQ. DBB is well-suited to serve as an efficient in-line monitor for systematic and random defects, providing designers with the information required to solve critical pattern printability issues.

To learn more about design based inspection, go to:
www.kla-tencor.com/07DecemberJP