Using Design Based Binning to Improve Defect Excursion Control for 45nm Production

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Design Based Binning (DBB), a method that integrates design information and defect inspection results, can be used to identify design locations where defects frequently occur, allowing advanced fabs to correct systematic problems through design or OPC modifications. DBB techniques can also be extended to enable better monitoring for systematic and random defect excursions in production.

Introduction

For the 45nm node, immersion lithography has been a major enabling technology for pattern shrinkage. Litho R&D engineers have applied OPC and tighter process windows to mitigate the impact of decreasing pitch and complex pattern design. However, pattern-related systematic yield loss is still listed as a major barrier for 45nm advancement to production. Certain pattern designs are sensitive to process variation from film deposition, photo and etch steps. A combination of film over-deposition and under-etching at these steps can lead to film residue in the form of line bridging defects (Figure 1).

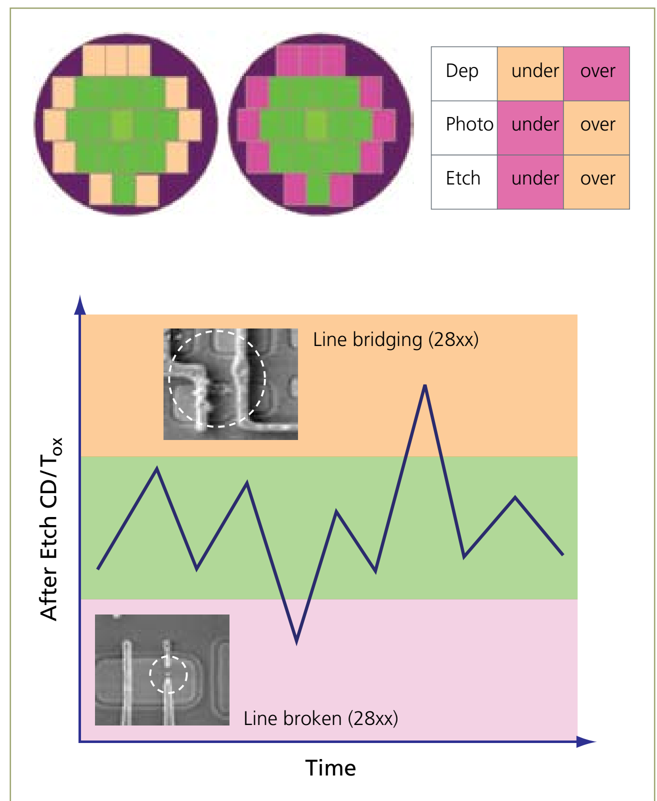

Figure 1: Marginal design and process variation can lead to systematic excursion events.

This problem will get worse in the production stage, with process variation arising from multiple tools and modules. With sensitive inspection tools and small-pixel inspection recipes, pattern excursions can be identified. However, if the failed pattern count is low (in tens) and the total defect count is high (in thousands), current random sampling methods for SEM review, sampling 50 to 100 defects per wafer, can easily miss this excursion. Consequences can be significant, affecting yield, time to market and profit.

To address this issue, we employed a new methodology called Design Based Binning (DBB) that bins defects of interest according to their background pattern information. This information can be used to identify certain design locations where defects frequently occur. While these known, systematic pattern problems might be addressed with design/OPC modifications, they can still show up in production as excursions, and thus need to be constantly monitored. We can bin and track for such excursions with DBC (Design Based Classification, shown conceptually in Figure 2).

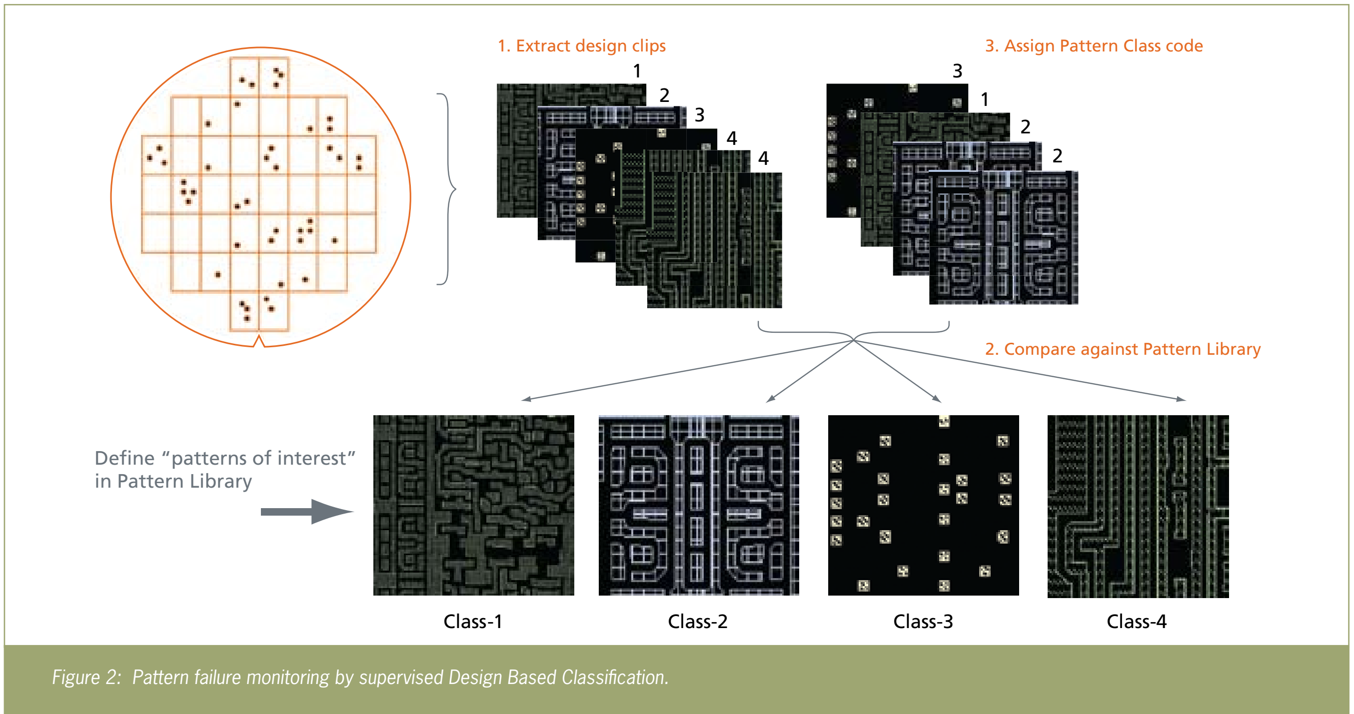

Figure 2: Pattern failure monitoring by supervised Design Based Classification.

We can also use design and pattern information to monitor for random excursions. For each defect, a proprietary model merges its background pattern information with the size information assigned by the inspection tool, and generates a value to indicate the defect's likely yield impact. This Defect Criticality Index (DCI) ranges in value from 0 to 1.

By applying DBC and DCI to inspection results, we can build SPC charts to monitor systematic (DBC) and random (DCI) excursions. During the R&D stage, we can identify marginal pattern sites from either the design library or PWQ/FEM data. These risky pattern features will be built into a hot spot library and passed to production for monitoring. When a defect excursion happens during a pilot/production stage, the SPC chart will flag the problem. This will trigger additional defect sampling and review specific to the problematic pattern location. This methodology will enable us to take prompt corrective action at an early stage of the excursion, before many wafers are lost.

Experimental Data and Results

Wafer inspection and defect binning

We selected four SRAM wafers from the same lot, processed through the gate etch layer. We inspected these wafers using a brightfield inspection tool (KLA-Tencor 28xx), and reviewed around 50 randomly chosen defects on each wafer with the review SEM. We classified the defects manually, and normalized the data by defect type to check for excursions. The results, shown in Figure 3, indicated potential random excursions on wafers 3 and 4, as well as a systematic problem (type B) on wafer 4. However, due to the high total defect count on the

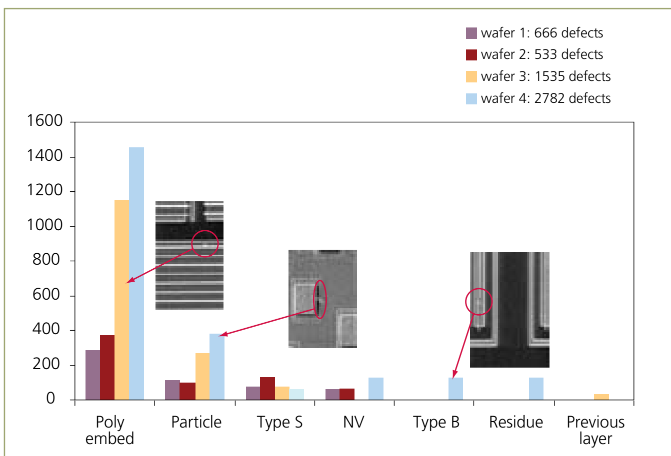

Figure 3: Defect Pareto resulting from traditional method for review sampling and normalization.

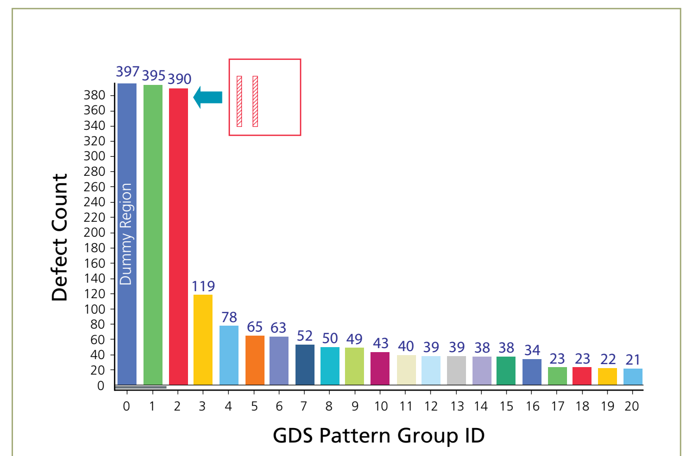

Figure 4: Unsupervised Design Based Binning results on Wafer 4. Top bin represents defects on dummy pattern.

wafers, and the limited SEM review sample (average=42), the excursion signal did not clearly indicate the extent of the problem.

DBC binning results for systematic excursion monitoring

Next, results from these four wafers were binned using DBB. An example of DBB results from wafer #4 is shown in Figure 4. The top bin in the chart represents defects on dummy pattern regions, which are regarded as "don't care" regions. These defects can be filtered out with no impact on yield. By running DBC analysis on the four wafers, we found that one pattern type from the hot spot library had a high defect count on wafer 4 (Figure 5). This wafer was sent for further SEM review, and the outcome was confirmed as a systematic excursion.

DCI results for random excursion monitoring

For each defect, DCI was calculated automatically. A lower index indicates that a defect is less critical. The DCI results can help prioritize defects for inclusion in the SEM review sample. An example of DCI values with their corresponding defect images is given in Figure 6. To protect customer IP, all GDS clips were hand drawn and do not reflect their original design.

Based on SEM review and DCI number, we set a threshold of 0.1 for non-critical random defects (small defects on spare pattern). A plot of the percentage of non-critical defects (Figure 7) indicates that wafer #3 had the highest percentage of critical random defects among the four wafers. This result motivated us to review a sample of defects from the higher DCI group on the SEM. We identified a polymer excursion defect which was missed by the traditional sampling method.

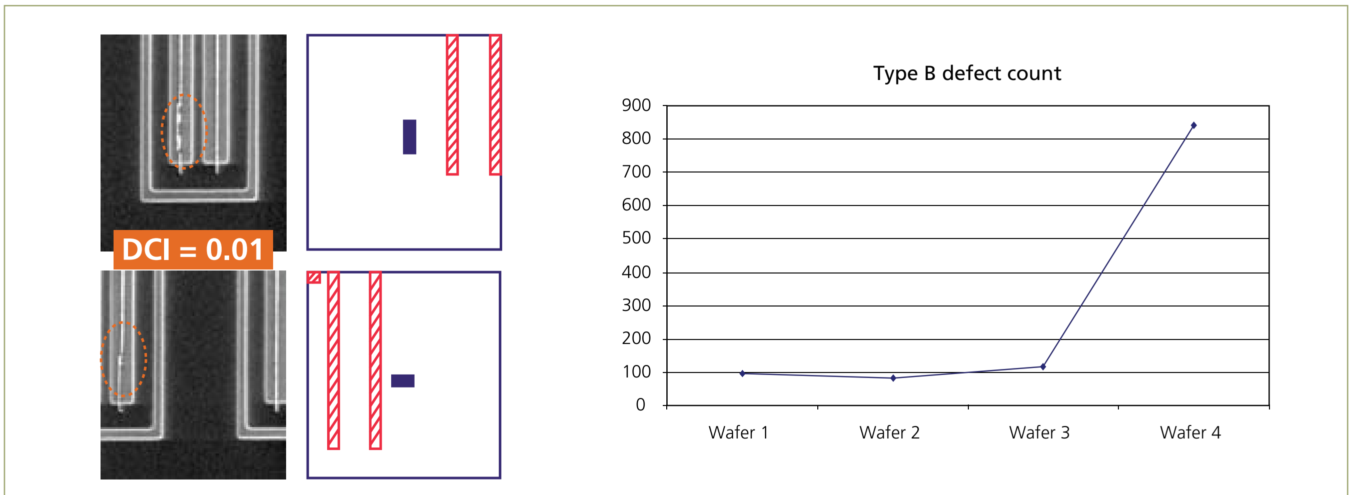

Figure 5: DBC results indicate Wafer #4 had a systematic excursion: the "line broken" defect type shown in the SEM images.

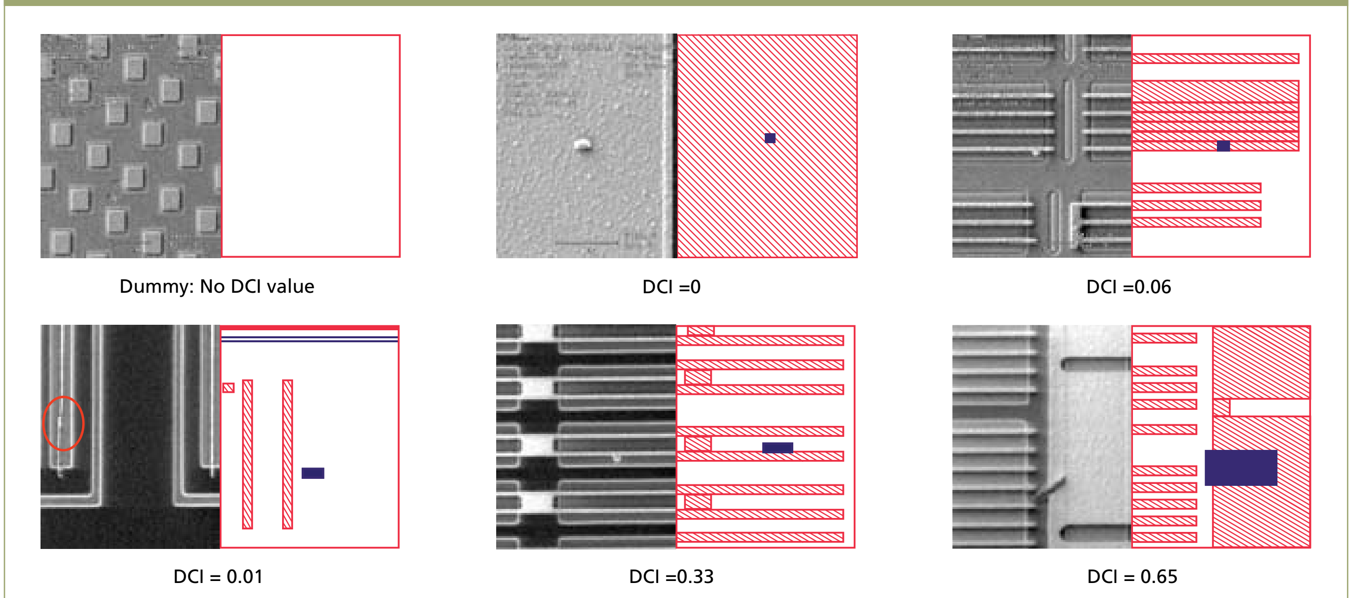

Figure 6: DCI samples show defect size (blue rectangle) and pattern background information (red line drawings, disguised to protect customer IP).

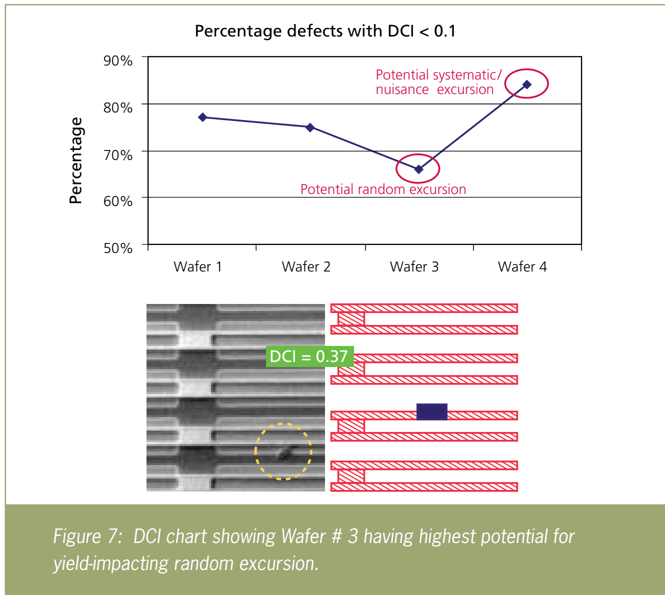

Figure 7: DCI chart showing Wafer # 3 having highest potential for yield-impacting random excursion.

Summary

We summarized the comparison between the new DBB methodology and the current UMC practice in Table 1.

From many use cases in UMC, DBB has shown benefits in finding pattern-related defects on 45nm device wafers. DBB is a novel method for finding systematic defects, and has the potential to serve as an in-line monitor for systematic and random excursions.

Item	Current Practice	New DBB Methodology
Defect on dummy	Many defects on dummy pattern	0 %
Nuisance (poly grain/cap, small particle/field)	Vary/high defect count	Use DCI < 0.1 to screen out random non-DOI
Systematic defect (pattern failure) identification	Repeater analysis Review same type > 2	Control chart on "known pattern of interest (POI)"
Excursion trigger	By total defect counts-Bad die%	By count and DCI % (e.g. for DCI < 0.1)
SEM review sampling, 50 defects	Random selection	Systematic defect with DBC and random review with high DCI

Table 1: UMC current practice compared with DBB method

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