Systematic Defect Management by Design Aware Inspection

Ellis Chang, Allen Park
KLA –Tencor Corporation,
Milpitas, CA, USA

ABSTRACT

As electronic users demand smaller form factor of devices that can pack more functionality, Semiconductor industry has been marching towards smaller design rules. With the advancement in newer design nodes such as 32nm and beyond, additional challenges are being faced by the Fabs developing the process technologies. These challenges are often difficult to solve using traditional approaches and therefore novel techniques must be implemented to address the challenges accordingly. In the area of wafer inspection, the traditional approach of simply using wafer level data alone is no longer sufficient. Some specific challenges regarding systematic defects that the Fabs are facing today are discussed in this paper along with several approaches that can help meet the challenges. These new approaches can help to take the wafer inspection to the next level in order to detect and identify key yield deterrents that limit reaching yield entitlement in a timely manner.

Keywords: Design, Process Integration, DFM, Defect Inspection, GDS, hotspot, OPC

INTRODUCTION

Based on three years of field engagement at IDM and Foundry Fabs, we have identified top defect challenges faced by Fabs developing devices for the 32/28nm technology node. The study included both Logic and Memory Fabs that are developing SOC, DRAM and Flash devices. Among the challenges identified were due to introduction of new materials, wafer edge die metrology and yield, and ever increasing Systematic defects. Major constituents of systematic defects were caused by process variation and interaction among design, process and OPC as illustrated in the results of the meta-analysis in Figure 1. The survey results, supported by previously published works [1-2], showed that several types of systematic defects were prevalent at these leading-edge nodes. With reduced lifecycle of devices and marketing window, systematic defects must be identified early in process development and ramp stages. In this document, novel design-aware defect management techniques for detecting and identifying systematic defects efficiently are discussed with specific examples from inspection set up to post-inspection analysis.

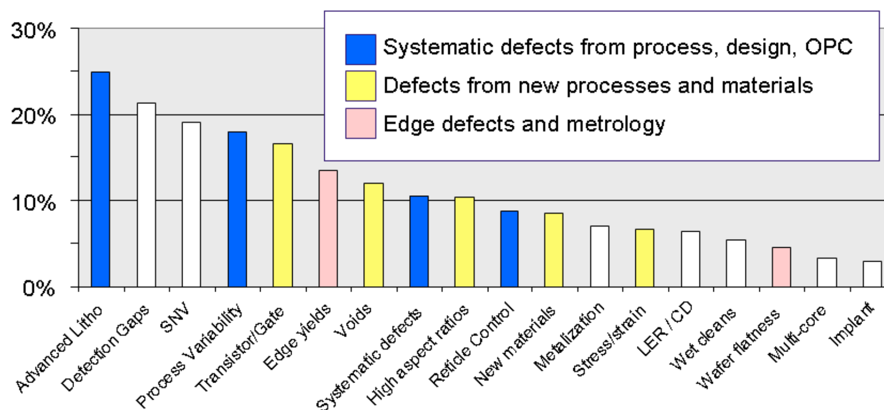


Figure 1: Composite data from field studies at IDM, memory and foundry fabs identified systematic defects from process, design and OPC interactions as some of the top challenges for the 32/28nm technology node.

Lithography Asia 2009, edited by Alek C. Chen, Woo-Sung Han, Burn J. Lin, Anthony Yen,
Proc. of SPIE Vol. 7520, 75201C · © 2009 SPIE · CCC code: 0277-786X/09/$18 · doi: 10.1117/12.836993

Downloaded from SPIE Digital Library on 22 Dec 2009 to 192.146.1.254. Terms of Use: http://spiedl.org/terms

APPROACH

Several ingredients are needed to achieve an effective management of systematic defects. First detection of the key defect types is important. Conventional approach of blanket inspection may produce too many defects while not providing the optimal detection sensitivity. Being able to develop a 'surgical' inspection not only reduces overall defect count but can also improve sensitivity by focusing on the right areas. Filtering and grouping of pertinent defects during the inspection further helps increase signal by processing defects even before the final defect counts are reported. Once all critical defects are detected, binning and prioritization enable users to identify key defect types while optimizing the use of SEM review capacity. This type of approach has been demonstrated in earlier work [3]. To implement such comprehensive design-aware defect management, two major components are required: 1) Use of design layout data (e.g. GDS or OASIS file) to inspect critical areas identified by both simulation and empirical data gathering during process development, and 2) Identification of systematic pattern failures and random particles through defect binning by design and functional areas. Figure 2 illustrates data flow of how such approach can be implemented. Using the design-defect integrated system; systematic defects can be identified and verified using SEM review.

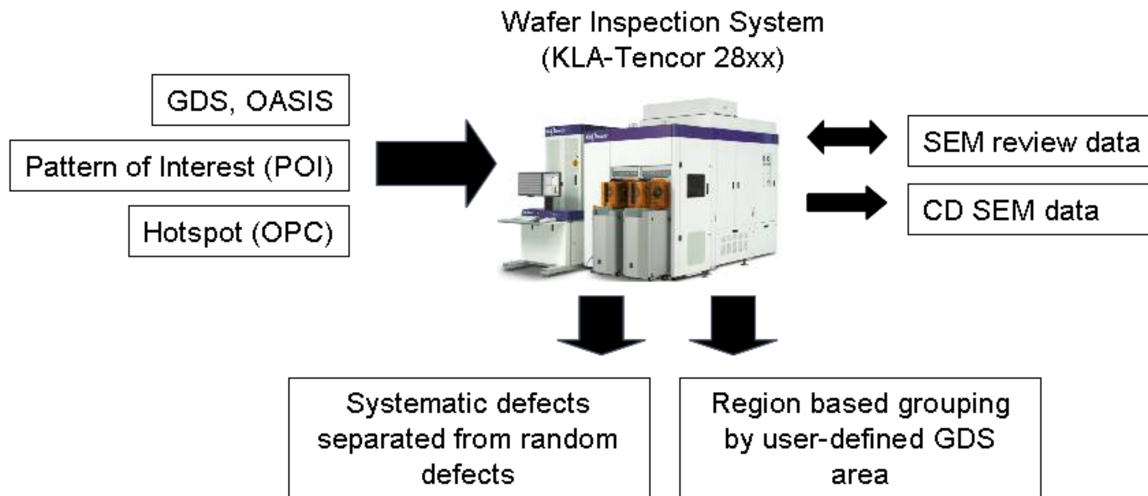


Figure 2: Integration of design data in defect inspection enables new capability in both detection and monitoring of systematic defects.

DEPLOYMENT

Design-aware defect inspection can be used in many applications. In this work we discuss the following case studies:

1) Use of design data to identify systematic defects due to design-process interaction. Weak pattern can fail in a spatially random distribution across die and wafer where not every die will exhibit a failure. These failures are not just due to reticle or design issues but can occur due to design-process interaction. Due to the frequency and location of failure, it is often difficult to identify the defects among high volume of defect data. However such failures can be identified by the use of design-based grouping easily since the defects failure due to certain structures can be grouped based on the pattern in design data (Figure 3).

Downloaded from SPIE Digital Library on 22 Dec 2009 to 192.146.1.254. Terms of Use: http://spiedl.org/terms

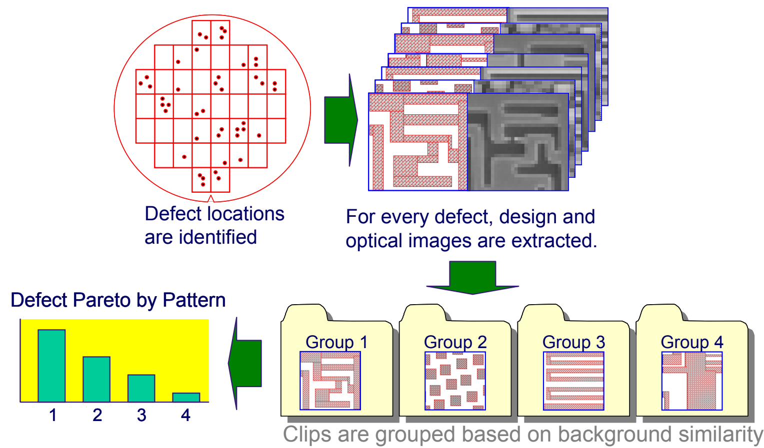


Figure 3: Illustration of how defect data can be grouping according to the design data to identify systematic defects occurring at particular pattern types.

2) Efficiency in inspection care-area generation. A typical SOC device can contain thousands of scattered SRAM areas, however it is also important to separate them from the random logic area to improve inspection sensitivity and to separate defects that are impacting the memory structures. Due to the count and the distribution of the SRAMs, the time it takes for an engineer to find them and group them into a single care area while setting up an inspection recipe is often very time consuming. By searching SRAM in design data these areas can be quickly identified in minutes rather than hours of manual operation, and a customized inspection recipe, enabling optimal sensitivity in each area of the die, can be built within a short time allotted by the Fab. Limited tool availability is often a challenge for user setting up inspection recipes and such capability of being able to scan design off-line mitigate the burden of using tool time. Results from tests of this concept in one fab are given in Figure 4.

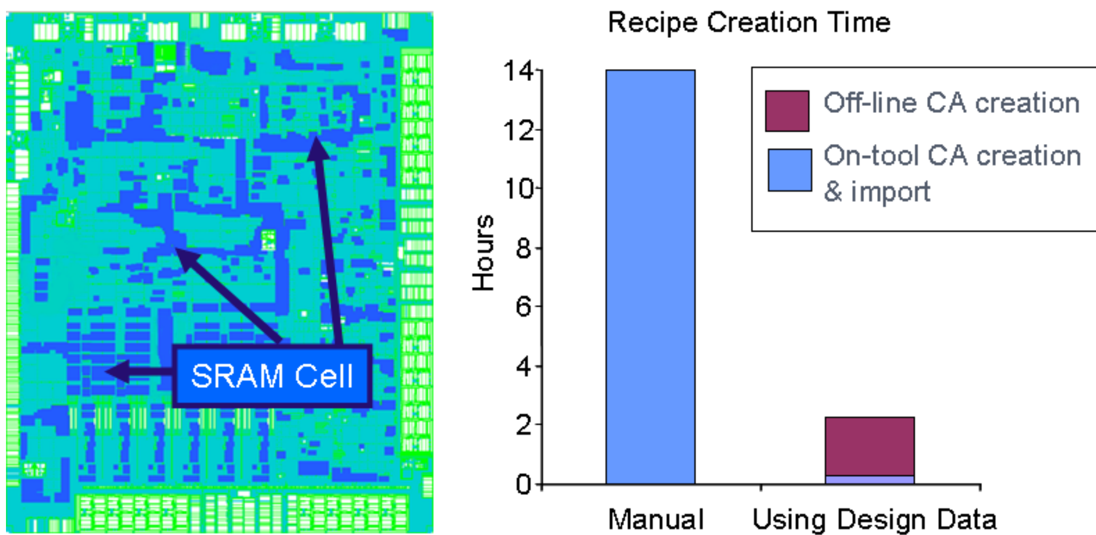
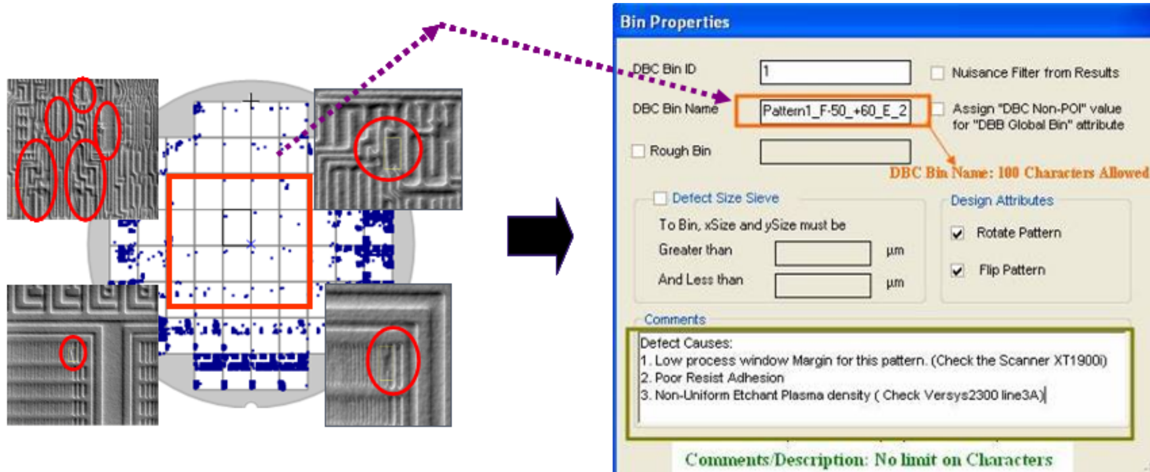


Figure 4. SOC exhibits many embedded SRAM cells. It is very time consuming to identify all SRAM cells for array-mode inspection. Utilizing design data, recipe generation efficiency was improved by 7X.

Downloaded from SPIE Digital Library on 22 Dec 2009 to 192.146.1.254. Terms of Use: http://spiedl.org/terms

3) Use of marginal pattern information. Marginal patterns that failure at intermittent frequency and location are difficult to detect but can be a good source of information for monitoring health of lithography tools. Focus-Exposure-Matrix wafer is often used by Fabs to understand photo process window where device structures can be printed successfully. Using Design data, failing pattern can be grouped according to the background pattern. Such pattern can either be grouped ad-hoc or be saved as a pattern library once the patterns are known. By evaluating the spatial signature of weak patterns using a pattern library, litho tool condition can be monitored. For example, a process window may show +/- 0. 06 um or +/- 0.04 um depending on the health of the litho tools. For known marginal pattern types, they can be assigned with photo condition where they fail to automatically monitor in case they fail due to litho tools drifting. Similarly process split or mask revision can be analyzed quickly by using a pattern library that contains marginal pattern. Once the pattern is registered into a library, defects that are occurring at the particular sites can be automatically monitored, saving time and effort evaluating the results. These methodologies are illustrated in Figures 5 and 6.

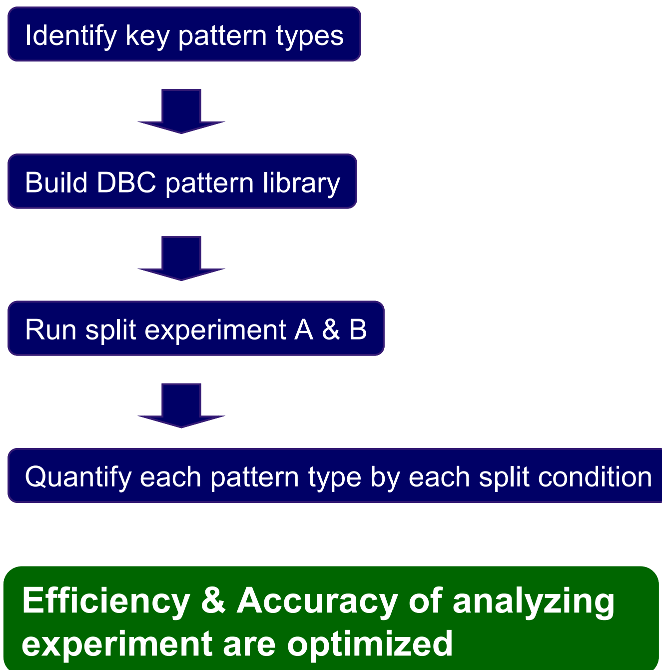


Step 1: Perform Design-Aware Binning on FEM wafer to discover new systematic defects under different FEM conditions

Step 2: Document POI (pattern of interest) in Design-Aware Classification library with FEM condition and possible root cause

Figure 5. BKM developed at major foundry uses signature of weak patterns to monitor lithography tools where litho failure modes can be monitored by specific pattern and location.

Downloaded from SPIE Digital Library on 22 Dec 2009 to 192.146.1.254. Terms of Use: http://spiedl.org/terms



Experiment result: Split A & B

Design-Aware Library	A	B
Bin-1	Count X	Count Y
Bin-2	Count Z	Count F
Bin-3	Count N	Count P
Bin-4	Count P	Count W
Bin-5	Count T	Count K

Figure 6. Design-aware inspection technique accelerates analysis of split experiment by quantifying analysis of pattern failures with the use of pattern library.

SUMMARY

In this paper it is show that with the increase in systematic defects at the 32/28nm nodes. Integration of design data into the Fab environment proves valuable and novel approach in meeting the challenges detection and identification of systematic defects. In the first case study, introduction of design information helped identify weak pattern distributed randomly across the wafer. In the second case study, use of design information increased productivity in inspection recipe setup through accurate care-area definition and by permitting off-line setup. In the third case study, design information enabled engineers to make best use of marginal pattern data to monitor their litho tools. Both design-based setup where detection ability can be optimized and design-based binning where signal can be visualized proved to be essential part of managing systematic defects for 32 nm process and beyond.

REFERENCES

[1] Yeh, J. H. and Park, A., "Novel Technique to Separate Systematic and Random Defects During 65 nm and 45 nm Process Development", Proceedings, SPIE 2007
[2] S. Jensen, "Utilizing Design Layout Information to Improve Efficiency of SEM Defect Review Sampling", Proceedings, ASMC 2008
[3] P.R. Jeng, et al, Accelerating 32nm BEOL technology development by advanced wafer inspection methodology, SPIE Asia 2008

Downloaded from SPIE Digital Library on 22 Dec 2009 to 192.146.1.254. Terms of Use: http://spiedl.org/terms