Defect Criticality Index (DCI): A New Methodology to Significantly Improve DOI Sampling Rate in a 45nm Production Environment

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To reduce the percentage of non-DOI or nuisance defect types populating the defect Pareto, a new methodology associates GDS clip (design layout) information with every defect detected by the inspection system. This information, together with traditional inspector-assigned attributes such as size and brightness, is used to assign a Defect Criticality Index (DCI) to each defect. When only high-DCI defects are included in the SEM review sample, resulting defect Paretos are more actionable. For a gate process on a 45nm logic device, the DOI extraction rate improved from 12% to 68%.

Introduction

Because smaller defects become yield relevant as minimum design features shrink, manufacturers have had to increase wafer inspection sensitivity in order to capture all defects of interest (DOI). This has resulted in an increased number of detected defects and a higher percentage of non-DOI or nuisance defect types during in-line monitoring. When a SEM review tool is used to observe and classify these defects in order to determine root cause, a problem arises. Time constraints in the fab usually limit review sampling to a relatively small, fixed defect sample per wafer—typically 50 to 100 defects. If 100 defects were sampled from a population of several thousand defects on a wafer, the sampling rate would be only a few percent. Under such conditions, it is difficult to identify DOI types that should be monitored in production. A new sampling method is required for effective DOI capture under very low sampling-rate conditions (Figure 1).

In this paper, we verify the effectiveness of utilizing design data for the separation of DOI from non-DOI. We also propose a new review sampling method that assigns a "criticality" index based on design data. This index is used together with traditional defect information for improved DOI sampling.

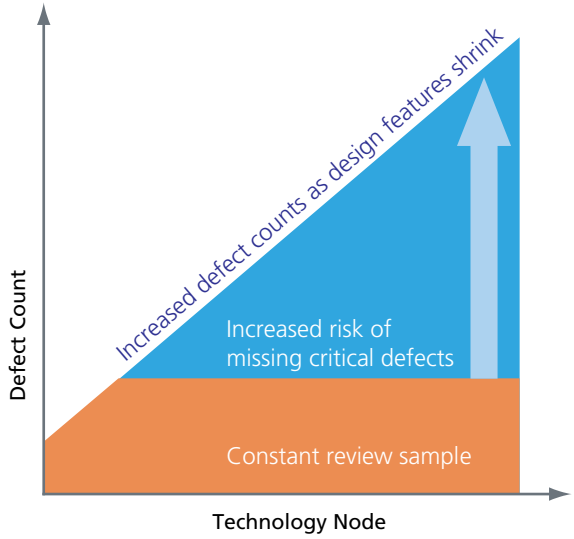

Figure 1: Increased risk with technology node of missing critical defects, from low review sampling rate.

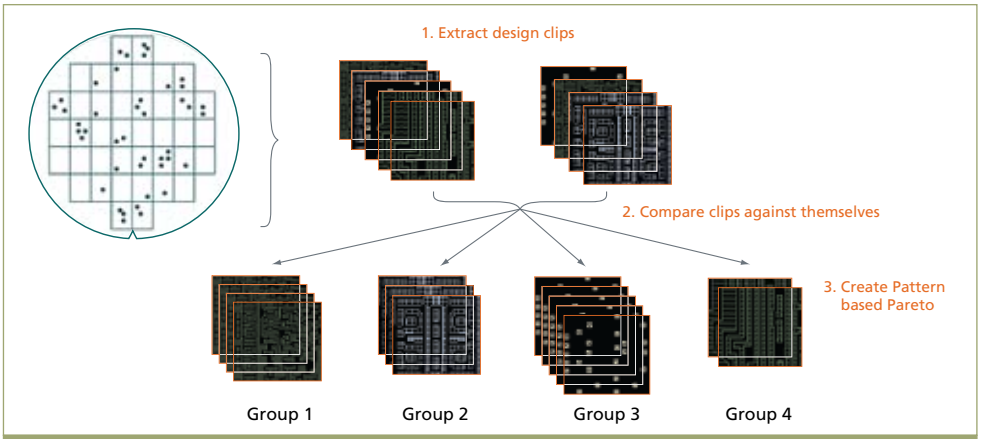

Figure 2: Overview of Design Based Binning.

System Overview

Design Based Binning

The principles of Design Based Binning are shown in Figure 2. After in-line defect inspection, the following actions occur:

1. Each defect is mapped to its GDS coordinate, and the corresponding pattern background data is extracted (GDS clip). Any GDS layer can be chosen for mapping.
2. The GDS clips are compared.
3. Defects are binned based on pattern matching, patch image and design attributes such as line width and line space.

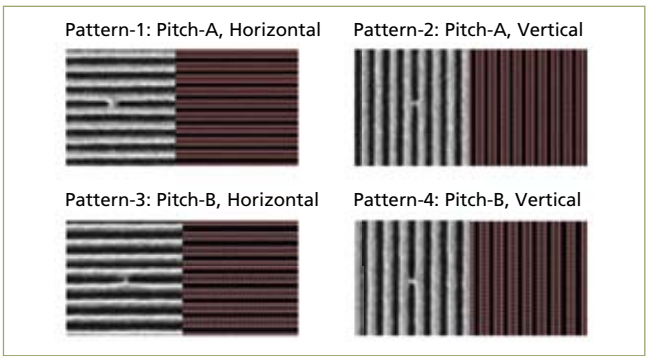

Figure 3: TEG pattern used for system verification.

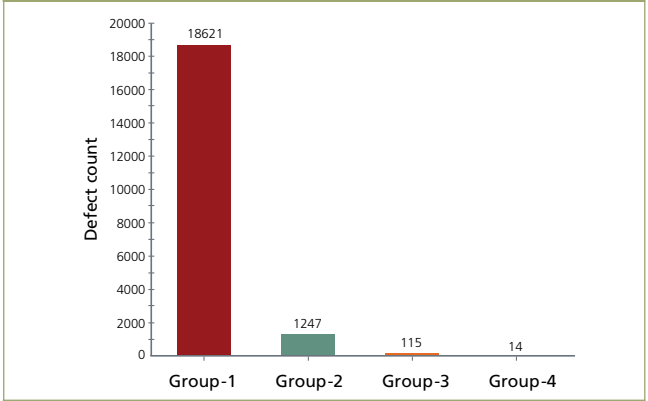

Figure 4: Pareto chart by pattern group..

The binning results are utilized for DOI/non-DOI separation and systematic/non-systematic separation analysis.

System verification

To verify this system we used a TEG (Test Element Group: includes all test elements from a single transistor to small-scale SRAM circuits, etc.) pattern as shown in Figure 3, line-and-space patterns, with design rule and line directions different in each TEG block. A broadband bright-field system (KLA-Tencor 28xx) was used to inspect the wafer after metal 1 trench formation.

After wafer inspection, we obtained the GDS clip of the metal 1 layer and performed Design Based Binning as described above. Auto classification created four groups representing the four background patterns. The resulting Pareto chart by pattern group is shown in Figure 4.

The defect count in each group exhibited wide variation. Group 1, representing the horizontal pattern with the smaller line spacing, showed the highest defect count. It is possible to determine pattern-specific defects by restricting SEM review sampling to each pattern group in turn.

Figure 5 shows part of a defect wafer map color coded by pattern group. Each TEG block clearly shows a single color, which suggests good accuracy and purity of the auto classification by background pattern.

Figure 6 shows the Design Based Binning results for defect data from a 45nm SRAM gate process. After wafer inspection, the GDS clip of the gate layer was extracted and the patterns were automatically classified. The pattern type showing the most defects was found to be "blank clip" (no gate-layer pattern); thus, defects on blank areas were dominant in the inspection data. These defects are non-DOI.

Defect Criticality Index (DCI)

Each defect detected by an inspection tool has attributes such as defect size and brightness, in addition to coordinate data that indicate its location on the wafer. These defect attributes are traditionally utilized for automatic defect classification.

Figure 7 shows the new concept of the Defect Criticality Index (DCI). Generally, the criticality (yield relevance) of a defect is determined by the background pattern associated with the neighborhood of the defect, along with traditional defect attributes. For example, a small defect on a sparse background (low pattern complexity) would be considered less yield relevant. On the other hand, a large defect on a complex background pattern tends to have relatively higher impact on yield.

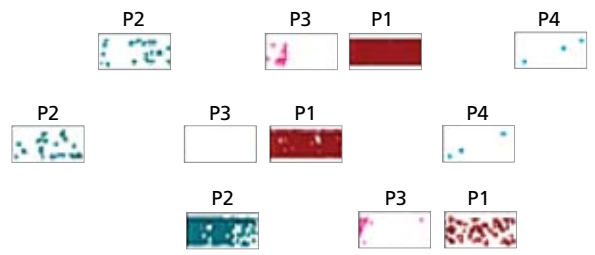

Figure 5: Defect map by pattern group.

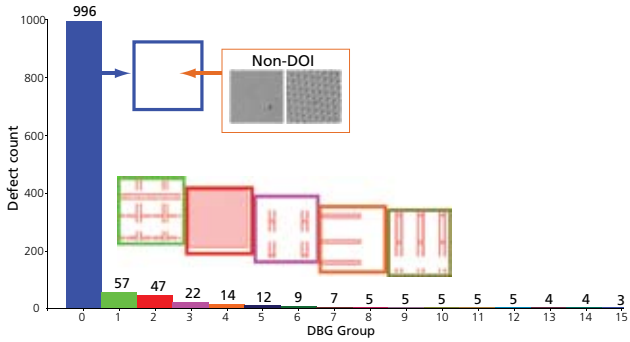

Figure 6: Pareto chart resulting from Design Based Binning for 45nm SRAM gate layer. Top defect type is non-DOI 'blank clip.'

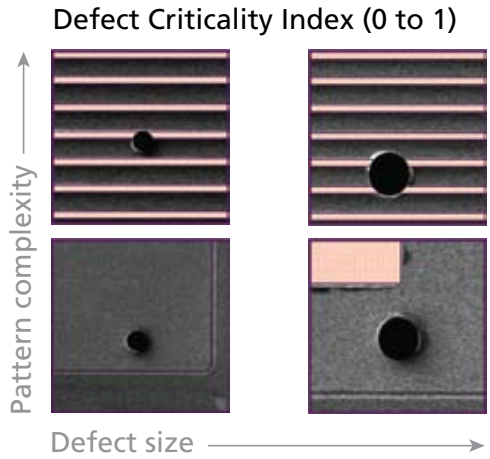

Figure 7: Defect Criticality Index concept.

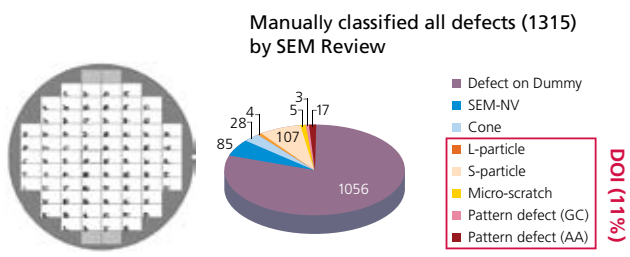

Figure 8: Complete defect data set for sampling experiment, based on 100% SEM review. Results show 11% DOI in the total population of detected defects, and five distinct DOI types. (45nm SRAM device, gate layer, inspected by KLA-Tencor 2800).

As with Design Based Binning, the design attribute for each defect is extracted from the GDS clip. Then the DCI is calculated by combining the design attribute with traditional defect attributes. DCI values range in value from 0 to 1 and are used to assess priority for inclusion in the SEM review sample.

Sampling experiment

In order to verify the DCI sampling method, we planned and executed the following experiment. First we inspected the wafer, which had a 45nm design rule TEG pattern, after salicide formation. We reviewed and manually classified all detected defects (total 1315 count) on the SEM. We identified five pattern defect and particle types as DOI. Non-DOI types included "defect on dummy pattern" and "cone" (Si spike). The DOI percentage in the full defect population was about 11% (Figure 8).

We then tested three methods for determining a 100-defect SEM review sample. The first was random selection, the method most commonly employed in fabs today. The Pareto generated by our random sample was considered the baseline. The second used the inspector's assigned defect size information to choose the 100 biggest defects for SEM review. The third used the new DCI method described above, selecting the 100 defects with the highest DCI values for the SEM review sample. For the calculation of the DCI, both defect size and design attributes were used.

Results and Discussion

Results of the sampling experiment are summarized in Figure 9. In the randomly sampled defect group (the baseline), 70% of defects were found on the dummy pattern. The total DOI percentage was 12% in the baseline Pareto (similar to the true DOI population found by 100% review), but only two of the five DOI types were represented in this Pareto.

In the sampling group ordered by defect size, the total DOI percentage improved to 33% and all five DOI types were represented. The best results were observed in the DCI-driven sampling group, which showed 68% DOI. The DCI Pareto also delivered the highest number of pattern defect AA, the pattern defect considered the most critical defect type.

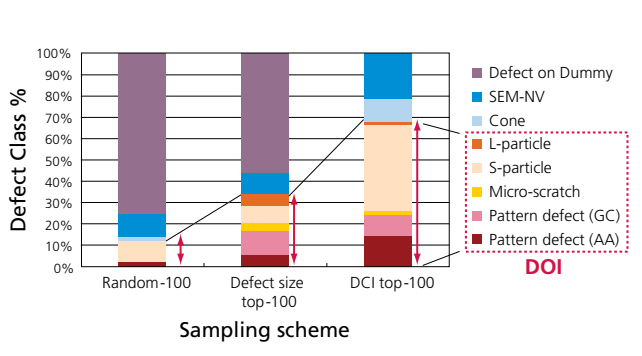

Figure 9: Comparison of DOI capture rate and DOI type for three different sampling scenarios.

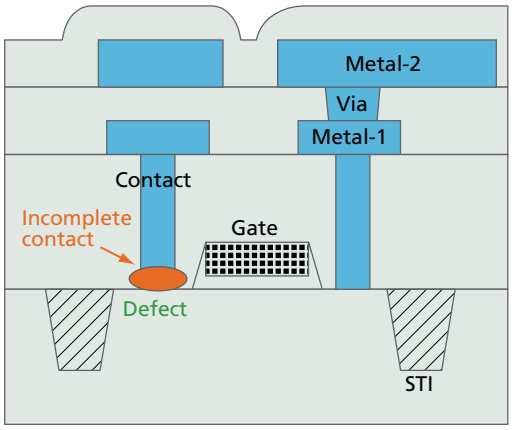

Figure 10: Particles at the gate layer could cause an incomplete contact.

One of the reasons the DOI ratio in the DCI sampling group was so high is that it totally eliminated the prevalent defect-on-dummy type from the sampling group. Since a specific GDS layer code is usually assigned to the dummy pattern, GDS clips that only include dummy pattern can be perfectly separated.

We also compared SEM images of particle defects from the random sample with those of the DCI-driven sample. In the random sampling group, the majority were particles in the field oxide region, while in the DCI sampling group, more particles on transistor structures (active region and gate poly structure) were represented. This observation shows that DCI-ordered sampling can improve the quality of the review sample in addition to boosting its DOI ratio.

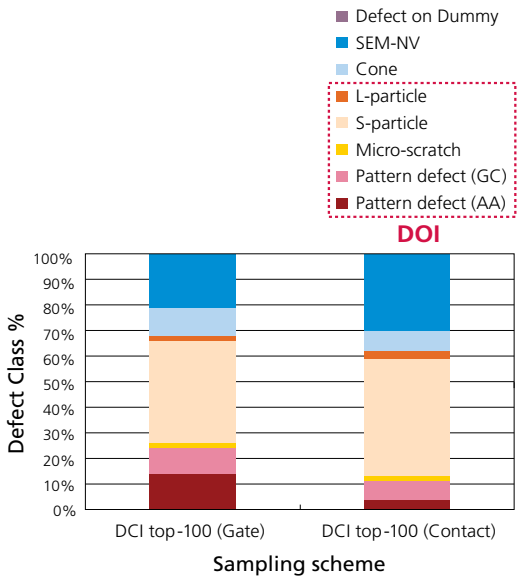

Figure 11: Comparison of DCI-generated defect Paretos for gate and contact layers, based on gate defect data, and both gate and contact GDS information.

Gate process–related defects can also affect subsequent contact formation. As shown in Figure 10, particles that have fallen on gate structures may cause incomplete contacts. By overlaying contact layer GDS data (a future layer), another DCI set can be calculated. The new set of DCI values could help estimate yield-relevant defectivity for the upcoming contact layer.

To validate this idea, we designed another sampling experiment. We used the defect data from the gate layer together with GDS data from both gate and contact. Using the DCI methodology, we compared the results, shown in Figure 11. The DOI percentage based on the contact-layer GDS was 62%, nearly equivalent to the 68% value based on the gate-layer GDS. However, in the contact-layer GDS case, more particle-type defects (large particle and small particle) were included in the Pareto. Clearly some of these defects were less critical (lower DCI) at gate than at contact, where they could cause contact failure. This result suggests that DCI can use a combination of current-layer defect data and future-layer GDS data to predict yield for subsequent processes.

Conclusion

A new sampling method assigns a Defect Criticality Index (DCI) to all defects detected by an inspection tool and uses this information to select a SEM review sample skewed toward a higher percentage of DOI. The DCI is calculated for each defect by using a combination of traditional defect attributes assigned by the inspection system and design information associated with the location of the defect.

We verified the value of this methodology on a 45nm logic device. At the gate process, the DOI extraction rate was improved from 12% to 68%. Furthermore, by overlaying defect data from the gate layer with design data from the contact layer (a future layer), the DCI method was able to predict defect criticality for the contact process.

We achieved our purpose of creating defect Paretos with higher yield relevance, by using the DCI method to bias the SEM review sample toward more yield-critical defects. Further investigation is needed to correlate our results with yield data and optimize DCI application to line monitoring.

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