Immersion Lithography Defect Control

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Immersion lithography is a critical technology for ≤65nm device patterning. By increasing the effective numerical aperture of the imaging lens, immersion lithography provides improved optical resolution and an enhanced depth of focus. While this enables the printing of smaller features, the introduction of a fluid between the wafer and scanner has led to integration challenges related to intricate interactions between multiple process parameters – including the resist, topcoat, scanner and fluid. This complexity affects several areas of process control and requires an immersion litho cell qualification strategy to accelerate development and optimize production.

One process control challenge associated with immersion lithography involves reducing defectivity to levels comparable to or better than that obtained with dry lithography. This is necessary to meet the cost targets and production timing of the devices produced with immersion lithography. New defect challenges associated with immersion lithography include: immersion-specific defect types such as water marks, bubbles, bridging and protrusions; wafer edge defectivity; defects introduced by the addition of a top anti-reflective coating (TARC); and increased defect levels related to higher scan speeds. In order to address these defect challenges and achieve the fastest time to market at high yields, chipmakers require a comprehensive portfolio of immersion lithography defect solutions.

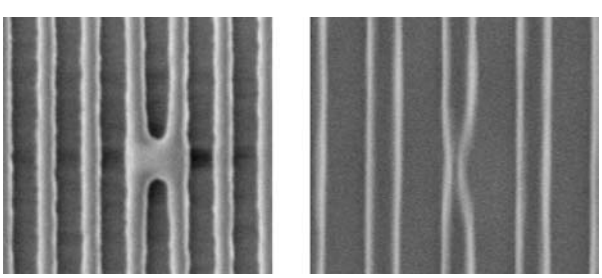

Figure 1: Immersion lithography defects captured by the 2800™ broadband brightfield inspector, including bridging (left) and line thinning (right).

Immersion lithography defect management involves inspectors that monitor both macro- and micro-litho defects on blanket, photo-cell monitor (PCM), and after-develop inspect (ADI) wafers, and also monitor wafer edge defectivity. Patterned wafer inspection is an important part of immersion lithography process control. High-resolution broadband brightfield inspectors, with features such as a tunable illuminator and selectable optical apertures, provide the broadest capture of yield-limiting immersion litho defects on both PCM and ADI wafers. These inspectors provide chipmakers with a low-risk defect monitoring solution for fast immersion process ramp, and production control.

Immersion lithography is closely coupled to the condition of the wafer's edge, as water goes over the edge during scanning. Device yield can be negatively affected by edge defects which are transported by the water from the edge of the wafer to the interior. These edge defects can include particles or residues, or flakes resulting from the delamination of the resist stack. Including a wafer edge inspector as part of the immersion lithography defect portfolio allows wafer edge issues to be quickly identified, correlated to defect problems on interior die, and solved before device yields are critically affected.

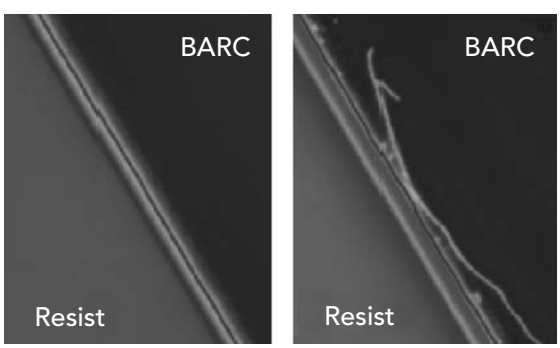

Figure 2: Example of flakes formed by the motion of the showerhead across the wafer's edge. Such immersion-related edge defects can be detected and monitored using the VisEdge™ inspection system.

Blanket wafer monitoring is also an essential part of immersion lithography defect control. Particle measurements on blanket wafers, when used in conjunction with defect source analysis, allow chipmakers to understand the process step where defects are being introduced. Additionally, high speed measurements of blanket wafer process signatures enable the quick identification of issues related to the introduction of water. Monitoring these process signatures is an effective way to quickly identify and reduce immersion lithography defectivity, leading to a faster and more efficient production ramp.

To learn more about immersion lithography defect control, go to:
www.kla-tencor.com/yield07Jan1